Device Data Book

WIRELESS RF PRODUCT DEVICE DATA

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Wireless RF Product Device Data

FOREWORD

This publication includes technical information for the several product families that comprise the Motorola portfolio of Wireless RF products. The product families include bipolar, RF BiCMOS, SiGe:C BiCMOS, LDMOS, MOSFET RF Power, and gallium arsenide chip technologies in a variety of ceramic and plastic surface mount packages. Discrete components, hybrid modules, and integrated circuits provide different levels of complexity in an effort to provide solutions for our customers' needs.

All devices are in alphanumeric order in the *Data Sheet Device Index* of this book. Just turn to the appropriate page for technical details of the known device. Complete device specifications are provided in the form of *Data Sheets* which are categorized by product type into six chapters for easy reference. *Selector Guides* by product family are provided at the beginning of the book as well as in the beginning of each chapter to enable quick comparisons of performance characteristics and to aid you in identifying devices that meet your functional performance requirements of frequency, output power, gain, or other parameters.

Chapters on Tape and Reel Options, Packaging Information, Applications and Product Literature include additional information to aid you in the design process.

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274. Please refer to our section on *On–line Access to Wireless Semiconductor Data* so that you will always have easy access to the most current information available on Motorola's Wireless RF product portfolio.

Refer to the *End of Life Product Index* section for information on products that are Not Recommended for New Design, End of Life or available through After Market Support.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer. MOTOROLA and the M logo are registered in the US Patent & Trademark Office. All other product or service names are the property of their respective owners.

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ABOUT THIS REVISION

This edition of the Wireless RF Product Device Data Book encompasses a considerable number of changes that have occurred since our last printing. Some devices have been removed from this book due to package changes or new technology replacements and many new devices have been added.

Application Notes, Engineering Bulletins and Article Reprints of special interest to designers of RF and IF equipment are available on the Motorola Semiconductor Product Sector Web site or are available through the Motorola Literature Distribution Center. Phone and fax numbers for ordering literature are listed on the back cover of this book and in our Accessing Data On–line section. See Chapter Ten for a complete listing of Application Literature.

For information on products that are Not Recommended for New Design, End of Life or available through After Market Support, see the End of Life Product Index section in this data book.

For Cross Reference information on Motorola replacement devices, please consult your local Distributor or Motorola Sales Office. See Chapter Eleven in this data book for a complete listing of Motorola Distributor and Worldwide Sales Offices.

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, pre–production, or first production stages. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.

BitGrabber is a trademark of Motorola, Inc.
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Teflon is a registered trademark of du Pont de Nemours & Co., Inc.
Thermal Clad is a trademark of the Bergquist Company

Access Data On–Line! – Use Motorola's SPS Internet Server

Motorola SPS has provided a World Wide Web Server to deliver Motorola SPS technical data to the global Internet community. Available online are the SPS Product Library, Documentation Library, Tools Library, Industry Focus sites, Design Resource sites, Technical Helpline, Technical Training and Where to Buy at the following URL: http://www.motorola.com/semiconductors.

See the RF and IF Design Resource site at http://www.motorola.com/rf for specific Wireless RF Product support information for:

- Data sheets
- Applications notes
- Selector guides
- Packaging information
- Application information
- Models
- Reference designs
- Circuit board artwork
- Roadmaps
- Press releases
- Events

RF Reference Designs

- Great RF Performance for Specific Standard Broadcast Formats
- Low Cost Component Selection
- Complete BOM, Layout, PCB and All Design Information Available
- Integral Temperature Compensated Bias Circuits Included
- Extensive RF Characterizations

Motorola is pleased to offer applications specific reference designs to go along with our selection of high power RF transistors. These reference design examples show some of the many possible uses of the standard devices and they allow the customer's design engineers a fast and accurate tool to both evaluate the performance envelope and fully characterize the devices under a variety of different operating conditions.

Low cost component selection was chosen so that the end users could transition the design and all of its Bill of Materials into a high volume base station manufacturing process and be very cost competitive with other competing technologies.

The circuit board is made out of a recently developed ceramic loaded thermoset plastic woven glass material that offers very low material costs, low PCB fabrication cost, and yet still has an exceptionally low dissipation factor for low RF loss. The dielectric constant of this material is high enough to allow for compact, distributed element matching structures, yet of a reasonable value to make it relatively insensitive to fabrication and etching variations.

The circuit's matching and decoupling capacitors utilize a low cost silicon dioxide dielectric process rather than the traditional porcelain multi–layered assemblies and they offer low ESRs, very high Q's and tight capacitance value tolerances.

The reference design data sheet contains a wealth of information that customers can use to better understand the range and capabilities of the Motorola devices. Items included on the sheet include the basics such as the intended end use application (GSM, W–CDMA, etc.), the typical performance level expected (2% EVM, –40 dBc ACP, etc.) and some of the device features such as ESD protection and good thermal stability.

For more information, go to the following URL: http://www.motorola.com/rf. Select Tools.

RF LDMOS Models

Motorola continues to populate its LDMOS Model Library with the LDMOS MET (Motorola's Electro Thermal) models and with the LDMOS Root models. All product models available in the RF LDMOS Model Library (Root and MET) include package, bond wire and internal matching network effects.

The Motorola Electro Thermal (MET) model for RF LDMOS transistors is a nonlinear model that for the first time examines both electrical and thermal phenomena and can account for dynamic self–heating effects of device performance. It is specifically tailored to model high power RF LDMOS transistors used in wireless base station applications.

Implemented in the Agilent®EEsof®EDA Advanced Design System, APLAC®'s Analog Design Tool and Applied Wave Research's Microwave Office™, the MET LDMOS model is capable of performing small–signal, large–signal, harmonic–balance, noise and transient simulations. Because of its ability to simulate self–heating effects, the MET model is more accurate than existing models, enabling circuit designers to predict prototype performance more accurately and reduce design cycle time.

The current release of the MET LDMOS model is available for:

- Agilent EEsof's ADS® (UNIX and PC) nonlinear circuit simulator
- APLAC's Analog Design Tool
- Applied Wave Research's Microwave™ Office

The LDMOS Model Library is available for all major computer platforms supported by these simulators.

For more information, go to the following URL: http://www.motorola.com/rf/models.

Literature Centers

Printed literature can be obtained from the Literature Centers upon request. For those items that incur a cost, the U.S. Literature Center will accept Master Card and Visa.

How to reach us:

USA/EUROPE/Locations Not Listed:
Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
Phone: 1–800–441–2447 or 1–303–675–2140

JAPAN:
Motorola Japan Ltd.
SPS, Technical Information Center
3–20–1, Minami–Azabu. Minato–ku
Tokyo 106–8573 Japan
Phone: 81–3–3440–3569

ASIA/PACIFIC:
Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre
2 Dai King Street, Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
Phone: 852–26668334

Technical Information Center:
1–800–521–6274

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END OF LIFE PRODUCT INDEX

Motorola SPS follows the industry standard "EIA-724 Product Life Cycle Data Model" to track the life cycle of its product. This model tracks the product's life cycle from "Product Newly Introduced" to "Product Phase Out." Products can be phased for a variety of reasons: improved product performance, change in technology roadmap, process obsolescence, market decline, etc. When products are discontinued, a suggested possible replacement device or an alternative source of supply for discontinued devices are made available when possible.

For a list of discontinued devices with possible alternative suppliers, please contact your local Motorola sales office or authorized distributor, or visit the following URL:

http://www.motorola.com/rf

Wireless Infrastructure RF Products

Product	Last Order Date	Last Ship Date	Possible Replacement
Not Recommended for New Design			
MHW1224	—	—	MHW1224LA
MHW1304L	—	—	MHW1304LA
MHW7185CL	—	—	MHW7185C
End of Life			
CA2810C	3/4/02	9/4/02	MHW6342T
CA2830C	12/31/01	6/30/02	MHW6342T
CA2832C	4/6/02	10/6/02	None
CA901	4/6/02	10/6/02	MHW8182B
CA901A	4/6/02	10/6/02	MHW8182B
CA922	4/6/02	10/6/02	MHW8185
CA922A	4/6/02	10/6/02	MHW8185
MHL8018	4/6/02	10/6/02	None
MHL8115	4/6/02	10/6/02	None
MHL8118	4/6/02	10/6/02	None
MHW5182A	9/22/01	3/22/02	MHW7182B
MHW5222A	9/22/01	3/22/02	None
MHW6182	9/22/01	3/22/02	MHW7182B
MHW6272	9/22/01	3/22/02	MHW7272A
MHW7222A	9/22/01	3/22/02	MHW7222B
MHW7292	4/6/02	10/6/02	None
MHW8185LR	7/2/02	1/2/03	None
MHW8185R	12/8/01	6/8/02	None
MHW8205R	4/6/02	10/6/02	None
MHW8292	4/6/02	10/6/02	None
MHW910	12/31/02	6/30/03	MHVIC910HR2
MHW916	12/31/02	6/30/03	None
MRF1507T1	6/30/02	12/30/02	MRF1511T1 or MRF1517T1
MRF182	7/31/04	1/31/05	MRF9030
MRF182SR1	7/31/04	1/31/05	MRF9030S or MRF9030SR1
MRF183	7/31/04	1/31/05	MRF9045

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Product	Last Order Date	Last Ship Date	Possible Replacement
End of Life – continued			
MRF183S	7/31/04	1/31/05	MRF9045MR1 or MRF9045S
MRF183SR1	7/31/04	1/31/05	MRF9045MR1 or MRF9045S
MRF184	7/31/04	1/31/05	MRF9060
MRF184SR1	7/31/04	1/31/05	MRF9060SR1 or MRF9060MR1
MRF185	7/31/04	1/31/05	MRF9080
MRF186	7/31/04	1/31/05	MRF9120
MRF187	7/31/04	1/31/05	MRF9085
MRF187S	7/31/04	1/31/05	MRF9085SR3
MRF1946	9/15/01	3/15/02	MRF1535T1
MRF1946A	9/15/01	3/15/02	MRF1535T1
MRF20030R	9/15/01	3/15/02	MRF19030
MRF20060R	9/15/01	3/15/02	MRF19060
MRF20060RS	9/15/01	3/15/02	MRF19060
MRF247	9/15/01	3/15/02	MRF1550T1
MRF2628	9/15/01	3/15/02	None
MRF373	7/31/04	1/31/05	MRF373A
MRF373S	7/31/04	1/31/05	MRF373AS
MRF374	7/31/04	1/31/05	MRF374A
MRF492	9/15/01	3/15/02	MRF1550T1
MRF5015	9/15/01	3/15/02	None
MRF6401	9/15/01	3/15/02	None
MRF6404	9/15/01	3/15/02	MRF9030
MRF646	9/15/01	3/15/02	MRF1550T1
MRF648	9/15/01	3/15/02	MRF1550T1
MRF650	9/15/01	3/15/02	MRF1550T1
MRF652	9/15/01	3/15/02	MRF1518T1
MRF6522–060	7/31/04	1/31/05	MRF9060
MRF6522–10R1	7/31/04	1/31/05	MRF282SR1
MRF6522–5R1	7/31/04	1/31/05	MRF282ZR1 or MRF9002R2
MRF652S	10/23/00	4/23/01	MRF1518T1
MRF847	9/15/01	3/15/02	MRF9045
MRF857S	9/15/01	3/15/02	MRF9002R2
MRF897	9/15/01	3/15/02	MRF9045S
MRF897R	9/15/01	3/15/02	MRF9045
MRF898	9/15/01	3/15/02	MRF9060
MRF899	9/15/01	3/15/02	MRF9180
TPV8100B	9/15/01	3/15/02	None

For information on Wireless RF and IF handset products, see After Market Support at the following URL:

http://www.motorola.com/rf

AFTER MARKET SUPPORT

For a list of discontinued devices with possible alternative suppliers, please contact your local Motorola sales office or authorized distributor, or visit the following URL:

http://www.motorola.com/rf

For Wireless Infrastructure products transferred to another manufacturer, see the list of Wireless Infrastructure RF products below. After market support on these parts is available through M/A–COM. For additional information, contact M/A–COM Customer Service at (310) 320–6160 x 354 (voice), clarkj@tycoelectronics.com (email) or (310) 618–9191 (FAX).

2N6439	MRF137	MRF171A	MRF317
MRF10005	MRF140	MRF173	MRF321
MRF1000MB	MRF141	MRF173CQ	MRF323
MRF10031	MRF141G	MRF174	MRF327
MRF1004MB	MRF148A	MRF175GU	MRF392
MRF10120	MRF150	MRF175GV	MRF393
MRF10150	MRF151	MRF175LU	MRF421
MRF10350	MRF151G	MRF176GU	MRF422
MRF10502	MRF154	MRF176GV	MRF426
MRF1090MA	MRF157	MRF177	MRF428
MRF1090MB	MRF158	MRF275G	MRF429
MRF1150MA	MRF160	MRF275L	MRF448
MRF1150MB	MRF16006	MRF3104	MRF454
MRF134	MRF16030	MRF313	MRF455
MRF136	MRF166C	MRF314	MRF587
MRF136Y	MRF166W	MRF316	

Chapter One

Wireless RF Product Selector Guide

As a leading supplier of semiconductor products, Motorola has a broad RF portfolio of products that serve the wireless infrastructure and subscriber markets. Utilizing LDMOS, BiCMOS, GaAs and SMARTMOS™ technologies, Motorola is committed to the development of new products and expansion of its product offerings to meet the increasing global demands of ISM band and personal communications systems, including cellular phone, broadband data, TV broadcast, land mobile and CATV systems.

How to Use This Selector Guide

The RF Monolithic Integrated Circuits and the RF/IF Integrated Circuits products in this guide are divided into three major functional categories: RF Front End ICs, RF/IF Subsystem ICs and Frequency Synthesis. Each of these categories is further subdivided based on circuit functionality. This structure differentiates highly integrated subsystem ICs from fundamental circuit building blocks and discrete transistors.

The Power LDMOS Transistors, Power GaAs Transistors, Power Amplifier Modules and CATV Distribution Amplifiers are FIRST divided into major categories by frequency band. SECOND, within each category, parts are listed by power level. THIRD, within a frequency band, transistors are further grouped by operating voltage and, finally, output power.

Applications Assistance

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274.

Access Data On–Line!

Use the Motorola SPS Internet to access Motorola Semiconductor Product data at http://www.motorola.com/semiconductors or http://www.motorola.com/rf. The SPS Internet provides you with instant access to product summary pages, data sheets, selector guide information, application information, design tools, package outlines, on–line technical support and much more.

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RF Front End ICs

Motorola's RF Front End integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SOT–343, SOT–363, TSSOP–16, Micro–8, TSSOP–20EP, QFN–20, QFN–24, or QFN–32 packages.

Evaluation Boards

Evaluation boards are available for RF Front End Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

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RF Front End ICs

RFICs

Upconverters/Exciters

Product	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Conv. Gain dB (Typ)	Output IP3 dBm (Typ)	Packaging	System Applicability
MRFIC1813[18b]	1700 to 2000	2.7 to 4.5	25	0.1	15	11	948C/ TSSOP–16	DCS1800, PCS
MC13751FC[18b]	800 to 900 1900 to 1950	2.7 to 2.9	53	0.025	21.5 23	24	1307/ QFN–24	TDMA, PCS

Power Amplifiers

Product	Freq. Range MHz	Supply Volt. Range Vdc	Saturated P_{out} dBm (Typ)	PAE % (Typ)	Gain P_{out}/P_{in} dB (Typ)	Packaging	System Applicability
MRFIC0970[46b]	800 to 1000	2.8 to 5.5	35.2	53	30.2	1308/ QFN–20	GSM, ISM
MRFIC1870[46b]	1700 to 2000	2.8 to 5.5	33	45	28	1308/ QFN–20	DCS1800, PCS

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units:, l) T1 = 5,000 units.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

RF Building Blocks

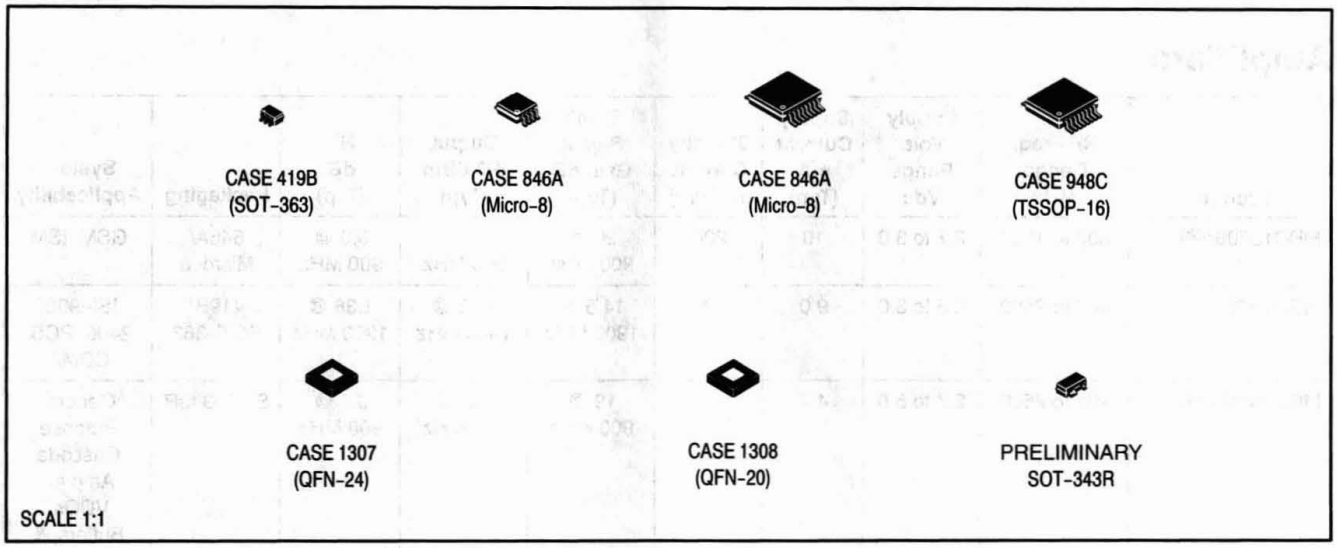
Amplifiers

Product	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Small Signal Gain dB (Typ)	Output IP3 dBm (Typ)	NF dB (Typ)	Packaging	System Applicability
MBC13706[46b]	800 to 1000	2.7 to 3.6	10	200	26 @ 900 MHz	6.0 @ 900 MHz	3.0 @ 900 MHz	846A/ Micro–8	GSM, ISM
MBC13720[18c]	400 to 2500	2.5 to 3.0	9.0	<20	14.5 @ 1900 MHz	24.5 @ 1900 MHz	1.38 @ 1900 MHz	419B/ SOT–363	ISM900, 2400, PCS, CDMA
MBC13916[18c]	100 to 2500	2.7 to 5.0	4.7	–	19 @ 900 MHz	16.5 @ 900 MHz	0.9 @ 900 MHz	SOT–343R	General Purpose Cascode Amp for VCOs, Buffers, & LNAs

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units:, l) T1 = 5,000 units.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

RF Front End Integrated Circuit Packages



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RF/IF Subsystems

Tranceivers

Product	V_{CC}	I_{CC}	GSM Receiver	TDMA/iDEN Receiver	Fractional–N PLL	Direct Launch GSM Transmitter	System Applicability	Packaging
MC13760	2.65 to 2.9 4.78 to 5.22 (Charge Pumps)	Transmit 20 mA Receive 30 mA	✓	✓	✓	✓	GSM/DCS, TDMA, iDEN, AMPS	1285/ BGA–104

Miscellaneous Functions

ADCs/DACs

Product	Function	I/O Format	Resolution	Number of Analog Channels	On–Chip Oscillator	Other Features	Suffix/ Packaging
MC144110	DAC	Serial	6 Bits	6	–	Emitter–Follower Outputs	DW/751D
MC144111				4			DW/751G

Encoders/Decoders

Product	Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Suffix/ Packaging
MC145026	Encoder	Depends on Decoder	Depends on Decoder	Depends on Decoder	Simplex	P/648, D/751B
MC145027	Decoder	5	243	4	Simplex	P/648, DW/751G
MC145028		9	19,683	0	Simplex	

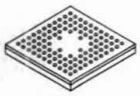
RF/IF Subsystems Packages

CASE 648
P SUFFIX
(DIP-16)

CASE 751B
D SUFFIX
(SO-16)

CASE 751D
DW SUFFIX
(SO-20L)

CASE 751G
DW SUFFIX
(SO-16W)



CASE 1285
(BGA-104)

Frequency Synthesis

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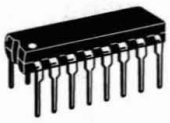
Frequency Synthesis

Single PLL Synthesizers

Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Features	Product	Suffix/ Packaging
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface	MC145151–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface, Uses External Dual–Modulus Prescaler	MC145152–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface	MC145157–2	DW/751G
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface, Uses External Dual–Modulus Prescaler	MC145158–2	DW/751G
100 @ 3.0 V 185 @ 4.5 V	2.7 to 5.5	2 @ 3 V 6 @ 5 V	Serial Interface, Auxiliary Reference Divider, Evaluation Kit – MC145170EVK	MC145170–2	P/648, D/751B, DT/948C

Frequency Synthesis Packages



CASE 648
P SUFFIX
(DIP-16)

CASE 751B
D SUFFIX
(SO-16)

CASE 751F
DW SUFFIX
(SO-28L)

CASE 751G
DW SUFFIX
(SO-16W)

CASE 948C
DT SUFFIX
(TSSOP-16)

Motorola RF Transistors

Motorola continues to be an industry leader in RF transistor technology. Our current portfolio ranges from high gain and low noise devices at microwave frequencies to high power devices for fixed RF and microwave applications. Technical innovation combined with world–class manufacturing capability allows Motorola to offer world class product, service and support to its customers.

From our LDMOS and GaAs portfolio, the user can choose from a variety of packages. They include plastic and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.

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Motorola RF Transistors

RF High Power LDMOS Transistors

Motorola LDMOS technology is ideally suited for RF power amplifier applications. Several families of products have been targeted for specific markets including VHF and UHF portable/land mobile, 900 MHz linear cellular, GSM, TDMA and CDMA, digital television, GSM EDGE, PCS, UMTS, and W–CDMA.

With the unique LDMOS characteristics, these parts offer superior thermal performance. This is due to the simplified package design, which offers excellent Class AB intermodulation performance under medium peak–to–average ratios providing a superior device choice for advanced digital modulations formats or high gain applications.

Table 1. Mobile – To 520 MHz

Designed for broadband VHF and UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 12.5/7.5 volt mobile, portable and base station operation.

Product	Frequency Band[37]		P_{out} Watts	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
VHF & UHF, Land Mobile Radio, Class AB								
MRF1511T1[18f]	U	136–175	8	7.5	11.5/175	55	2.0	466/1
MRF1517T1[18f]	U	430–520	8	7.5	11/520	55	2.0	466/1
MRF1513T1[18f]	U	400–520	3	7.5/12.5	11/520	55	4.0	466/1
MRF1518T1[18f]	U	400–520	8	12.5	11/520	55	2.0	466/1
MRF1535T1[18j]	U	400–520	35	12.5	10(Min)/520	50(Min)	0.90	1264/1
MRF1550T1[18j]	U	136–175	50	12.5	10(Min)/175	50(Min)	0.75	1264/1

Table 2. TV Broadcast – To 1.0 GHz

Product	Frequency Band[37]		P_{out} Watts	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	IMD dBc	Package/Style
470 – 1000 MHz, Class AB									
MRF373A★	U	470–860	75 CW	32	18.2/860	60	0.89	—	360B/1
MRF373AS★	U	470–860	75 CW	32	18.2/860	60	0.63	—	360C/1
MRF374A★	U	470–860	130 PEP	32	17.3/860	41	0.58	–31	375F/1
MRF372	M	470–860	180 PEP	32	17/860	36	0.5	–35	375G/1
MRF377[46b]	M	470–860	240 PEP	32	16/860	40	0.5	–30	375G/1

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

★New Product

Table 3. Cellular – To 1.0 GHz

Product	Frequency Band[37]	P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
800 – 1.0 GHz, Class AB								
MRF9002R2[18e]★	U	960	(3x) 2 PEP[41]	2–Tone	26	16/960	50	12	978/–
MRF9030MBR1[18a,46b]	U	945	30 PEP	2–Tone	26	19.2/945	41	1.08	1337/1
MRF9030MR1[18a]★	U	945	30 PEP	2–Tone	26	19.2/945	41	1.08	1265/1
MRF9030★	U	945	30 PEP	2–Tone	26	19/945	41.5	1.9	360B/1
MRF9030S★	U	945	30 PEP	2–Tone	26	19/945	41.5	1.5	360C/1
MRF9030SR1[18a]★	U	945	30 PEP	2–Tone	26	19/945	41.5	1.5	360C/1
MRF9045MBR1[18a]★	U	945	45 PEP	2–Tone	28	19/945	41	0.85	1337/1
MRF9045MR1[18a]	U	945	45 PEP	2–Tone	28	19/945	41	0.85	1265/1
MRF9045	U	945	45 PEP	2–Tone	28	18.8/945	42	1.4	360B/1
MRF9045S	U	945	45 PEP	2–Tone	28	18.8/945	42	1.0	360C/1
MRF9045SR1[18a]	U	945	45 PEP	2–Tone	28	18.8/945	42	1.0	360C/1
MRF9060MBR1[18a]★	U	945	60 PEP	2–Tone	26	18/945	40	0.56	1337/1
MRF9060MR1[18a,46b]	U	945	60 PEP	2–Tone	26	18/945	40	0.56	1265/1
MRF9060★	U	945	60 PEP	2–Tone	26	17/945	40	1.1	360B/1
MRF9060S★	U	945	60 PEP	2–Tone	26	17/945	40	0.8	360C/1
MRF9060SR1[18a]★	U	945	60 PEP	2–Tone	26	17/945	40	0.8	360C/1
MRF6522–70	M	921–960	70 CW	1–Tone	26	16/921,960	58	1.1	465D/1
MRF6522–70R3[18i]	M	921–960	70 CW	1–Tone	26	16/921,960	58	1.1	465D/1
MRF9080	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465/1
MRF9080R3[18i]	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465/1
MRF9080S	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465A/1
MRF9080SR3[18i]	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465A/1
MRF9080LSR3[18i]★	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465A/1
MRF9085	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465/1
MRF9085R3[18i]	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465/1
MRF9085S	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465A/1
MRF9085SR3[18i]	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465A/1
MRF9085LS★	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465A/1
MRF9085LSR3[18i]★	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465A/1
MRF9100[46a]	M	921–960	100 CW	1–Tone	26	17/960	51	1.0	465/1
MRF9100R3[18i,46a]	M	921–960	100 CW	1–Tone	26	17/960	51	1.0	465/1
MRF9100S[46a]	M	921–960	100 CW	1–Tone	26	17/960	51	1.0	465A/1
MRF9100SR3[18i,46a]	M	921–960	100 CW	1–Tone	26	17/960	51	1.0	465A/1
MRF9120★	M	880	120 PEP	2–Tone	26	16.5/880	39	0.45	375B/1
MRF9120S★	M	880	120 PEP	2–Tone	26	16.5/880	39	0.45	375H/1
MRF9130L[46b]	M	921–960	130 CW	1–Tone	28	16/921,960	48	0.6	465/1
MRF9130LR3[18i,46b]	M	921–960	130 CW	1–Tone	28	16/921,960	48	0.6	465/1
MRF9130LS[46b]	M	921–960	130 CW	1–Tone	28	16/921,960	48	0.6	465A/1
MRF9130LSR3[18i,46b]	M	921–960	130 CW	1–Tone	28	16/921,960	48	0.6	465A/1
MRF9135L[46a]	M	880	25 AVG	N–CDMA	26	17/880	25	0.6	465/1
MRF9135LR3[18i,46a]	M	880	25 AVG	N–CDMA	26	17/880	25	0.6	465/1
MRF9135LS[46a]	M	880	25 AVG	N–CDMA	26	17/880	25	0.6	465A/1
MRF9135LSR3[18i,46a]	M	880	25 AVG	N–CDMA	26	17/880	25	0.6	465A/1
MRF9180	M	880	170 PEP	2–Tone	26	17.5/880	39	0.45	375D/1
MRF9180S	M	880	170 PEP	2–Tone	26	17.5/880	39	0.45	375E/1
MRF9210[46b]	M	880	200 PEP	2–Tone	26	15/880	39	0.5	375G/1

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[41]Three individual transistors in a single package.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

★New Product

Table 4. PCS and 3G – To 2.1 GHz

Product	Frequency Band[37]	P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
1805 – 1990 MHz, Class AB (GSM1800, GSM1900, GSM EDGE and PCS TDMA)								
MRF18030A★	M	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465E/1
MRF18030AR3[18i]★	M	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465E/1
MRF18030AS★	M	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465F/1
MRF18030ASR3[18i]★	M	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465F/1
MRF18030B★	M	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465E/1
MRF18030BR3[18i]★	M	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465E/1
MRF18030BS★	M	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465F/1
MRF18030BSR3[18i]★	M	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465F/1
MRF18060A	M	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465/1
MRF18060AR3[18i]	M	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465/1
MRF18060AS	M	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465A/1
MRF18060ASR3[18i]	M	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465A/1
MRF18060B	M	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465/1
MRF18060BR3[18i]	M	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465/1
MRF18060BS	M	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465A/1
MRF18060BSR3[18i]	M	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465A/1
MRF18085A[46b]	M	1805–1880	85 CW	1–Tone	26	13/1805,1880	53	0.64	465/1
MRF18085AS[46b]	M	1805–1880	85 CW	1–Tone	26	13/1805,1880	53	0.64	465A/1
MRF18085B[46a]	M	1930–1990	85 CW	1–Tone	26	13/1930,1990	52	0.64	465/1
MRF18085BS[46b]	M	1930–1990	85 CW	1–Tone	26	13/1930,1990	52	0.64	465A/1
MRF18090A	M	1805–1880	90 CW	1–Tone	26	13.5/1805,1880	52	0.7	465B/1
MRF18090AS	M	1805–1880	90 CW	1–Tone	26	13.5/1805,1880	52	0.7	465C/1
MRF18090B	M	1930–1990	90 CW	1–Tone	26	13.5/1930,1990	45	0.7	465B/1
MRF18090BS	M	1930–1990	90 CW	1–Tone	26	13.5/1930,1990	45	0.7	465C/1
1.9 GHz, Class AB (2–CH N–CDMA)								
MRF19030	M	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465E/1
MRF19030R3[18i]	M	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465E/1
MRF19030S	M	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465F/1
MRF19030SR3[18i]	M	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465F/1
MRF19045★	M	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	0.65	465E/1
MRF19045R3[18i]★	M	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	0.65	465E/1
MRF19045S★	M	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	0.65	465F/1
MRF19045SR3[18i]★	M	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	0.65	465F/1
MRF19060	M	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465/1
MRF19060R3[18i]	M	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465/1
MRF19060S	M	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465A/1
MRF19060SR3[18i]	M	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465A/1
MRF19090	M	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465B/1
MRF19090S	M	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465C/1
MRF19090SR3[18i]	M	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465C/1
MRF19085	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465/1
MRF19085R3[18i]	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465/1
MRF19085S	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19085SR3[18i]	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19085LS★	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19085LSR3[18i]★	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19120[3]	M	1930–1990	120 PEP	2–Tone	26	11.7/1990	34	0.45	375D/1
MRF19120S[3]	M	1930–1990	120 PEP	2–Tone	26	11.7/1990	34	0.45	375E/1

[3]Internal Impedance Matched Push-Pull Transistors

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

★New Product

Table 4. PCS and 3G – To 2.1 GHz (continued)

Product		Frequency Band[37]	P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
1.9 GHz, Class AB (2–CH N–CDMA) (continued)									
MRF19125	M	1930–1990	24 AVG	N–CDMA	26	13.5/1990	22	0.53	465B/1
MRF19125S	M	1930–1990	24 AVG	N–CDMA	26	13.5/1990	22	0.53	465C/1
MRF19125SR3[18i]	M	1930–1990	24 AVG	N–CDMA	26	13.5/1990	22	0.53	465C/1
MRF5S19150[46c]	M	1930–1990	34 AVG	W–CDMA	28	13.6/1990	26	—	465B/1
MRF5S19150S[46c]	M	1930–1990	34 AVG	W–CDMA	28	13.6/1990	26	—	465C/1
MRF19180[46b]	M	1930–1990	40 AVG	N–CDMA	26	11.4/1990	22	0.46	375D/1
MRF19180S[46b]	M	1930–1990	40 AVG	N–CDMA	26	11.4/1990	22	0.46	375E/1
2.0 GHz, Class A, AB									
MRF281SR1[18a]	U	1930–2000	4 PEP	2–Tone	26	12.5/2000	33	5.74	458B/1
MRF281ZR1[18a]	U	1930–2000	4 PEP	2–Tone	26	12.5/2000	33	5.74	458C/1
MRF282SR1[18a]	U	1930–2000	10 PEP	2–Tone	26	11.5/2000	28(min)	4.2	458B/1
MRF282ZR1[18a]	U	1930–2000	10 PEP	2–Tone	26	11.5/2000	28(min)	4.2	458C/1
MRF284	U	1930–2000	30 PEP	2–Tone	26	10.5/2000	35	2.0	360B/1
MRF284SR1[18a]	U	1930–2000	30 PEP	2–Tone	26	10.5/2000	35	2.0	360C/1
MRF286[46a]	M	1930–2000	60 PEP	2–Tone	26	10.5/2000	32	0.73	465/1
MRF286S[46a]	M	1930–2000	60 PEP	2–Tone	26	10.5/2000	32	0.73	465A/1
2.1 GHz, Class AB (2–CH W–CDMA, UMTS)									
MRF21010	U	2110–2170	10 PEP	2–Tone	28	13.5/2170	35	5.5	360B/1
MRF21010S★	U	2110–2170	10 PEP	2–Tone	28	13.5/2170	35	5.5	360C/1
MRF21030	M	2110–2170	30 PEP	2–Tone	28	13/2170	33	2.1	465E/1
MRF21030R3[18i]	M	2110–2170	30 PEP	2–Tone	28	13/2170	33	2.1	465E/1
MRF21030S	M	2110–2170	30 PEP	2–Tone	28	13/2170	33	2.1	465F/1
MRF21030SR3[18i]	M	2110–2170	30 PEP	2–Tone	28	13/2170	33	2.1	465F/1
MRF21045	M	2110–2170	10 AVG	W–CDMA	28	15/2170	23.5	1.65	465E/1
MRF21045R3[18i]	M	2110–2170	10 AVG	W–CDMA	28	15/2170	23.5	1.65	465E/1
MRF21045S	M	2110–2170	10 AVG	W–CDMA	28	15/2170	23.5	1.65	465F/1
MRF21045SR3[18i]	M	2110–2170	10 AVG	W–CDMA	28	15/2170	23.5	1.65	465F/1
MRF21060	M	2110–2170	60 PEP	2–Tone	28	12.5/2170	34	1.02	465/1
MRF21060R3[18i]	M	2110–2170	60 PEP	2–Tone	28	12.5/2170	34	1.02	465/1
MRF21060S	M	2110–2170	60 PEP	2–Tone	28	12.5/2170	34	1.02	465/1
MRF21060SR3[18i]	M	2110–2170	60 PEP	2–Tone	28	12.5/2170	34	1.02	465A/1
MRF21085	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465/1
MRF21085LS★	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465A/1
MRF21085LSR3[18i]★	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465A/1
MRF21085S	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465A/1
MRF21085SR3[18i]	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465A/1
MRF21090	M	2110–2170	90 PEP	2–Tone	28	11.7/2170	33	0.65	465B/1
MRF21090S	M	2110–2170	90 PEP	2–Tone	28	11.7/2170	33	0.65	465C/1
MRF21120[3]	M	2110–2170	120 PEP	2–Tone	28	11.4/2170	34.5	0.45	375D/1
MRF21120S[3]	M	2110–2170	120 PEP	2–Tone	28	11.2/2170	34.5	0.45	375E/1
MRF21125	M	2110–2170	20 AVG	W–CDMA	28	13/2170	18	0.53	465B/1
MRF21125S	M	2110–2170	20 AVG	W–CDMA	28	13/2170	18	0.53	465C/1
MRF21125SR3[18i]	M	2110–2170	20 AVG	W–CDMA	28	13/2170	18	0.53	465C/1
MRF21180[3]★	M	2110–2170	38 AVG	W–CDMA	28	12.1/2170	22	0.46	375D/1
MRF21180S[3]★	M	2110–2170	38 AVG	W–CDMA	28	12.1/2170	22	0.46	375E/1

[3]Internal Impedance Matched Push-Pull Transistors

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

★New Product

Table 4. PCS and 3G – To 2.1 GHz (continued)

Product	Frequency Band[37]	P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
2.1 GHz, Class AB (2–CH W–CDMA, UMTS) (continued)								
MRF5S21090[46c]	M	2110–2170	19 AVG	W–CDMA	28	14.5/2170	26	—	465/1
MRF5S21090S[46c]	M	2110–2170	19 AVG	W–CDMA	28	14.5/2170	26	—	465A/1
MRF5S21090L[46c]	M	2110–2170	19 AVG	W–CDMA	28	14.5/2170	26	—	465/1
MRF5S21090LS[46c]	M	2110–2170	19 AVG	W–CDMA	28	14.5/2170	26	—	465A/1
MRF5S21100[46c]	M	2110–2170	23 AVG	W–CDMA	28	13.5/2170	26	—	465/1
MRF5S21100S[46c]	M	2110–2170	23 AVG	W–CDMA	28	13.5/2170	26	—	465A/1
MRF5S21100L[46c]	M	2110–2170	23 AVG	W–CDMA	28	13.5/2170	26	—	465/1
MRF5S21100LS[46c]	M	2110–2170	23 AVG	W–CDMA	28	13.5/2170	26	—	465A/1
MRF5S21150[46c]	M	2110–2170	35 AVG	W–CDMA	28	13/2170	26	—	465B/1
MRF5S21150S[46c]	M	2110–2170	35 AVG	W–CDMA	28	13/2170	26	—	465C/1
MRF5P21180[46c]	M	2110–2170	38 AVG	W–CDMA	28	13.5/2170	25	—	375D/1
MRF5P21180S[46c]	M	2110–2170	38 AVG	W–CDMA	28	13.5/2170	25	—	375E/1
MRF5P21240[46c]	M	2110–2170	55 AVG	W–CDMA	28	13/2170	25	—	375D/1
MRF5P21240S[46c]	M	2110–2170	55 AVG	W–CDMA	28	13/2170	25	—	375E/1

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

RF Power GaAs Transistors

Motorola power GaAs transistors are made using an InGaAs PHEMT epitaxial structure for superior RF efficiency and linearity. The FETs listed in this section are designed for operation in base station infrastructure RF power amplifiers and are grouped according to frequency range and type of application. Parts are listed first by order of operating voltage, then by increasing output power.

Table 1. 3.5 GHz – Linear Transistors

Product	Frequency Band[37]	P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/GHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
3.5 GHz, Class AB (WLL, BWA, W–CDMA)								
MRFG35010★	U	3.5 G	1 AVG	W–CDMA	12	10/3.5	26	5.8	360D/1
MRFG35030[9]	M	3.5 G	4 AVG	W–CDMA	12	10/3.5	26	—	—

[9]In development.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

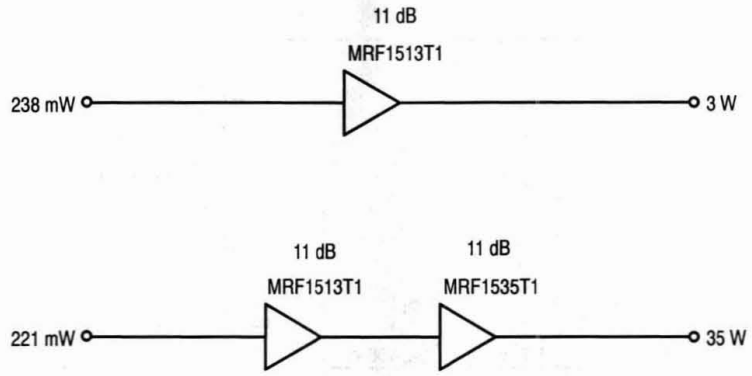
★New Product

RF Low Power Transistors

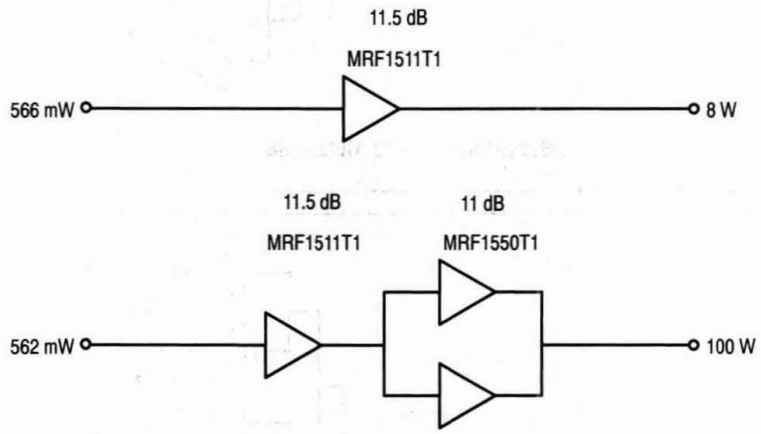
Product	Gain – Bandwidth		NFmin @ f		Gain @ f		Maximum Ratings		Packaging
	f_τ Typ GHz	I_C mA	Typ dB	GHz	Typ dB	GHz	V(BR) CEO Volts	I_C mA	
MBC13900[46b]	15	20	1.0	1.0	17	1.0	7.0	20	318M/ SOT–343
			1.3	2.0	14	2.0			

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

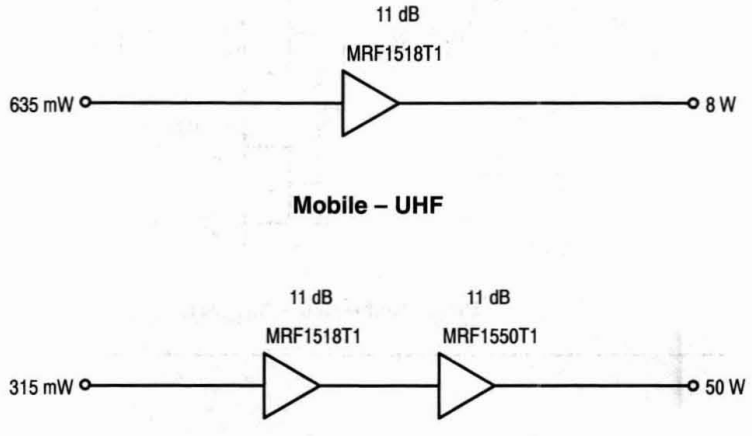
RF High Power Amplifier LDMOS Line–ups



Mobile – UHF



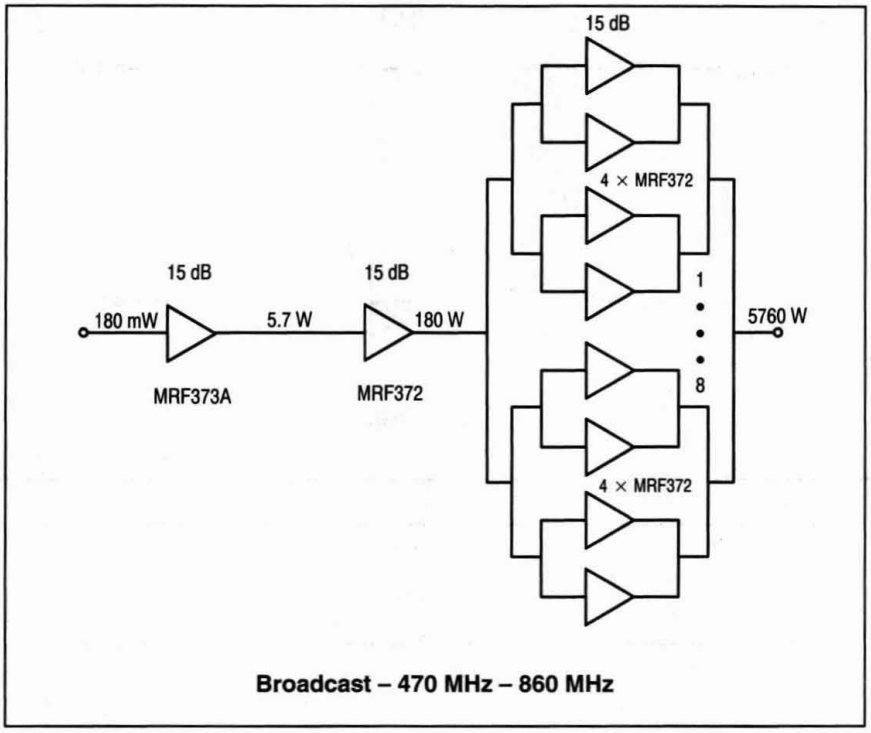
Mobile – VHF



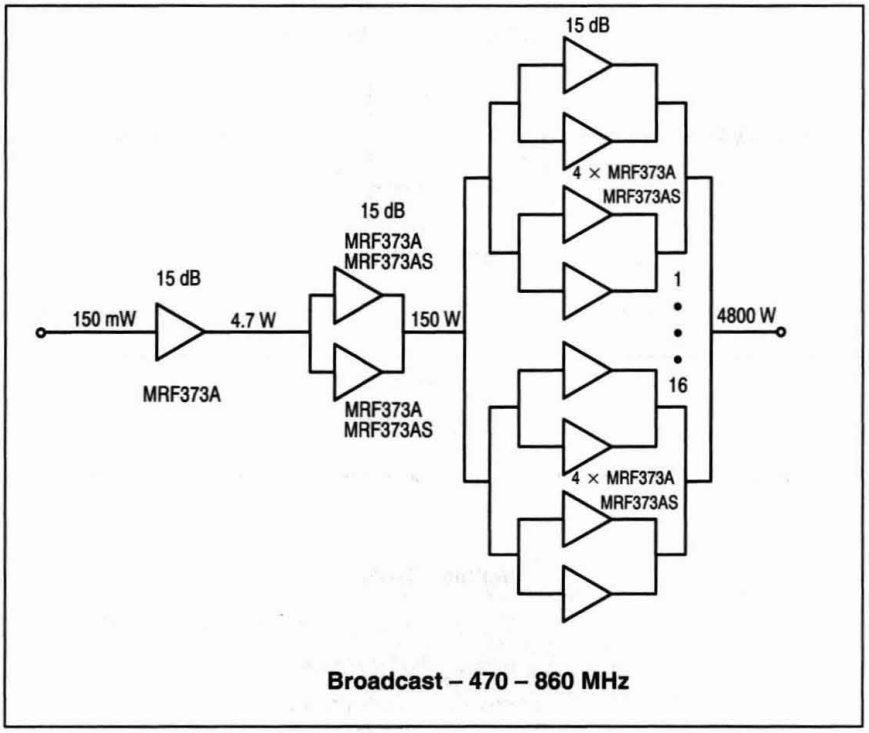
Mobile – UHF

Mobile – VHF

RF High Power Amplifier LDMOS Line–ups (continued)

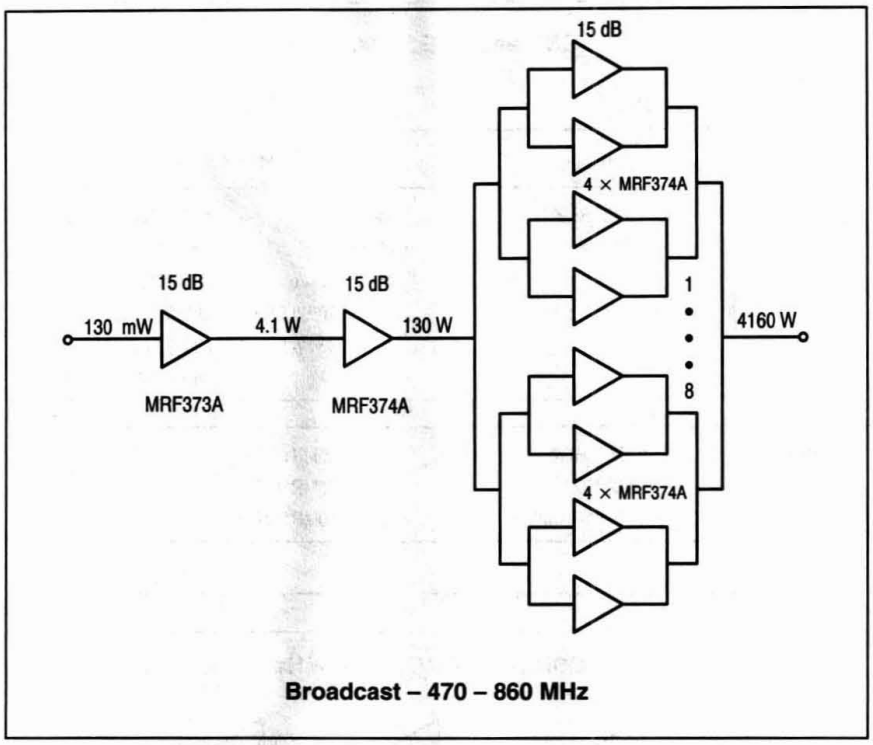


Broadcast – 470 MHz – 860 MHz



Broadcast – 470 – 860 MHz

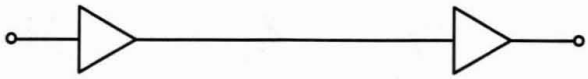
RF High Power Amplifier LDMOS Line–ups (continued)



Broadcast – 470 – 860 MHz

RF High Power Amplifier LDMOS Line–ups (continued)

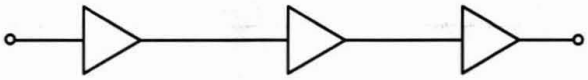
GSM and EDGE – 900 MHz



Ceramic	MRF282SR1/ZR1	MRF9045/S	MRF9100/S
	MRF9030/S	MRF9060/S	MRF9120/S
		MRF6522–70	MRF9130L/LS
		MRF9080/S/LSR3	MRF9135L/LS
		MRF9085/S/LS	MRF9180/S
			MRF9210

Plastic	MHVIC910HR2	MRF9030MR1/MBR1
	MRF9002R2	MRF9045MR1/MBR1
	MRF9030MR1/MBR1	MRF9060MR1/MBR1

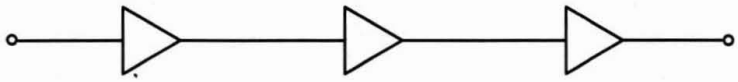
GSM and EDGE – 1800 MHz



Ceramic	MRF281SR1/ZR1	MRF18030A/S	MRF18060A/S
	MRF282SR1/ZR1	MRF284/SR1	MRF18085A/S
			MRF18090A/S

Hybrid	MHW1810–1
	MHW1810–2

GSM and EDGE – 1900 MHz

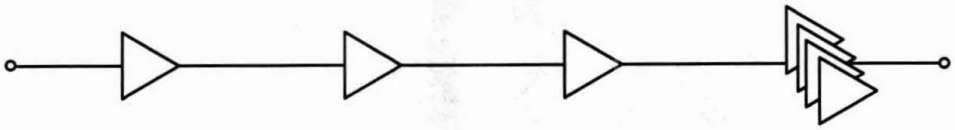


Ceramic	MRF281SR1/ZR1	MRF18030B/S	MRF18060B/S
	MRF282SR1/ZR1	MRF284/SR1	MRF18085B/S
			MRF18090B/S

Hybrid	MHW1910–1

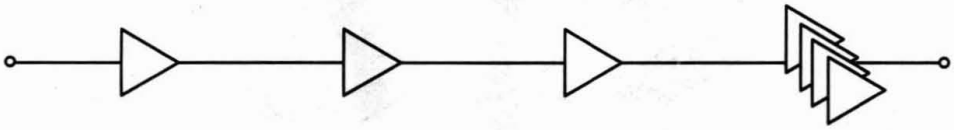
RF High Power Amplifier LDMOS Line–ups (continued)

N–CDMA – 1900 MHz



Ceramic	MRF21010/S	MRF19030/S MRF19045/S	MRF19060/S MRF19085/S/LS MRF19090/S MRF5S19090/S	MRF19120/S MRF19125/S MRF19180/S MRF5S19150/S
Hybrid	MHL19338 MHL19936	MHPA19010		

W–CDMA – 2200 MHz



Ceramic	MRF21010/S	MRF21030/S MRF21045/S	MRF21060/S MRF21085/S/LS MRF21090/S	MRF21120/S MRF21125/S MRF21180/S	MRF5S21090/S/L/LS MRF5S21100/S/L/LS MRF5S21150/S MRF5P21180/S MRF5P21240/S
Hybrid	MHL21336	MHPA21010			

RF Transistor Packages

CASE 318M
(SOT-343)

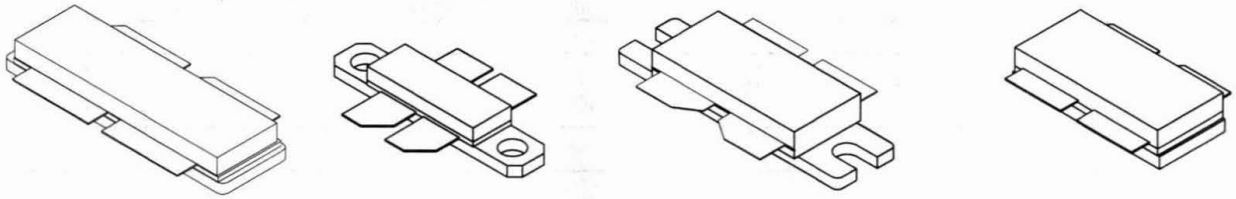
CASE 360B
STYLE 1
(NI-360)

CASE 360C
STYLE 1
(NI-360S)

CASE 360D
STYLE 1
(NI-360HF)

CASE 375B
STYLE 1
(NI-860)

CASE 375D
STYLE 1
(NI-1230)

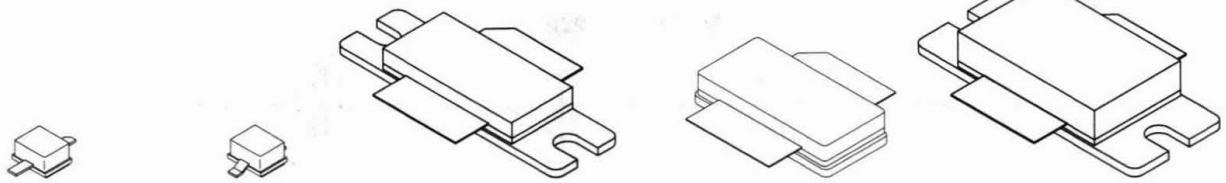


CASE 375E
STYLE 1
(NI-1230S)

CASE 375F
STYLE 1
(NI-650)

CASE 375G
STYLE 1
(NI-860C3)

CASE 375H
STYLE 1
(NI-860S)



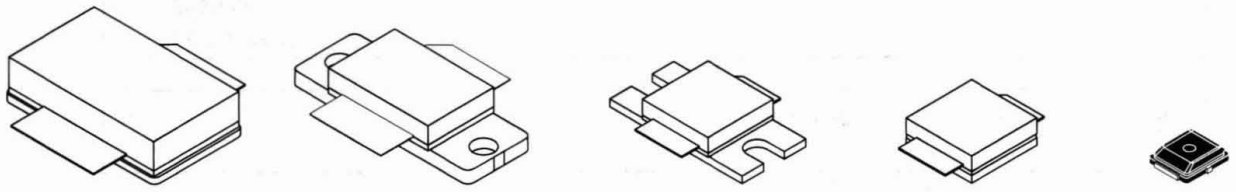
CASE 458B
STYLE 1
(NI-200S)

CASE 458C
STYLE 1
(NI-200Z)

CASE 465
STYLE 1
(NI-780)

CASE 465A
STYLE 1
(NI-780S)

CASE 465B
STYLE 1
(NI-880)



CASE 465C
STYLE 1
(NI-880S)

CASE 465D
STYLE 1
(NI-600)

CASE 465E
STYLE 1
(NI-400)

CASE 465F
STYLE 1
(NI-400S)

CASE 466
STYLE 1
PLASTIC
(PLD 1.5)

CASE 978
PLASTIC
(PFP-16)

CASE 1264
STYLE 1
PLASTIC
(TO-272)

CASE 1265
STYLE 1
PLASTIC
(TO-270)

CASE 1337
STYLE 1
PLASTIC
(TO-272 Dual Lead)

SCALE 1:1

Motorola RF Amplifier Modules/ICs

Motorola's RF portfolio includes many hybrid designs optimized to perform in narrowband base station transmitter applications. Motorola modules feature two or more active transistors (LDMOS or GaAs die technology) and their associated 50 ohm matching networks. Circuit substrate and metallization have been selected for optimum performance and reliability. For PA designers, hybrid modules offer the benefits of small and less complex system designs, in less time and at a lower overall cost.

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Packages	1.1–29

Motorola RF Amplifier Modules/ICs

Complete amplifiers with 50 ohm input impedances are available for all popular base station transmitter systems, including GSM and CDMA, covering frequencies from 800 MHz up to 2.2 GHz.

Base Stations

Designed for applications such as macrocell drivers and microcell output stage, these class AB amplifiers are ideal for base station systems with power requirements up to 10 watts.

Table 1. Base Station Drivers

Product	Frequency MHz	P1dB Watts	Gain (Min) dB	Supply Voltage Volts	Class	System Application	Die Technology	Package/Style
MHVIC910HR2[18e]★	921–960	10	38	26	AB	GSM900	LDMOS–IC	978/–
MHW1810–1	1805–1880	10	24	26	AB	GSM1800	LDMOS	301AW/1
MHW1810–2	1805–1880	10	32	26	AB	GSM1800	LDMOS	301AW/1
MHW1910–1	1930–1990	10	24	26	AB	GSM1900	LDMOS	301AW/1
MHPA19010[46a]	1930–1990	10	24	28	AB	PCS1900	LDMOS	301AP/3
MHPA21010[46b]	2110–2170	10	24	28	AB	W–CDMA	LDMOS	301AP/3

Table 2. Base Station Pre–Drivers

These 50 ohm amplifiers are recommended for modern multi–tone CDMA, TDMA and UMTS base station pre–driver applications. Their high third–order intercept point, tight phase and gain control, and excellent group delay characteristics make these devices ideal for use in high–power feedforward loops.

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A (LDMOS Die) – Lateral MOSFETs

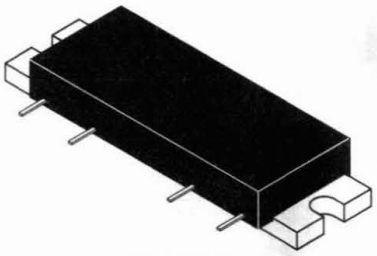
Product	Frequency Band MHz	V_{DD} (Nom.) Volts	I_{DD} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Pkg/ Style
MHL9838	800–925	28	770	31	.1	39	50	3.7	301AP/1
MHL9236	800–960	26	550	30.5	.1	34	47	3.5	301AP/1
MHL9236M	800–960	26	550	30.5	.1	34	47	3.5	301AP/2
MHL9318	860–900	28	500	17.5	.1	35.5	49	3.0	301AS/1
MHL18336★	1800–1900	26	500	30	.2	36	46	4.2	301AP/1
MHL18926★	1805–1880	26	1100	28.6	.3	40	50	4.2	301AY/1
MHL19338	1900–2000	28	500	30	.1	36	46	4.2	301AP/1
MHL19926★	1930–1990	26	1000	29.4	.3	40	50	4.2	301AY/1
MHL19936	1900–2000	26	1400	29	.2	41	49.5	4.2	301AY/1
MHL21336	2110–2170	26	500	31	.15	35	45	4.5	301AP/1

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

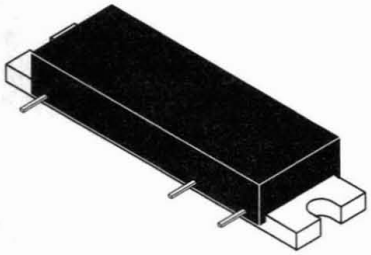
[46]To be introduced: a) 1Q02; b) 2Q02

★New Product

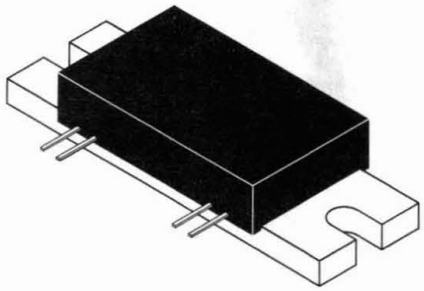
RF Amplifier Modules Packages



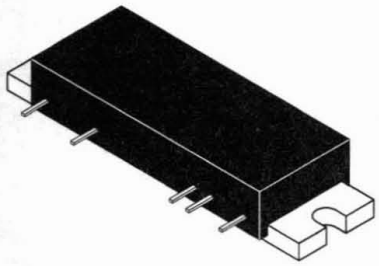
CASE 301AP
STYLE 1, 2, 3



CASE 301AS
STYLE 1



CASE 301AW
STYLE 1



CASE 301AY
STYLE 1

CASE 978
PLASTIC
(PFP-16)

SCALE 1:1

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest CATV generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels. Additions to our CATV product family include 40–870 MHz high output gallium arsenide (GaAs) power doublers as well as low distortion, low power consumption reverse amplifiers.

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Packages	1.1–36

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Forward Amplifiers

40–1000 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 152 CH	Cross Modulation dB 152 CH	Noise Figure @ 1000 MHz dB Max	Package/ Style
MHW9182B	18.5	152	+38	–63[40]	–61	–61	7.5	714Y/1
MHW9242A	24	152	+38	–61[40]	–58	–59	8.0	714Y/1

40–870 MHz High Output Gallium Arsenide Power Doubler

Product	Hybrid Gain (Nom.) @ 870 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 132 CH	Cross Modulation dB 132 CH	Noise Figure @ 870 MHz dB Max	Package/ Style
MHW9187★	20	132	+48	–62[34]	–56	–55	4.5	1302/1
MHW9227[9]	22	132	+48	–58[34]	–54	–54	6.0	1302/1
MHW9247[46b]	24	132	+48	–59[34]	–55	–54	5.5	1302/1
MHW9267[9]	26	132	+48	–60[34]	–56	–54	5.5	1302/1

40–870 MHz Gallium Arsenide Preamplifiers

Product	Hybrid Gain (Nom.) @ 870 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 132 CH	Cross Modulation dB 132 CH	Noise Figure @ 870 MHz dB Max	Package/ Style
MHW9146[9]	14	132	+44	–64[36]	–56	–55	5.5	1302/1
MHW9186[46a]	18.5	128	+44	–62[36]	–58	–52	5.0	1302/1
MHW9206[46b]	20	132	+44	–64[36]	–55	–55	4.5	1302/1
MHW9236[46b]	23	132	+44	–60[36]	–54	–53	5.5	1302/1
MHW9256[9]	25	132	+44	–60[36]	–55	–53	5.0	1302/1
MHW9276[9]	27	132	+44	–60[36]	–56	–53	5.0	1302/1

[9]In development.

[34]Composite 2nd Order; V_{out} = +48 dBmV/ch

[36]Composite 2nd order; V_{out} = +44 dBmV/ch

[40]Composite 2nd Order; V_{out} = +38 dBmV/ch

[46]To be introduced: a) 1Q02; b) 2Q02

★New Product

CATV Distribution: Forward Amplifiers (continued)

40–870 MHz Preamplifiers

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation dB 128 CH	Noise Figure @ 870 MHz dB Max	Package/ Style
MHW8202B[46a]	20.4	128	+38	–67[40]	–64	–64	7.0	1302/1

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55 MHz dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
MHW8182B	18.5	128	+38	–64[40]	–66	–65	7.5	714Y/1
MHW8222B	21.9	128	+38	–60[40]	–64	–63	7.0	1302/1
MHW8242A	24	128	+38	–62[40]	–64	–62	7.5	714Y/1
MHW8272A	27.2	128	+38	–64[40]	–64	–62	7.0	714Y/1
Power Doubling Hybrids								
MHW8185L[21]	18.5	128	+40	–62[39]	–63	–64	8.5*	714Y/1
MHW8185	18.8	128	+40	–62[39]	–64	–64	8.0	714Y/1
MHW8205L[22]	19.5	128	+40	–60[39]	–63	–64	8.5*	714Y/1
MHW8205	19.8	128	+40	–60[39]	–63	–64	8.0	714Y/1

*@ 870 MHz

40–750 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Cross Modulation FM = 55 MHz dB 110 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
MHW7182B	18.5	110	+40	–63[39]	–66	–64	6.5	714Y/1
MHW7222B	21.9	110	+40	–60[39]	–61	–60	6.5	1302/1
MHW7242A	24	110	+40	–62[39]	–63	–61	7.0	714Y/1
MHW7272A	27.2	110	+40	–64[39]	–64	–60	6.5	714Y/1
Power Doubling Hybrids								
MHW7185C	18.8	110	+44	–64[36]	–62	–63	7.5	714Y/1
MHW7205C	19.8	110	+44	–63[36]	–61	–62	7.5	714Y/1

[21]Low DC Current Version of MHW8185; Typical I_{CC} @ Vdc = 24 V is 365 mA.
[22]Low DC Current Version of MHW8205; Typical I_{CC} @ Vdc = 24 V is 365 mA.
[36]Composite 2nd order; V_{out} = +44 dBmV/ch
[39]Composite 2nd order; V_{out} = +40 dBmV/ch
[40]Composite 2nd Order; V_{out} = +38 dBmV/ch
[46]To be introduced: a) 1Q02; b) 2Q02

CATV Distribution: Forward Amplifiers (continued)

40–550 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 77 CH	Cross Modulation dB 77 CH	Noise Figure @ 550 MHz dB Max	Package/ Style
MHW6342T	34.5	77	+44	–64(35)	–57	–57	6.5	1302/1

Reverse Amplifiers

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB 22 CH	Composite Triple Beat dB 26 CH	Cross Modulation dB 22 CH	Cross Modulation dB 26 CH	Noise Figure @ 175 MHz dB Max	Package/ Style
MHW1244	24	22	+50	–72	–68	–67.5(19)	–61	–61(19)	5.0	714Y/1

Low Current Amplifiers — 5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB 6 CH	2nd Order Test dB 10 CH	Composite Triple Beat dB 6 CH	Composite Triple Beat dB 10 CH	Cross Modulation dB 6 CH	Cross Modulation dB 10 CH	DC Current mA Typ.	Noise Figure @ 200 MHz dB Max	Pkg/ Style
MHW1223LA	22.7	6,10	50	–68	–65	–75	–66	–65	–60	95	7.0	1302/1
MHW1253LA	25.5	6,10	50	–68	–66	–75	–66	–65	–61	95	6.5	1302/1
MHW1303LA	30.8	6,10	50	–68	–65	–74	–64	–64	–58	95	5.7	1302/1

Low Current Amplifiers — 5–150 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB 6 CH	2nd Order Test dB 10 CH	Composite Triple Beat dB 6 CH	Composite Triple Beat dB 10 CH	Cross Modulation dB 6 CH	Cross Modulation dB 10 CH	DC Current mA Typ.	Noise Figure @ 150 MHz dB Max	Pkg/ Style
MHW1353LA	35.2	6,10	50	–68	–65	–73	–62	–63	–57	95	5.4	1302/1

(19)Typical

(30)Channels 2 and A @ 7

(35)Channels 2 and M30 @ M39

CATV Distribution: Reverse Amplifiers (continued)

Low Current Amplifiers — 5–65 MHz Hybrids, V_{CC} = 24 Vdc, Class A

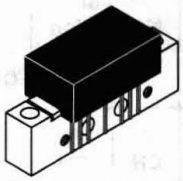
Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB: 6 CH	2nd Order Test dB: 10 CH	Composite Triple Beat dB: 6 CH	Composite Triple Beat dB: 10 CH	Cross Modulation dB: 6 CH	Cross Modulation dB: 10 CH	DC Current mA Typ.	Noise Figure @ 65 MHz dB Max	Pkg/ Style
MHW1224LA	22.7	6,10	50	–68	–65	–75	–66	–65	–60	95	7.0	1302/1
MHW1254LA	25.5	6,10	50	–68	–66	–75	–66	–65	–61	95	6.5	1302/1
MHW1304LA	30.8	6,10	50	–68	–65	–74	–64	–64	–58	95	5.7	1302/1
MHW1354LA	35.2	6,10	50	–68	–65	–73	–62	–63	–57	95	5.4	1302/1

Low Current Amplifiers — 5–50 MHz Hybrids, V_{CC} = 24 Vdc, Class A

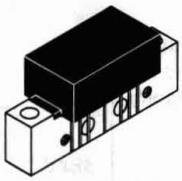
Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	I_{DC} mA Max	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test[30] dB	Composite Triple Beat dB: 4 CH	Cross Modulation dB: 4 CH	Noise Figure @ 50 MHz dB Max	Package/ Style
MHW1254L	25	4	135	+50	–70	–70	–62	4.5	714Y/1

[30]Channels 2 and A @ 7

RF CATV Distribution Amplifiers Packages



CASE 714Y
STYLE 1, 2



CASE 1302
STYLE 1

SCALE 1:2

Chapter Two
RF Front End ICs

Section One **2.1–0**
RF Front End ICs – Selector Guide

Section Two **2.2–0**
RF Front End ICs – Data Sheets

Section One
Selector Guide

RF Front End ICs

Motorola's RF Front End integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SOT–343, SOT–363, TSSOP–16, Micro–8, TSSOP–20EP, QFN–20, QFN–24, or QFN–32 packages.

Evaluation Boards

Evaluation boards are available for RF Front End Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

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Power Amplifiers	2.1–2
RF Building Blocks	2.1–3
Amplifiers	2.1–3
Packages	2.1–4

RF Front End ICs

RFICs

Upconverters/Exciters

Product	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Conv. Gain dB (Typ)	Output IP3 dBm (Typ)	Packaging	System Applicability
MRFIC1813[18b]	1700 to 2000	2.7 to 4.5	25	0.1	15	11	948C/ TSSOP–16	DCS1800, PCS
MC13751FC[18b]	800 to 900 1900 to 1950	2.7 to 2.9	53	0.025	21.5 23	24	1307/ QFN–24	TDMA, PCS

Power Amplifiers

Product	Freq. Range MHz	Supply Volt. Range Vdc	Saturated P_{out} dBm (Typ)	PAE % (Typ)	Gain P_{out}/P_{in} dB (Typ)	Packaging	System Applicability
MRFIC0970[46b]	800 to 1000	2.8 to 5.5	35.2	53	30.2	1308/ QFN–20	GSM, ISM
MRFIC1870[46b]	1700 to 2000	2.8 to 5.5	33	45	28	1308/ QFN–20	DCS1800, PCS

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units:, l) T1 = 5,000 units.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

RF Building Blocks

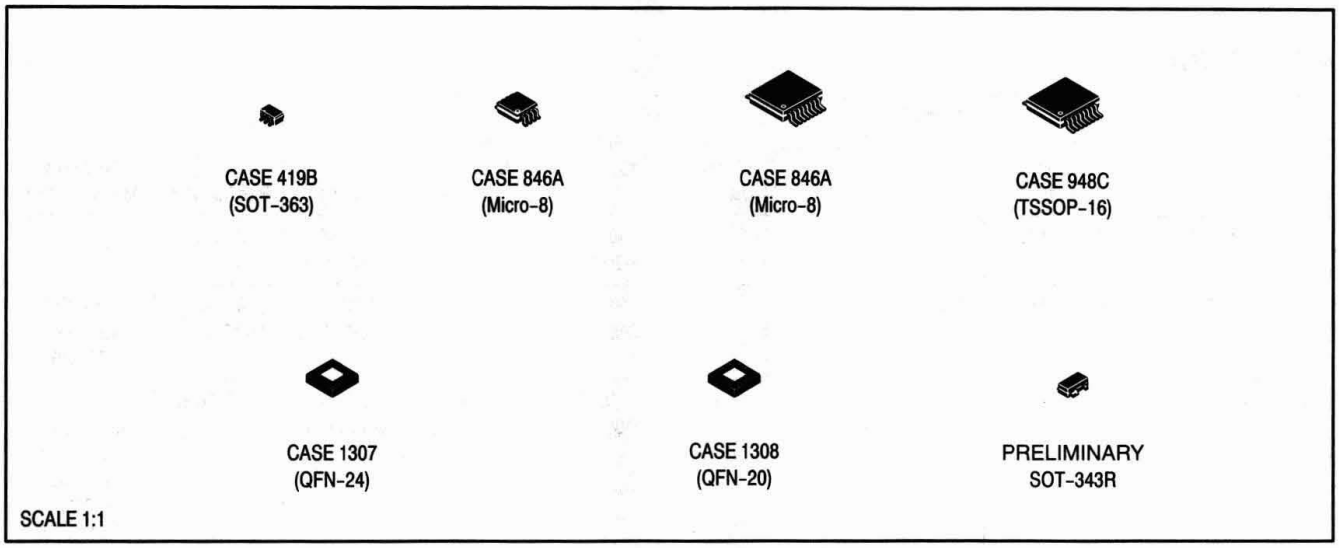
Amplifiers

Product	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Small Signal Gain dB (Typ)	Output IP3 dBm (Typ)	NF dB (Typ)	Packaging	System Applicability
MBC13706[46b]	800 to 1000	2.7 to 3.6	10	200	26 @ 900 MHz	6.0 @ 900 MHz	3.0 @ 900 MHz	846A/ Micro–8	GSM, ISM
MBC13720[18c]	400 to 2500	2.5 to 3.0	9.0	<20	14.5 @ 1900 MHz	24.5 @ 1900 MHz	1.38 @ 1900 MHz	419B/ SOT–363	ISM900, 2400, PCS, CDMA
MBC13916[18c]	100 to 2500	2.7 to 5.0	4.7	–	19 @ 900 MHz	16.5 @ 900 MHz	0.9 @ 900 MHz	SOT–343R	General Purpose Cascode Amp for VCOs, Buffers, & LNAs

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units:, l) T1 = 5,000 units.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

RF Front End Integrated Circuit Packages



Section Two

RF Front End ICs – Data Sheets

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Amplifiers	
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MBC13720	2.2–4
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MOTOROLA
intelligence everywhere

digital dna

MBC13706

Product Preview

The RF Building Block Series

GSM Low Noise Amplifier with Gain Control

Designed primarily for use in GSM wireless communication systems. The MBC13706 is a silicon low noise amplifier with three available gain settings. Two gain control pins control the gain settings. The LNA can be turned off during transmit mode to save current by disabling the RX Enable pin. The LNA is packaged in a low–cost Micro–8 package.

- Usable Frequency Range: 925 to 960 MHz
- Three Gain States: 26, 18, and 0 dB
- 3.0 dB Max Noise @ Max Gain
- High Reverse Isolation: > 40 dB @ 945 MHz
- Low Power Consumption = 30 mW @ Max Gain, 3.0 V
- Low Standby Current = 200 µA (Typ)
- Low Cost Surface Mount Plastic Package

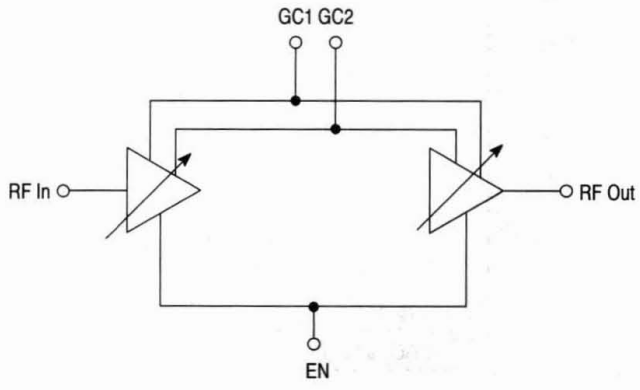
GSM LNA
WITH GAIN CONTROL

SEMICONDUCTOR
TECHNICAL DATA

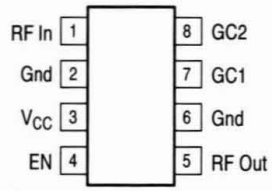
(Scale 2:1)

PLASTIC PACKAGE
CASE 846A
(Micro–8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MBC13706	T_A = –30 to 70°C	Micro–8

MOTOROLA
intelligence everywhere™

digital dna™

MBC13720

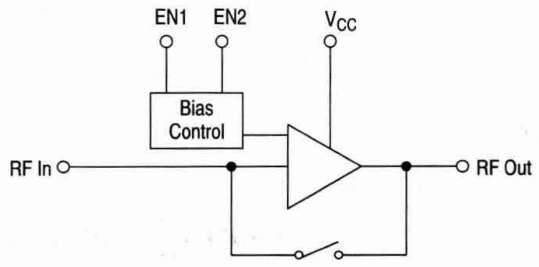
The RF Building Block Series

SiGe:C Low Noise Amplifier with Bypass Switch

The MBC13720 is a high IP3, low noise amplifier designed for 400 MHz to 2.4 GHz multistandard wireless applications. The input and output match is external to allow maximum design flexibility. The LNA has two selectable current settings as well as standby mode. The LNA will operate from a 2.5 to 3.0 V supply. The MBC13720 is fabricated using Motorola's Advanced RF BiCMOS process with the SiGe:C option and housed in an ultra small SOT–363 surface mount package.

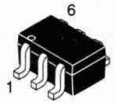
- Selectable Current, 5.0 mA or 11 mA
- Standby Mode to Turn Off Device Completely
- High Input IP3:
  - 10 dBm @ 1.9 GHz
  - 13 dBm @ 2.4 GHz
- Low Noise Figure:
  - 1.38 dB @ 1.9 GHz
  - 1.55 dB @ 2.4 GHz
- Gain @ 9.0 mA, 2.75 V:
  - 14.5 dB @ 1.9 GHz
  - 12 dB @ 2.4 GHz
- Suitable for use from 400 MHz to 2.4 GHz
- Bias Stabilized for Device and Temperature Variations
- Ultra Small SOT–363 Surface Mount Package
- Available Only in Tape and Reel Packaging

Simplified Block Diagram



SiGe:C LNA WITH BYPASS SWITCH

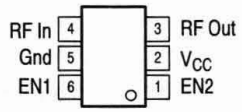
SEMICONDUCTOR TECHNICAL DATA



(Scale 4:1)

PLASTIC PACKAGE
CASE 419B
(SOT–363)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Device Marking	Package
MBC13720T1	20	SOT–363

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	3.3	V
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Ambient Temperature Range	T_A	–30 to 85	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤550 V and Machine Model (MM) ≤50 V. Additional EST data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{CC}	2.5	2.7	3.0	V
Frequency Range	f_{RF}	400	–	2400	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.75 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Consumption	I_{CC}				
Low IP3		–	5.0	–	mA
High IP3		–	11	–	mA
Bypass		–	0	–	µA
Input/Output Return Loss	RL				dB
Low IP3		–	10	–	
High IP3		–	10	–	
Bypass		–	12	–	
RF Gain (900 MHz)	G				dB
Low IP3		–	20	–	
High IP3		–	21	–	
Bypass		–	–2.9	–	
RF Gain (1.9 GHz)	G				dB
Low IP3		–	13	–	
High IP3		–	14.5	–	
Bypass		–	–2.5	–	
RF Gain (2.4 GHz)	G				dB
Low IP3		–	11.5	–	
High IP3		–	12	–	
Bypass		–	–2.8	–	
Noise Figure	NF				dB
900 MHz		–	1.2	–	
1.9 GHz		–	1.38	–	
2.4 GHz		–	1.55	–	
Input IP3 (900 MHz)	IIP3				dBm
Low IP3		–	–3.5	–	
High IP3		–	10	–	
Bypass		–	27	–	
Input IP3 (1.9 GHz)	IIP3				dBm
Low IP3		–	4.0	–	
High IP3		–	10	–	
Bypass		–	29	–	
Input IP3 (2.4 GHz)	IIP3				dBm
Low IP3		–	6.0	–	
High IP3		–	13	–	
Bypass		–	25	–	

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.75 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output 1dB Compression (900 MHz)	P_{1dB}				dBm
Low IP3		–	12	–	
High IP3		–	11.5	–	
Bypass		–	5.0	–	
Output 1db Compression (1.9 GHz)	P_{1dB}				dBm
Low IP3		–	11	–	
High IP3		–	11.5	–	
Bypass		–	5.0	–	
Output 1dB Compression (2.4 GHz)	P_{1dB}				dBm
Low IP3		–	14	–	
High IP3		–	14	–	
Bypass		–	5.0	–	
Reverse Isolation	$\lvert S_{12} \rvert$				dB
Low IP3		–	25	–	
High IP3		–	20	–	

Table 1. Truth Table

EN1	EN2	State	Current Consumption
0	0	Standby	< 20 μA
0	1	Bypass	0 μA
1	0	High IP3	11 mA (approx.)
1	1	Low IP3	5.0 mA (approx.)

NOTE: Logic state of "1" equals V_{CC} voltage. Logic state of "0" equals ground potential.

Table 2. Low IP3 Mode Scattering Parameters
(V_{CC} = 2.7 V, EN1 = High, EN2= High)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.811	–7	11.939	168	0.010	39	0.890	–5
200	0.787	–14	11.375	157	0.015	55	0.875	–9
300	0.756	–20	10.789	148	0.021	61	0.853	–12
400	0.706	–24	9.892	138	0.026	65	0.819	–15
500	0.673	–28	8.949	131	0.031	68	0.796	–17
600	0.636	–31	8.293	125	0.036	69	0.772	–19
700	0.602	–34	7.590	119	0.040	70	0.750	–21
800	0.575	–36	6.987	114	0.045	72	0.732	–22
900	0.553	–38	6.457	109	0.050	73	0.716	–24
1000	0.531	–39	5.972	105	0.055	74	0.702	–25
1100	0.514	–40	5.566	101	0.060	75	0.690	–26
1200	0.500	–42	5.218	98	0.065	76	0.680	–27
1300	0.488	–43	4.884	95	0.070	77	0.671	–28
1400	0.477	–44	4.629	92	0.075	77	0.664	–29
1500	0.469	–45	4.373	89	0.081	78	0.657	–30
1600	0.458	–46	4.136	87	0.087	79	0.651	–31
1700	0.455	–47	3.938	84	0.093	79	0.645	–32
1800	0.450	–48	3.762	82	0.099	80	0.641	–33
1900	0.445	–49	3.614	80	0.105	80	0.636	–34
2000	0.442	–50	3.479	78	0.112	81	0.631	–35
2100	0.440	–51	3.352	76	0.119	81	0.625	–37
2200	0.438	–52	3.223	74	0.126	82	0.621	–38
2300	0.440	–53	3.127	72	0.135	82	0.619	–39
2400	0.440	–55	3.044	70	0.144	82	0.615	–41
2500	0.443	–57	2.966	68	0.154	82	0.610	–43
2600	0.446	–59	2.886	66	0.165	83	0.603	–45
2800	0.447	–64	2.778	62	0.189	83	0.589	–50
3000	0.458	–71	2.691	58	0.221	82	0.570	–56

Table 3. High IP3 Mode Scattering Parameters
(V_{CC} = 2.7 V, EN1 = High, EN2= Low)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.661	–8	21.189	161	0.010	36	0.829	–6
200	0.629	–14	18.913	146	0.014	54	0.801	–10
300	0.583	–20	16.730	134	0.019	61	0.764	–14
400	0.544	–21	14.168	123	0.024	67	0.726	–15
500	0.526	–23	12.141	116	0.029	71	0.709	–16
600	0.502	–25	10.757	111	0.034	73	0.690	–17
700	0.486	–26	9.523	106	0.039	75	0.676	–18
800	0.473	–27	8.531	101	0.044	76	0.665	–19
900	0.464	–28	7.725	98	0.050	77	0.656	–20
1000	0.457	–29	7.028	94	0.056	78	0.650	–21
1100	0.450	–30	6.461	92	0.061	79	0.643	–22
1200	0.446	–31	5.990	89	0.067	79	0.639	–23
1300	0.445	–32	5.551	86	0.073	80	0.634	–24
1400	0.443	–33	5.226	84	0.079	80	0.632	–25
1500	0.440	–35	4.903	82	0.085	80	0.628	–26
1600	0.437	–35	4.611	80	0.091	80	0.626	–27
1700	0.439	–37	4.370	78	0.097	80	0.623	–28
1800	0.439	–38	4.160	76	0.103	81	0.622	–29
1900	0.437	–40	3.981	74	0.111	81	0.618	–31
2000	0.440	–41	3.822	73	0.117	81	0.617	–32
2100	0.439	–42	3.675	71	0.124	81	0.613	–34
2200	0.443	–44	3.530	69	0.132	81	0.612	–35
2300	0.444	–45	3.416	68	0.140	82	0.611	–37
2400	0.448	–48	3.322	66	0.149	82	0.608	–38
2500	0.452	–50	3.236	64	0.159	81	0.605	–41
2600	0.456	–52	3.151	63	0.169	82	0.600	–43
2800	0.460	–57	3.032	59	0.193	81	0.589	–48
3000	0.472	–65	2.943	55	0.223	80	0.573	–54

Table 4. Bypass Mode Scattering Parameters
(V_{CC} = 2.7 V, EN1 = Low, EN2= High)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.958	–11	0.115	79	0.116	80	0.950	–8
200	0.921	–21	0.222	70	0.224	70	0.925	–16
300	0.881	–30	0.318	61	0.319	61	0.889	–23
400	0.832	–38	0.399	53	0.396	53	0.849	–29
500	0.786	–45	0.457	45	0.462	46	0.806	–35
600	0.737	–52	0.515	39	0.513	39	0.764	–41
700	0.693	–57	0.552	33	0.553	33	0.724	–45
800	0.654	–63	0.585	28	0.584	28	0.689	–49
900	0.618	–67	0.610	23	0.609	23	0.655	–53
1000	0.587	–72	0.626	19	0.627	19	0.626	–57
1100	0.561	–76	0.642	16	0.643	15	0.598	–61
1200	0.533	–80	0.655	12	0.654	12	0.573	–64
1300	0.514	–83	0.660	9.0	0.663	8	0.549	–67
1400	0.493	–87	0.673	6.0	0.669	5	0.527	–71
1500	0.478	–90	0.672	2.0	0.673	2	0.506	–74
1600	0.461	–93	0.674	–1.0	0.676	–1	0.486	–78
1700	0.449	–96	0.675	–4.0	0.677	–4	0.468	–82
1800	0.435	–99	0.673	–7.0	0.675	–6	0.448	–85
1900	0.427	–102	0.671	–9.0	0.673	–9	0.431	–89
2000	0.421	–104	0.668	–11	0.670	–11	0.413	–93
2100	0.412	–107	0.663	–14	0.664	–14	0.397	–98
2200	0.407	–110	0.655	–16	0.658	–16	0.380	–103
2300	0.401	–114	0.647	–19	0.648	–19	0.364	–109
2400	0.396	–117	0.634	–21	0.638	–21	0.347	–115
2500	0.396	–121	0.622	–23	0.623	–23	0.335	–122
2600	0.396	–124	0.608	–25	0.609	–26	0.319	–130
2800	0.393	–132	0.569	–29	0.571	–29	0.294	–147
3000	0.397	–142	0.527	–32	0.528	–32	0.276	–167

Table 5. Standby Mode Scattering Parameters
(V_{CC} = 2.7 V, EN1 = Low, EN2= Low)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.963	–4	0.010	35	0.010	43	0.951	–3
200	0.953	–7	0.014	61	0.016	61	0.948	–4
300	0.949	–10	0.022	71	0.022	68	0.947	–6
400	0.945	–13	0.029	76	0.029	72	0.945	–8
500	0.943	–16	0.036	75	0.036	74	0.944	–10
600	0.937	–19	0.043	70	0.043	74	0.941	–12
700	0.932	–21	0.050	76	0.049	74	0.938	–15
800	0.926	–24	0.054	74	0.056	74	0.935	–16
900	0.920	–27	0.062	75	0.063	73	0.932	–19
1000	0.914	–30	0.069	72	0.069	73	0.928	–21
1100	0.911	–33	0.075	72	0.075	72	0.923	–23
1200	0.903	–36	0.082	71	0.081	71	0.919	–25
1300	0.897	–38	0.086	72	0.087	70	0.913	–27
1400	0.892	–41	0.094	69	0.092	70	0.908	–29
1500	0.885	–44	0.097	69	0.097	69	0.902	–31
1600	0.877	–47	0.101	68	0.102	69	0.894	–33
1700	0.874	–50	0.104	68	0.106	69	0.887	–35
1800	0.861	–52	0.109	69	0.110	69	0.878	–37
1900	0.855	–55	0.115	69	0.115	69	0.868	–39
2000	0.850	–58	0.120	69	0.118	69	0.857	–42
2100	0.841	–61	0.120	70	0.122	70	0.845	–44
2200	0.831	–64	0.127	71	0.126	71	0.832	–46
2300	0.821	–67	0.132	72	0.132	73	0.816	–49
2400	0.808	–70	0.138	74	0.138	74	0.798	–52
2500	0.797	–73	0.146	75	0.146	76	0.776	–55
2600	0.784	–76	0.155	79	0.156	78	0.751	–58
2800	0.751	–82	0.183	80	0.184	81	0.688	–64
3000	0.720	–89	0.222	82	0.225	81	0.609	–70

APPLICATION INFORMATION

The MBC13720 SiGe:C LNA is designed for applications in the 400 MHz to 2.4 GHz range. It has four different modes; Low IP3, High IP3, Bypass, and Standby. The IC is programmable through the Enable 1 and 2 pins. In Low IP3 mode, the current consumption is optimized. Current consumption is higher in High IP3 mode to boost the intercept point performance. The gain difference between Low IP3 and High IP3 modes is typically 1.0 dB and typically the Low IP3 mode has a slightly better noise figure performance.

The internal bypass switch is designed for broadband applications. One of the advantages of the MBC13720 is the simplification of matching network in both bypass and amplifier modes. The bypass switch is designed such that the changes of input and output return losses between bypass mode and amplifier mode is minimized. As a result, the mismatch at the LNA input and output is minimized and therefore, the matching network design is simplified as well.

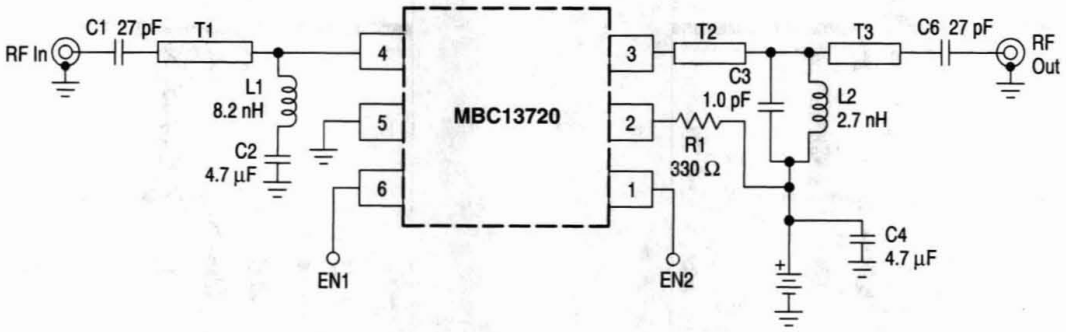
In the design of the external matching network, conjugate match condition does not necessarily provide the best noise figure performance. Balancing between noise figure, gain, and intercept point is the major design consideration. Typical circuits are provided in Figures 1 and 2 for 1.9 GHz, 2.4 GHz and 900 MHz applications.

In Figure 1, it shows the typical application circuit at 1.9 and 2.4 GHz. The noise figure, input intercept point, gain, and return losses are optimized. L2 and C2 act as a low frequency trap to improve the input intercept point. The noise figure measured on this board is 1.4 dB (in Low IP3 mode) at 1.9 GHz, including the external components, connectors, and PC board. The input third order intercept point is 10 dBm (in High IP3 mode).

In Figure 2, the typical application circuit at 900 MHz is shown. The input low frequency trap again is used to maximize the input intercept point. It has moderate IP3 performance and high gain. For higher IP3, Figure 3 shows the application circuit with feedback network. Capacitive feedback method is used to reduce the gain and therefore increase the 3rd order input intercept point. The feedback circuit is designed to provide unconditional stability.

The corresponding PCBs are shown in Figures 4 through 9. Typical characteristics of the application boards are shown in Table 6.

Figure 1. Typical 1.9 and 2.4 GHz LNA Application Schematic



T1, T2, T3 = 50 Ω Microstrip Line @ 150 mils

Figure 2. Typical 900 MHz LNA Application Schematic

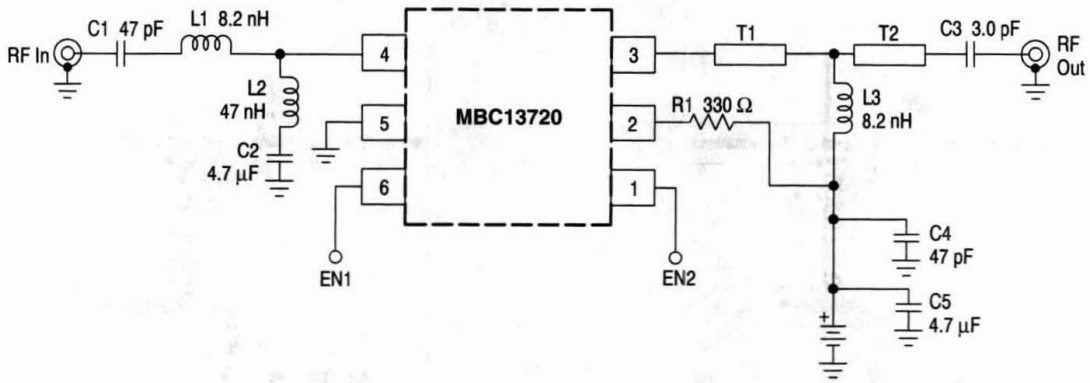


Figure 3. High IP3 900 MHz LNA Application Schematic

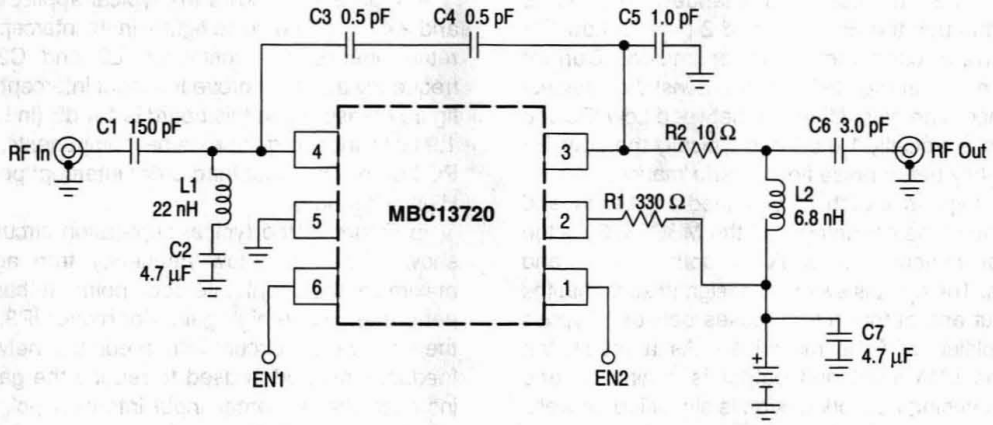


Figure 4. 1.9/2.4 GHz PCB

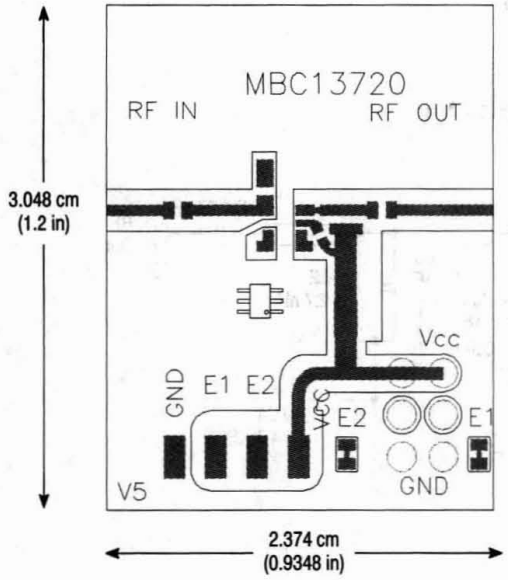


Figure 5. 1.9/2.4 GHz Assembly Diagram

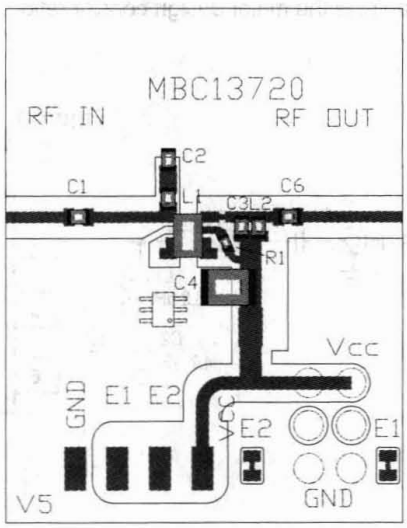


Figure 6. 900 MHz PCB

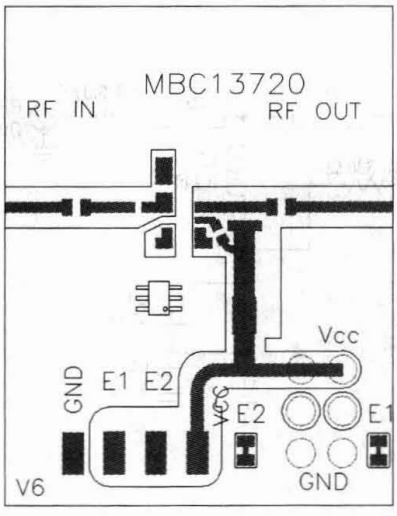


Figure 7. 900 MHz Assembly Diagram

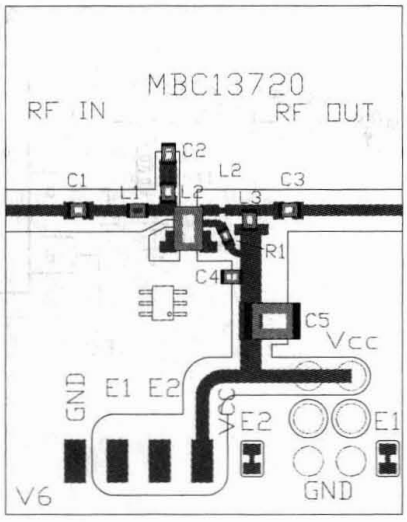


Figure 8. 900 MHz Capacitive Feedback PCB

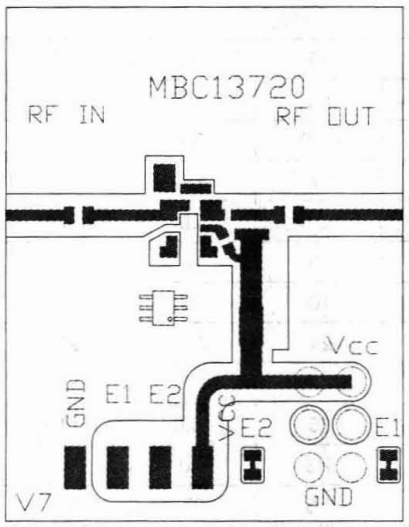


Figure 9. 900 MHz Capacitive Feedback Assembly Diagram

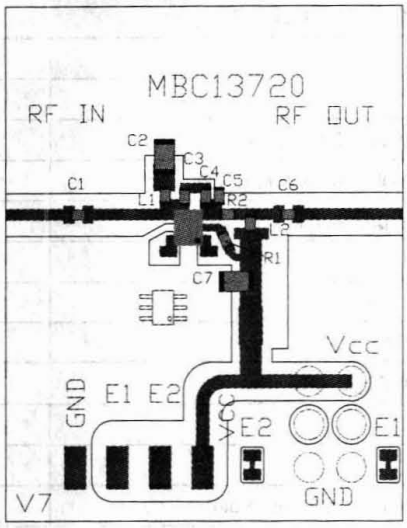


Table 6. Typical Electrical Characteristics of the Application Boards

Mode	Symbol	High IP3	Low IP3	Bypass	Standby	Unit
900 MHz TYPICAL (See Figure 2)						
Gain	G	21	20	–2.9	–22	dB
Noise Figure	NF	1.3	1.2	2.9	–	dB
Input Intermodulation Intercept Point	IIP3	2.0	–3.0	29	–	dBm
Output Intermodulation Intercept Point	OIP3	23	17	26	–	dBm
Output 1dB Compression Point	P_{1dB}	11.5	10.5	5.0	–	dBm
Input Return Loss	$\|S11\|^2$	11	10	12	–	dB
Output Return Loss	$\|S22\|^2$	11	10	15	–	dB
Reverse Isolation	$\|S12\|^2$	25	24	2.9	22	dB
900 MHz HIGH IP3 (See Figure 3)						
Gain	G	16	15	–4.0	–14.5	dB
Noise Figure	NF	1.4	1.3	4.0	–	dB
Input Intermodulation Intercept Point	IIP3	10	3.5	27	–	dBm
Output Intermodulation Intercept Point	OIP3	26	18.5	23	–	dBm
Output 1dB Compression Point	P_{1dB}	11.5	12	7.0	–	dBm
Input Return Loss	$\|S11\|^2$	12	11	8.0	–	dB
Output Return Loss	$\|S22\|^2$	12	12	14	–	dB
Reverse Isolation	$\|S12\|^2$	22	20	4.0	14.5	dB
1.9 GHz (See Figure 1)						
Gain	G	14	13	–2.5	–16	dB
Noise Figure	NF	1.5	1.4	2.5	–	dB
Input Intermodulation Intercept Point	IIP3	10	4.0	29	–	dBm
Output Intermodulation Intercept Point	OIP3	24.4	17	26.5	–	dBm
Output 1dB Compression Point	P_{1dB}	11.5	11	5.0	–	dBm
Input Return Loss	$\|S11\|^2$	10	8.0	20	–	dB
Output Return Loss	$\|S22\|^2$	8.0	7.0	30	–	dB
Reverse Isolation	$\|S12\|^2$	19	19	2.5	16	dB
2.4 GHz (See Figure 1)						
Gain	G	12	11	–2.8	–15	dB
Noise Figure	NF	1.7	1.65	2.8	–	dB
Input Intermodulation Intercept Point	IIP3	13	6.0	25	–	dBm
Output Intermodulation Intercept Point	OIP3	25	17.5	22	–	dBm
Output 1dB Compression Point	P_{1dB}	14	14	5.0	–	dBm
Input Return Loss	$\|S11\|^2$	12	10	12	–	dB
Output Return Loss	$\|S22\|^2$	8.0	7.0	14	–	dB
Reverse Isolation	$\|S12\|^2$	17	17	2.8	15	dB

NOTE: PCB trace losses and connector losses are included in the measurement results.

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MBC13916

The RF Building Block Series
General Purpose SiGe:C RF Cascode Amplifier

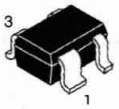
The MBC13916 is a cost–effective, high isolation amplifier fabricated with Motorola's Advanced RF BiCMOS process using the SiGe:C module. It is intended to be a similar replacement for the MRFIC0916 and is housed in the smaller SOT–343R surface mount package. As with the MRFIC0916, the device is designed for general purpose RF applications, but has improved high frequency gain and noise figure. On–chip bias circuitry sets the bias point, while matching is accomplished off–chip, affording the maximum in application flexibility.

- Usable Frequency Range = 100 to 2500 MHz
- 19 dB typical gain at 900 MHz, V_{CC} = 2.7 V
- NF_{min} (Device Level) = 0.9 dB @ 900 MHz
- NF_{min} (Device Level) = 1.9 dB @ 1.9 GHz
- 2.5 dBm typical Output Power at 1.0 dB Gain Compression at 900 MHz, V_{CC} = 2.7 V
- 45 dB Typical Reverse Isolation (Device Level) at 900 MHz, V_{CC} = 2.7 V
- 4.7 mA Typ Bias Current at V_{CC} = 2.7 V
- 2.7 to 5.0 V Supply
- Industry Standard SOT–343R Package
- Available Only in Tape and Reel Packaging
- Device Weight = 0.00642 g (Typ)

GENERAL PURPOSE SiGe:C RF CASCODE AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

Pin 1. Gnd
2. RF In
3. RF Out
4. Gnd



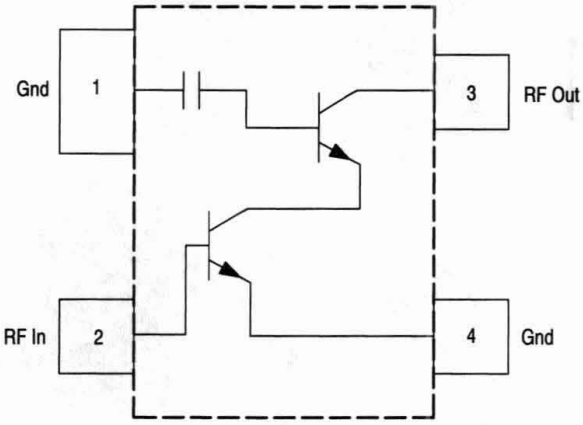
(Scale 4:1)

PLASTIC PACKAGE
SOT–343R
(Tape & Reel Only)

ORDERING INFORMATION

Device	Device Marking	Package
MBC13916T1	916	SOT–343R

Functional Block Diagram



(SOT–343R package)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
RF Input Power	P_{RF}	10	dBm
Power Dissipation	P_{DIS}	100	mW
Supply Current	I_{CC}	20	mA
Thermal Resistance, Junction to Case	$R_{\theta JC}$	400	C/W
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Case Temperature	T_C	–40 to 100	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤550 V and Machine Model (MM) ≤50 V. Additional EST data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
RF Frequency	f_{RF}	100	–	2500	MHz
Supply Voltage	V_{CC}	2.7	–	5.0	Vdc

DEVICE LEVEL CHARACTERISTICS (V_{CC} = 2.7 V, T_A = 25°C, measured in S–parameter test fixture, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Insertion Gain	$\|S_{21}\|^2$				dB
f = 900 MHz		–	16.5	–	
f = 1900 MHz		–	10	–	
Maximum Stable Gain and/or Minimum Available Gain [Note 1]	MSG, MAG				dB
f = 900 MHz		–	24.5	–	
f = 1900 MHz		–	14.3	–	
Minimum Noise Figure [Note 2]	NF_{min}				dB
f = 900 MHz		–	0.9	–	
f = 1900 MHz		–	1.9	–	
Output Third Order Intercept Point [Note 3]	OIP3				dBm
f = 900 MHz		–	16.5	–	
f = 1900 MHz		–	17	–	
Reverse Isolation	$\|S_{12}\|^2$				dB
f = 900 MHz		–	–45	–	
f = 1900 MHz		–	–31	–	

NOTES: 1. Maximum Available Gain and Maximum Stable Gain are defined by the K factor as follows:

$$MAG = \left|\frac{S_{21}}{S_{12}}\left(K \pm \sqrt{K^2 - 1}\right)\right|, \text{ if } K > 1, \; MSG = \left|\frac{S_{21}}{S_{12}}\right|, \text{ if } K < 1$$

2. Device matched for best noise figure.
3. Z_{out} matched for optimum IP3.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V, T_A = 25°C, f_{RF} = 900 MHz, Tested in Circuit Shown in Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Small Signal Gain	S_{21}	17	19	21	dB
Noise Figure	NF	–	1.25	–	dB
Power Output at 1.0 dB Gain Compression	P_{1dB}	0	2.5	–	dBm
Output 3rd Order Intercept Point	OIP3	–	13	–	dBm
Reverse Isolation	S_{12}	–	–42	–	dB
Supply Current	I_{CC}	3.8	4.7	5.6	mA

Figure 1. 900 MHz Applications Circuit Configuration

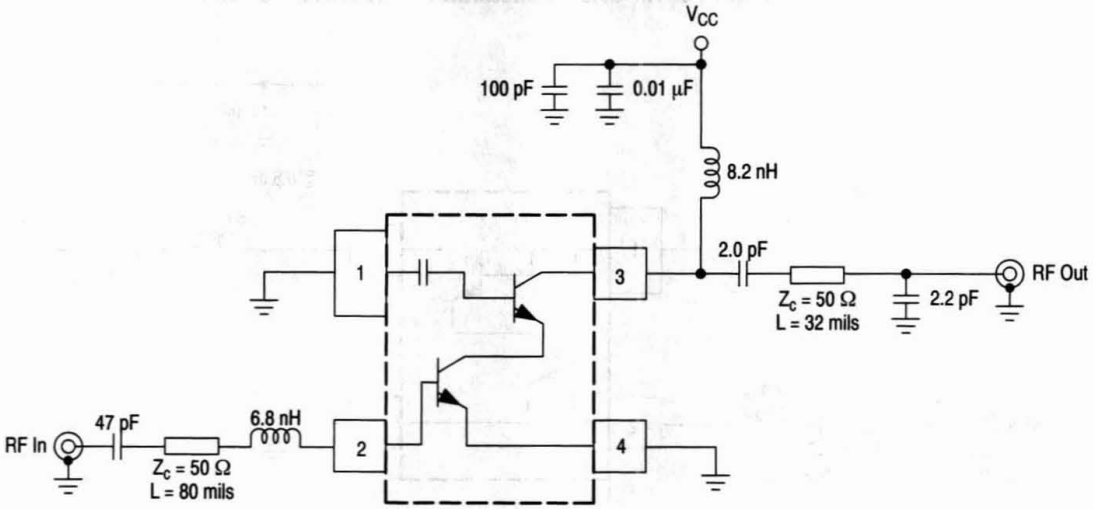
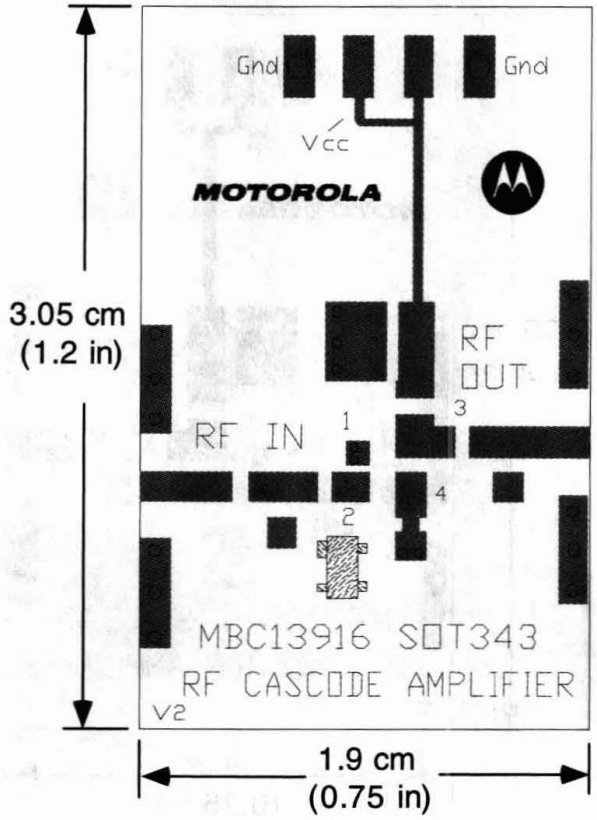


Figure 2. 900 MHz Printed Circuit Board



NOTE:
PCB material FR4
ε_r = 4.5
h = 25 mils
t = 1.75

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V, T_A = 25°C, f_{RF} = 1.9 GHz, Tested in Circuit Shown in Figure 3, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Small Signal Gain	S_{21}	9.5	11.5	13.5	dB
Noise Figure	NF	–	2.1	–	dB
Power Output at 1.0 dB Gain Compression	P_{1dB}	–	–4.0	–	dBm
Output 3rd Order Intercept Point	OIP3	–	5.5	–	dBm
Reverse Isolation	S_{12}	–	–28	–	dB
Supply Current	I_{CC}	3.8	4.7	5.6	mA

Figure 3. 1.9 GHz Application Configuration Circuit

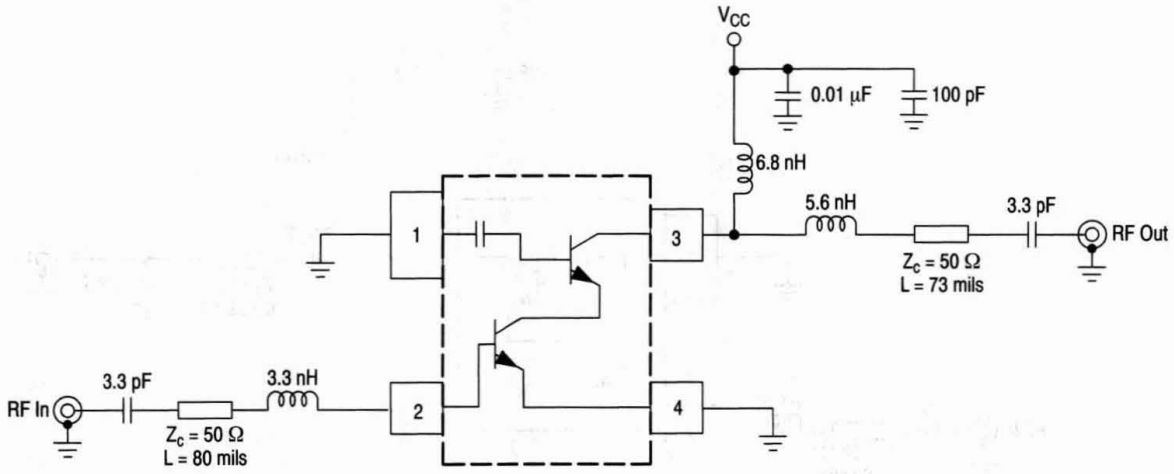
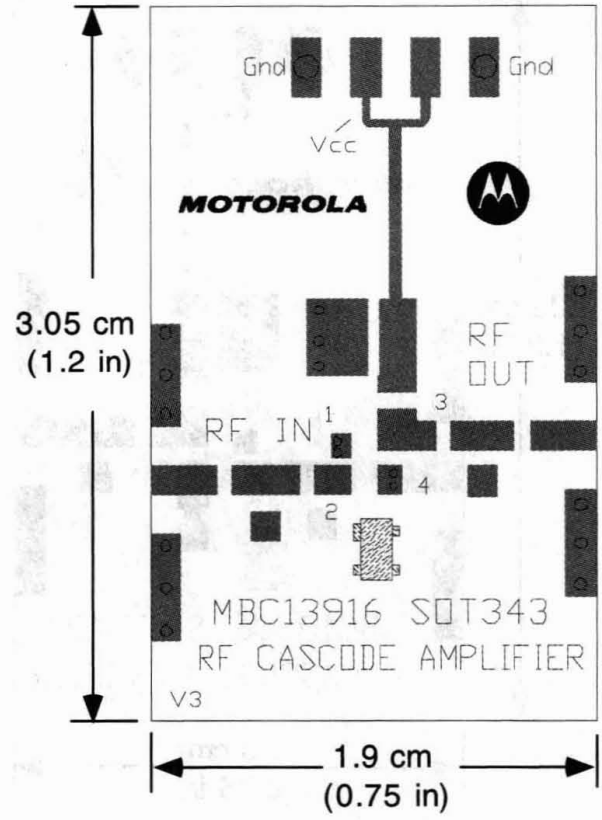


Figure 4. 1900 MHz Printed Circuit Board



NOTE:
PCB material FR4
ε_r = 4.5
h = 25 mils
t = 1.75

Figure 5. GUmax versus Frequency

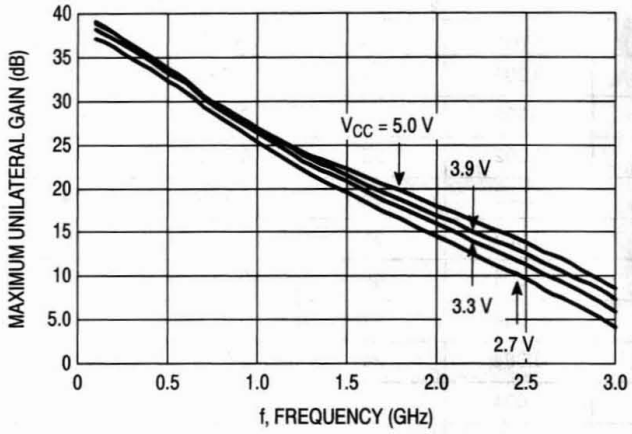


Figure 6. Output Power versus Input Power

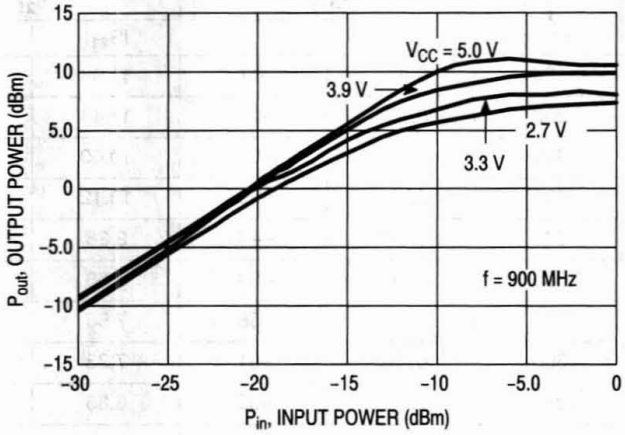


Figure 7. Output Power versus Input Power

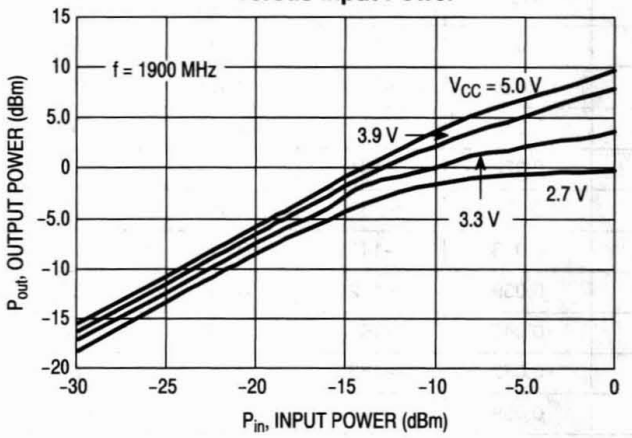


Figure 8. Supply Current versus Input Power

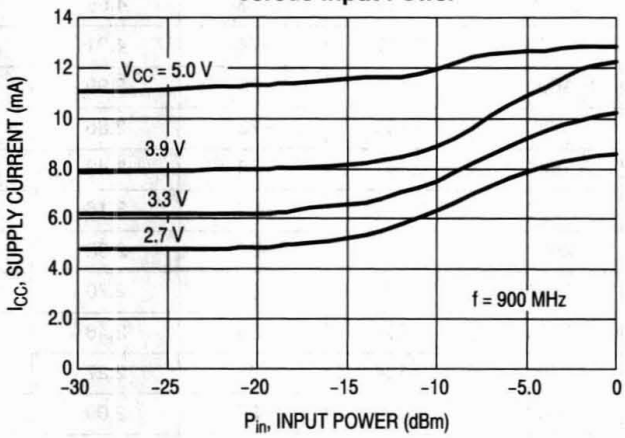


Figure 9. Supply Current versus Input Power

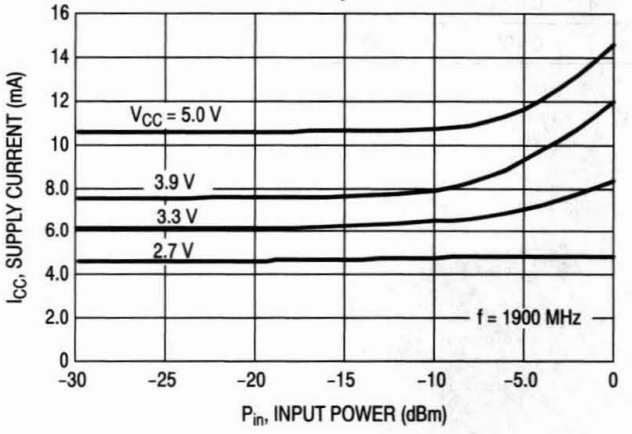


Table 1. Scattering Parameters
(V_{CC} = 2.7 V, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.829	–11	11.98	165	0.001	17	0.955	–4
200	0.798	–21	11.43	152	0.002	47	0.957	–7
300	0.753	–31	10.69	139	0.002	55	0.956	–11
400	0.701	–39	10.12	128	0.003	56	0.955	–14
500	0.648	–46	9.28	118	0.003	51	0.955	–18
600	0.599	–53	8.66	108	0.004	49	0.954	–22
700	0.554	–58	7.95	98	0.004	41	0.947	–26
800	0.518	–61	7.33	90	0.004	24	0.941	–30
900	0.485	–65	6.83	82	0.004	15	0.933	–34
1000	0.458	–67	6.23	74	0.004	–4	0.926	–38
1100	0.438	–69	5.78	67	0.004	–28	0.915	–43
1200	0.426	–71	5.39	60	0.005	–50	0.902	–46
1300	0.417	–72	4.97	52	0.006	–74	0.893	–51
1400	0.414	–73	4.59	46	0.008	–93	0.879	–54
1500	0.415	–74	4.31	39	0.011	–106	0.868	–58
1600	0.421	–75	3.99	32	0.014	–115	0.851	–62
1700	0.430	–76	3.66	25	0.018	–125	0.835	–66
1800	0.441	–78	3.43	19	0.022	–131	0.818	–70
1900	0.455	–80	3.16	12	0.027	–139	0.803	–73
2000	0.474	–82	2.93	5	0.033	–146	0.777	–77
2100	0.490	–85	2.70	–1	0.039	–152	0.761	–81
2200	0.504	–88	2.48	–8	0.045	–159	0.735	–85
2300	0.524	–92	2.27	–14	0.052	–163	0.707	–89
2400	0.542	–95	2.09	–21	0.059	–169	0.683	–93
2500	0.559	–98	1.90	–28	0.067	–175	0.651	–98
2600	0.572	–103	1.70	–34	0.075	180	0.624	–102
2700	0.587	–106	1.56	–40	0.083	174	0.593	–107
2800	0.603	–110	1.40	–48	0.091	169	0.562	–111
2900	0.610	–114	1.26	–55	0.098	163	0.533	–116
3000	0.613	–118	1.11	–60	0.105	160	0.501	–120

Table 2. Scattering Parameters
(V_{CC} = 3.0 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.812	–11	13.42	165	0.001	11	0.954	–3
200	0.778	–21	12.73	151	0.001	50	0.955	–7
300	0.731	–30	11.82	138	0.002	58	0.956	–11
400	0.677	–38	11.10	127	0.003	50	0.954	–14
500	0.623	–44	10.12	116	0.003	51	0.954	–18
600	0.575	–50	9.37	107	0.003	43	0.952	–22
700	0.533	–54	8.56	98	0.003	30	0.945	–26
800	0.499	–57	7.85	90	0.004	24	0.937	–30
900	0.470	–59	7.29	82	0.004	8	0.930	–34
1000	0.448	–61	6.63	74	0.003	–11	0.923	–38
1100	0.433	–63	6.14	67	0.004	–38	0.911	–42
1200	0.423	–64	5.72	60	0.005	–58	0.900	–46
1300	0.418	–65	5.27	53	0.006	–77	0.891	–50
1400	0.421	–66	4.87	47	0.008	–96	0.878	–54
1500	0.425	–67	4.56	40	0.011	–108	0.868	–58
1600	0.432	–68	4.23	34	0.014	–120	0.852	–61
1700	0.444	–70	3.89	27	0.018	–126	0.838	–65
1800	0.459	–72	3.63	21	0.022	–133	0.822	–69
1900	0.473	–74	3.35	15	0.027	–140	0.809	–73
2000	0.490	–77	3.12	8	0.033	–147	0.784	–77
2100	0.509	–80	2.87	2	0.039	–152	0.769	–80
2200	0.527	–83	2.64	–5	0.045	–159	0.744	–84
2300	0.545	–86	2.42	–11	0.051	–163	0.717	–88
2400	0.560	–90	2.23	–17	0.059	–170	0.694	–92
2500	0.579	–94	2.03	–24	0.067	–175	0.663	–97
2600	0.594	–98	1.82	–30	0.075	–180	0.637	–101
2700	0.606	–101	1.68	–36	0.083	175	0.607	–105
2800	0.620	–105	1.50	–43	0.090	169	0.576	–110
2900	0.630	–110	1.35	–50	0.097	164	0.548	–114
3000	0.636	–113	1.19	–55	0.105	160	0.516	–119

Table 3. Scattering Parameters
(V_{CC} = 3.3 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.796	–11	14.82	164	0.001	25	0.954	–3
200	0.760	–20	13.98	150	0.001	50	0.955	–7
300	0.711	–29	12.90	137	0.002	46	0.955	–11
400	0.655	–36	12.03	126	0.002	55	0.955	–14
500	0.602	–42	10.90	115	0.003	50	0.954	–18
600	0.556	–46	10.04	106	0.003	45	0.954	–22
700	0.517	–50	9.12	97	0.003	34	0.947	–26
800	0.487	–52	8.34	89	0.003	22	0.940	–30
900	0.463	–54	7.72	82	0.003	11	0.933	–34
1000	0.444	–56	7.02	74	0.003	–6	0.927	–38
1100	0.432	–57	6.49	67	0.003	–40	0.917	–42
1200	0.428	–58	6.03	61	0.005	–69	0.905	–46
1300	0.427	–59	5.55	53	0.006	–88	0.896	–50
1400	0.430	–60	5.13	48	0.008	–99	0.883	–53
1500	0.437	–61	4.81	41	0.011	–111	0.874	–57
1600	0.449	–62	4.45	35	0.014	–118	0.858	–61
1700	0.462	–64	4.09	29	0.018	–128	0.843	–64
1800	0.475	–66	3.83	23	0.022	–134	0.829	–68
1900	0.493	–69	3.53	17	0.027	–140	0.815	–72
2000	0.512	–72	3.28	10	0.032	–148	0.790	–76
2100	0.529	–75	3.03	4	0.038	–152	0.776	–79
2200	0.544	–78	2.79	–2	0.045	–159	0.752	–83
2300	0.565	–82	2.56	–8	0.051	–164	0.726	–87
2400	0.583	–85	2.37	–14	0.058	–169	0.704	–91
2500	0.599	–89	2.16	–21	0.067	–175	0.674	–96
2600	0.613	–93	1.94	–27	0.075	–179	0.648	–100
2700	0.629	–97	1.79	–32	0.083	175	0.621	–105
2800	0.643	–101	1.60	–39	0.091	170	0.589	–109
2900	0.650	–105	1.44	–46	0.098	164	0.562	–114
3000	0.653	–109	1.28	–51	0.105	160	0.531	–118

Table 4. Scattering Parameters
(V_{CC} = 3.9 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.768	–10	17.37	163	0.001	5	0.951	–3
200	0.728	–19	16.21	148	0.001	44	0.952	–7
300	0.676	–27	14.75	135	0.002	39	0.953	–11
400	0.621	–33	13.55	124	0.002	44	0.952	–14
500	0.573	–37	12.13	113	0.002	55	0.952	–18
600	0.532	–41	11.07	104	0.003	41	0.951	–22
700	0.498	–43	9.96	96	0.003	36	0.943	–26
800	0.477	–45	9.06	88	0.003	20	0.937	–29
900	0.461	–46	8.36	81	0.002	13	0.930	–33
1000	0.448	–47	7.56	74	0.002	–25	0.925	–37
1100	0.442	–48	6.97	68	0.003	–54	0.914	–41
1200	0.444	–49	6.48	62	0.005	–75	0.903	–45
1300	0.448	–50	5.95	54	0.006	–94	0.895	–49
1400	0.455	–51	5.50	49	0.008	–107	0.883	–52
1500	0.465	–53	5.15	43	0.011	–113	0.875	–56
1600	0.480	–55	4.77	37	0.014	–122	0.860	–60
1700	0.495	–56	4.39	32	0.018	–130	0.847	–63
1800	0.507	–59	4.11	26	0.022	–136	0.834	–67
1900	0.525	–62	3.80	20	0.027	–142	0.821	–71
2000	0.546	–65	3.54	14	0.032	–148	0.799	–74
2100	0.565	–67	3.28	8	0.038	–153	0.785	–78
2200	0.578	–71	3.02	2	0.044	–160	0.763	–82
2300	0.598	–75	2.78	–3	0.051	–163	0.739	–85
2400	0.617	–79	2.57	–9	0.059	–169	0.719	–90
2500	0.633	–82	2.36	–15	0.066	–174	0.690	–94
2600	0.645	–86	2.12	–21	0.073	–179	0.666	–98
2700	0.660	–90	1.96	–27	0.082	176	0.639	–103
2800	0.678	–94	1.76	–33	0.089	171	0.609	–107
2900	0.683	–98	1.59	–39	0.097	165	0.583	–112
3000	0.683	–102	1.42	–44	0.105	162	0.553	–116

Table 5. Scattering Parameters
(V_{CC} = 5.0 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
100	0.719	–9	21.47	161	0.001	5	0.939	–3
200	0.678	–17	19.60	145	0.001	18	0.939	–7
300	0.628	–23	17.43	132	0.001	38	0.940	–10
400	0.579	–27	15.66	120	0.002	47	0.937	–14
500	0.540	–30	13.78	110	0.002	38	0.936	–18
600	0.512	–32	12.40	101	0.003	37	0.934	–22
700	0.492	–34	11.05	93	0.002	32	0.927	–26
800	0.480	–34	9.97	86	0.002	9	0.920	–30
900	0.472	–35	9.12	79	0.002	–14	0.914	–34
1000	0.470	–37	8.21	73	0.002	–54	0.908	–38
1100	0.473	–37	7.54	67	0.003	–75	0.899	–42
1200	0.478	–39	6.97	61	0.004	–90	0.890	–46
1300	0.484	–40	6.37	54	0.006	–101	0.884	–50
1400	0.496	–42	5.86	50	0.008	–114	0.875	–54
1500	0.509	–44	5.49	44	0.010	–120	0.871	–57
1600	0.521	–46	5.08	39	0.013	–128	0.858	–60
1700	0.535	–49	4.67	34	0.017	–133	0.848	–63
1800	0.552	–51	4.38	29	0.021	–139	0.838	–67
1900	0.570	–54	4.06	23	0.025	–144	0.829	–70
2000	0.587	–56	3.80	18	0.030	–150	0.807	–73
2100	0.604	–60	3.54	13	0.036	–154	0.795	–76
2200	0.621	–63	3.28	7	0.042	–160	0.772	–79
2300	0.643	–67	3.04	2	0.048	–164	0.746	–83
2400	0.658	–70	2.84	–4	0.056	–169	0.722	–87
2500	0.673	–74	2.61	–10	0.063	–175	0.687	–91
2600	0.690	–78	2.36	–16	0.071	–179	0.657	–96
2700	0.705	–82	2.19	–21	0.079	176	0.623	–101
2800	0.715	–86	1.97	–27	0.088	170	0.588	–107
2900	0.720	–91	1.78	–33	0.094	164	0.556	–113
3000	0.723	–94	1.57	–38	0.101	161	0.523	–119

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MC13751

Dual-Band Upmixer and Driver Amplifier

The MC13751 is an integrated transmit upmixer and driver amplifier designed for use in cellular phones. It includes two mixers and two RF step attenuators. The device is fabricated using Motorola's Advanced RF BiCMOS process with the SiGe:C option and is housed in a leadless QFN–24 package.

- Total Gain:
  22 dB for Low Band
  19.5 dB for High Band
- Total Current Consumption = 53 mA (Typ)
- Available in Tape and Reel, 2500 Units per 12 mm, 7 inch Reel

DUAL–BAND UPMIXER AND DRIVER AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

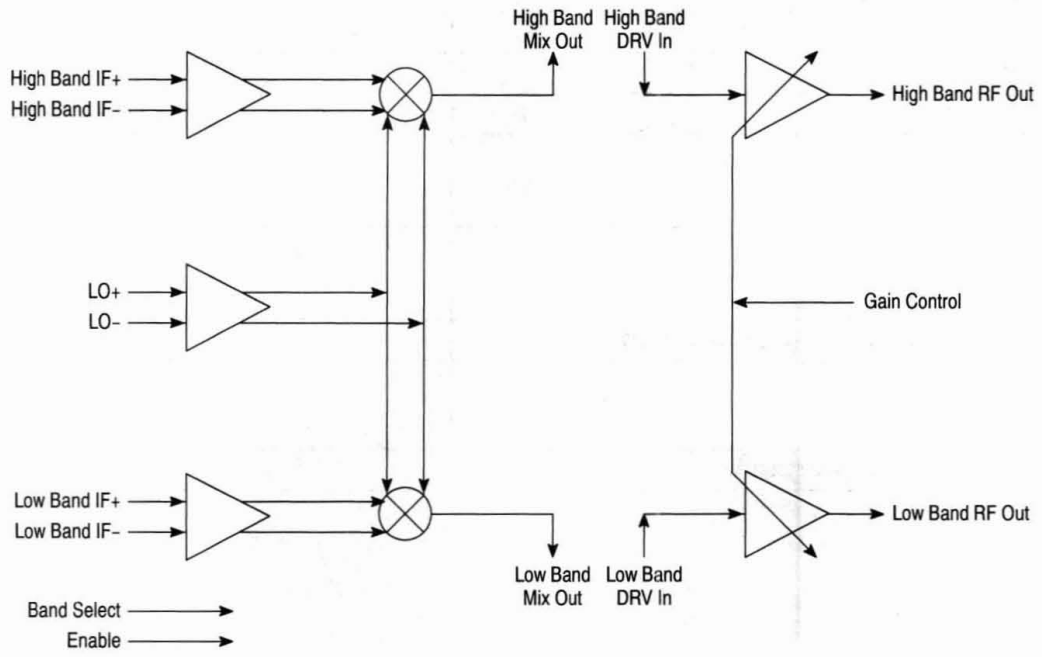
(Scale 2:1)

PLASTIC PACKAGE
CASE 1307
(QFN–24, Tape and Reel Only)

ORDERING INFORMATION

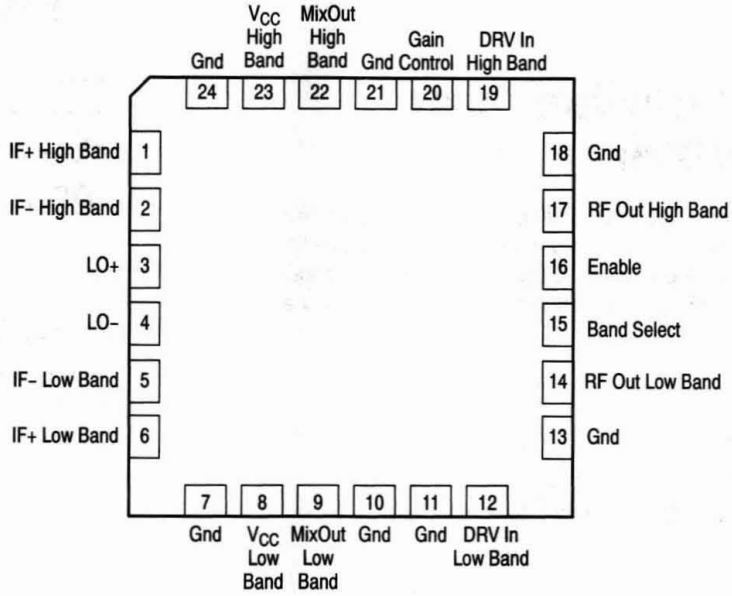
Device	Device Marking	Package
MC13751FCR2	MC751	QFN–24

Simplified Block Diagram



This device contains 223 active transistors.

CONTACT CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	3.6	V
LO Input Power		0	dBm
IF Input Level		0	dBm
Operating Temperature Range	T_A	–30 to 85	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤250 V and Machine Model (MM) ≤25 V. Additional ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage		2.7	2.78	2.86	V
Power Supply Current		–	53	64	mA
Enable					V
Inactive State		–	–	0.6	
Active State		1.6	–	–	
Band					V
800 MHz Enabled		–	–	0.6	
1900 MHz Enabled		1.6	–	–	
Power Down State Leakage Current (0.2 V Logic Levels)		–	–	25	µA
Gain Select Voltage					V
Gain High = 1		1.6	–	–	
Gain Low = 0		–	–	0.6	
Gain Select (enable and band signals current)		–	–	10	µA

ELECTRICAL CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
IF Frequency Low Band High Band			 150 150	 178 213	 250 250	MHz
LO Frequency Range Low Band High Band			 1002 2028	 – –	 1029 2125	MHz
RF Frequency Range Low Band High Band			 824 1850	 – –	 849 1910	MHz
IF Input Level, Both Bands (differential, typ –7.0 dBm)			–60	–	0	dBm
LO Input Level, Both Bands (differential)			–12	–10	–8.0	dBm
RF GMSK Output Level Both Bands Both Bands, Low Gain			 10 6.0	 – –	 – –	dBm
RF Linear Output Level, TDMA Both Bands Both Bands, Low Gain			 6.0 2.0	 – –	 – –	dBm
ACP @ f ±30 kHz, TDMA @ f ±60 kHz, TDMA @ f ±200 kHz, GSM @ f ±400 kHz, GSM			 –32 –51 –36 –66	 – – – –	 – – – –	dBc
Conversion Gain Mixer Low Band High Band			 6.3 6.5	 8.3 8.5	 10.3 10.5	dBc
Gain, Driver, High Gain Low Band High Band			 11.7 9.0	 13.7 11	 15.7 13	dBc
Gain, Drivers, Low Gain Low Band High Band			 7.7 5.0	 9.7 7.0	 11.7 9.0	dBc
Noise Figure Mixer (SSB) Drivers			 – –	 11 5.0	 14 8.0	dB
IF Impedance (differential)			–	200	–	Ω
LO Impedance (differential)			–	100	–	Ω
RF Impedance (Both Bands @ Mixer (rf out, driver rf in and driver rf out))			–	50	–	Ω

SPURIOUS (measured with interstage filter)

Characteristic	Symbol	Min	Typ	Max	Unit
LO Leakage to RF Port (Both bands, P_{out} = 6.0 dBm)		–	–	–20	dBc
IF Leakage to RF Port (Both bands)		–	–	–50	dBc
Image Supression (Both bands)		–	–	–20	dBc
2x Image Supression (Both bands)		–	–	–40	dBc
LO – 2x IF (Both bands)		–	–	–30	dBc
2x LO – 7x IF (Low band)		–	–	–40	dBc
5 * IF (Low band)		–	–	–80	dBc
11 * IF (Low band)		–	–	–80	dBc

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MRFIC0970

Product Preview

3.2 V GSM GaAs Integrated Power Amplifier

The MRFIC0970 is a single supply, RF power amplifier designed for the 2.0 W GSM900 handheld radios. The device is packaged in the QFN–20 package, with exposed backside pad, which allows excellent electrical and thermal performance through a solderable contact.

- Target 3.2 V Characteristics:
  RF Output Power: 34.5 dBm Minimum
  Efficiency: 50% Minimum
- Single Positive Supply Solution

GSM 880 – 915 MHz
INTEGRATED
POWER AMPLIFIER

SEMICONDUCTOR
TECHNICAL DATA

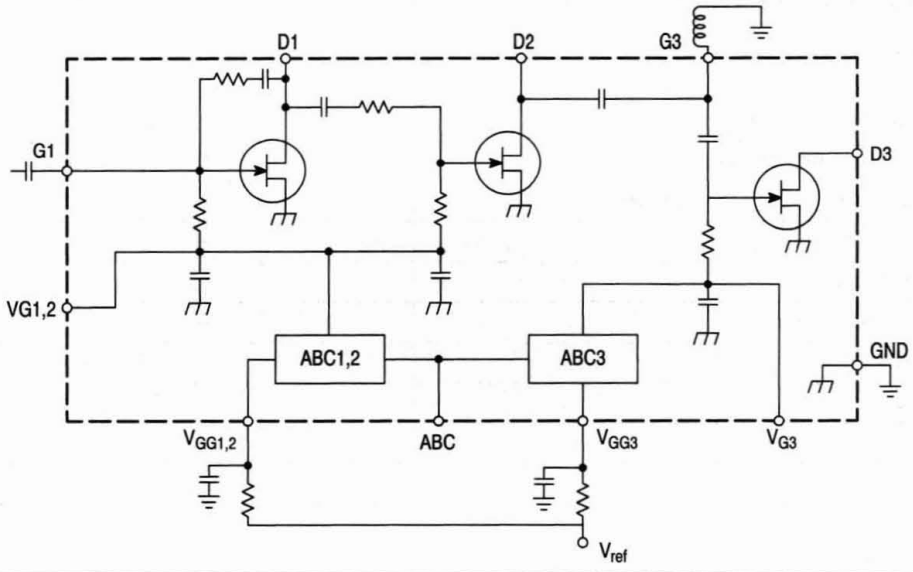
(Scale 2:1)

PLASTIC PACKAGE
CASE 1308
(QFN–20)

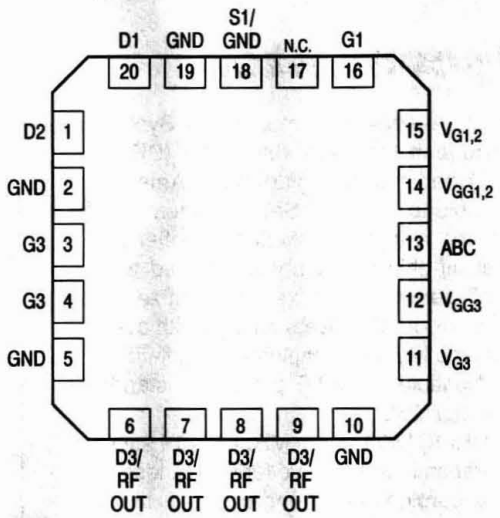
ORDERING INFORMATION

Device	Device Marking	Package
MRFIC0970	0970	QFN–20

Functional Block Diagram



CONTACT CONNECTIONS



The MRFIC Line

1.9 GHz GaAs Upconverter

MRFIC1813

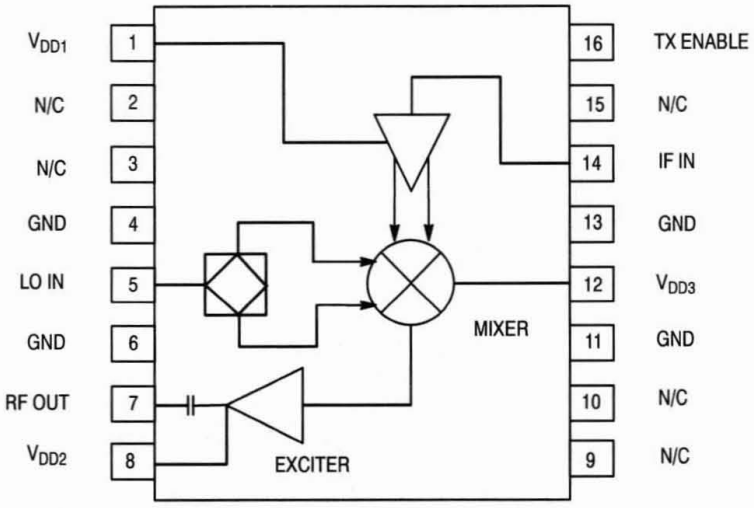
1.9 GHz UPMIXER AND EXCITER AMPLIFIER

CASE 948C–03
(TSSOP–16)

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS) and the emerging North American systems. The MRFIC1813 is also applicable to 2.4 GHz ISM equipment. The device combines a balanced upmixer and a transmit exciter amplifier in a low-cost TSSOP–16 package. Minimal off-chip matching is required while allowing for maximum flexibility and efficiency. The mixer is optimized for low–side injection and provides more than 12 dB of conversion gain with over 0 dBm output at 1 dB gain compression. Image filtering is implemented off-chip to allow maximum flexibility. A CMOS compatible ENABLE pin allows standby operation where the current drain is less than 250 μA.

Together with other devices from the MRFIC180X or the MRFIC240X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone or 2.4 GHz ISM band equipment.

- Usable Frequency Range = 1.7 to 2.5 GHz
- 15 dB Typ IF to RF Conversion Gain
- 3 dBm Power Output Typ, 0 dBm Minimum at 1 dB Gain Compression
- Simple Off-chip Matching for Maximum Flexibility
- Low Power Consumption = 75 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 Volts
- Low LO Power Requirement = – 5 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1813R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1813



Pin Connections and Functional Block Diagram

REV 2

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

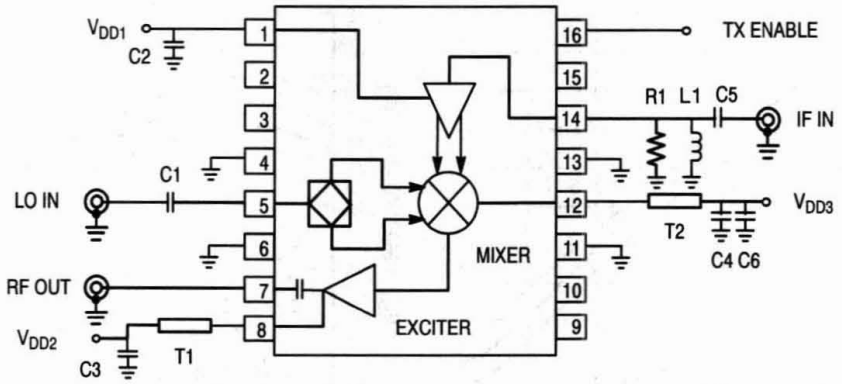
Ratings	Symbol	Limit	Unit
Supply Voltage	V_{DD1}, V_{DD2}, V_{DD3}	5.5	Vdc
IF Input Power	P_{IF}	3	dBm
LO Input Power	P_{LO}	3	dBm
Enable Voltage	TX ENABLE	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Output Frequency	f_{RF}	1.7 to 2.5	GHz
LO Input Frequency	f_{LO}	1.5 to 2.4	GHz
IF Input Frequency	f_{IF}	70 to 350	MHz
Supply Voltage	V_{DD}	2.7 to 4.5	Vdc
TX Enable Voltage, ON	TX ENABLE	2.7 to V_{DD}	Vdc
TX Enable Voltage, OFF	TX ENABLE	0 to 0.2	Vdc

ELECTRICAL CHARACTERISTICS ($V_{DD1,2,3}$, TX ENABLE= 3 V, T_A = 25°C, f_{LO} = 1.65 GHz @ – 5 dBm, f_{IF} = 250 MHz @ –15 dBm)

Characteristic	Min	Typ	Max	Unit
IF to RF Small Signal Conversion Gain (P_{RF} = –35 dBm)	12	15	—	dB
RF Output 1 dB Gain Compression	0	3	—	dBm
RF Output 3rd Order Intercept	—	11	—	dBm
LO Feedthrough to RF Port	—	–15	–10	dBm
Noise Figure	—	11	—	dB
Lower Sideband Output Power at RF Port	—	–10	–6	dBm
Supply Current TX Mode	—	25	35	mA
Supply Current Standby Mode (TX ENABLE = 0 V, LO Off)	—	100	250	μA
TX Enable Current	—	3	—	μA



C1, C2, C3, C4 15 pF
C6 1 μF
R1 300 Ω
T1, T2 MICROSTRIP, Z_0 = 73 Ω, θ = 29° @ 1.9 GHz
BOARD MATERIAL – GLASS/EPOXY, ε_r = 4.45,
DIELECTRIC THICKNESS = 0.018 INCH

IF Frequency	L1	C5
110 MHz	180 nH	12 pF
250 MHz	68 nH	5.6 pF
350 MHz	39 nH	3.9 pF

Figure 1. Applications Circuit Configuration

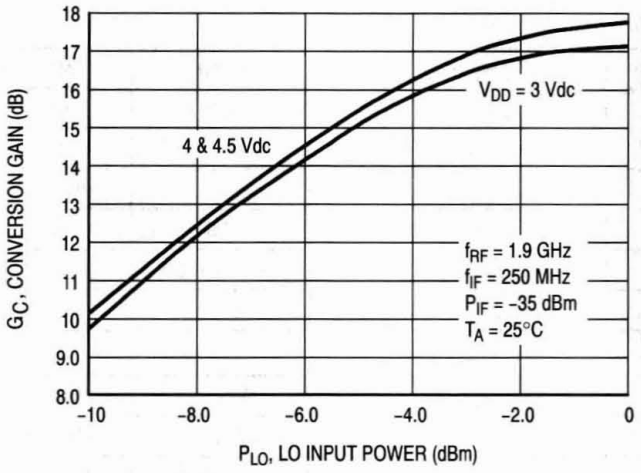


Figure 2. Conversion Gain versus LO Power

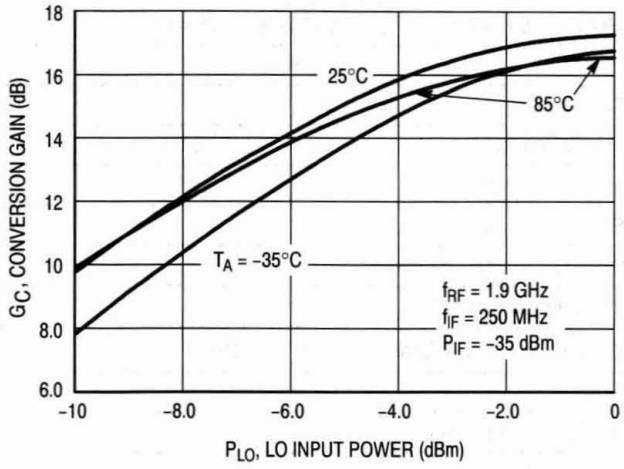


Figure 3. Conversion Gain versus LO Power

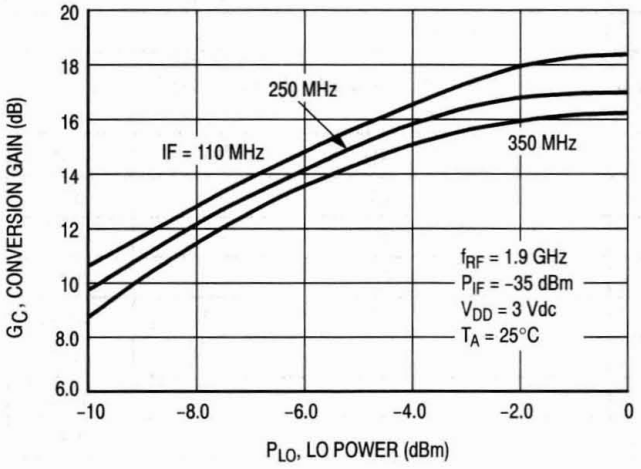


Figure 4. Conversion Gain versus LO Power

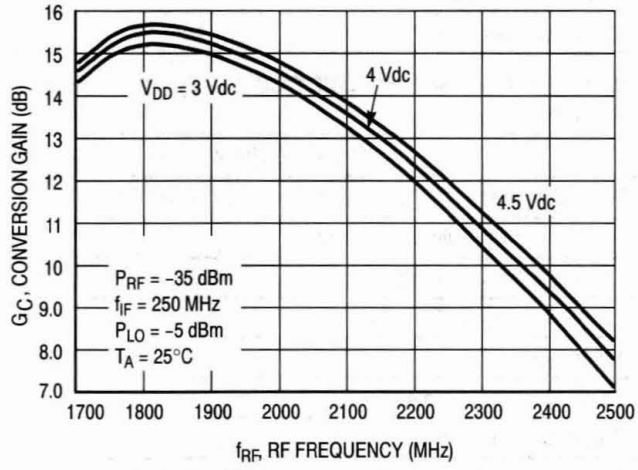


Figure 5. Conversion Gain versus RF Frequency

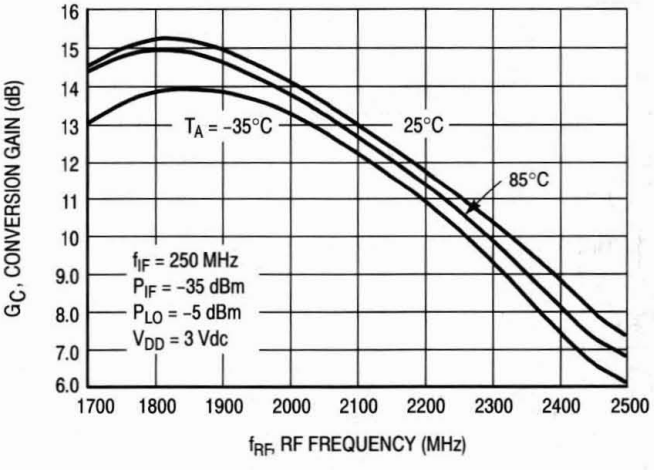


Figure 6. Conversion Gain versus RF Frequency

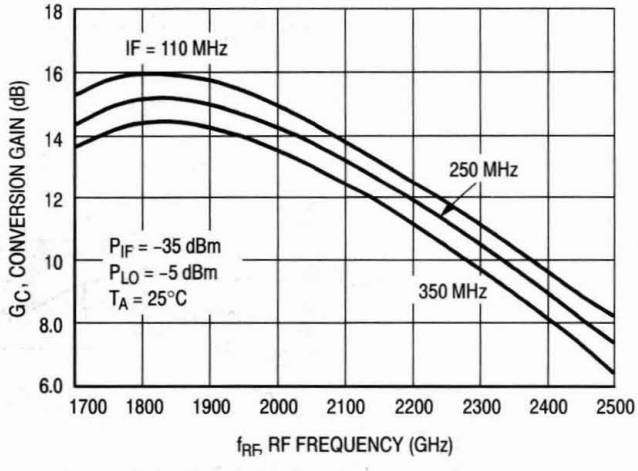


Figure 7. Conversion Gain versus RF Frequency

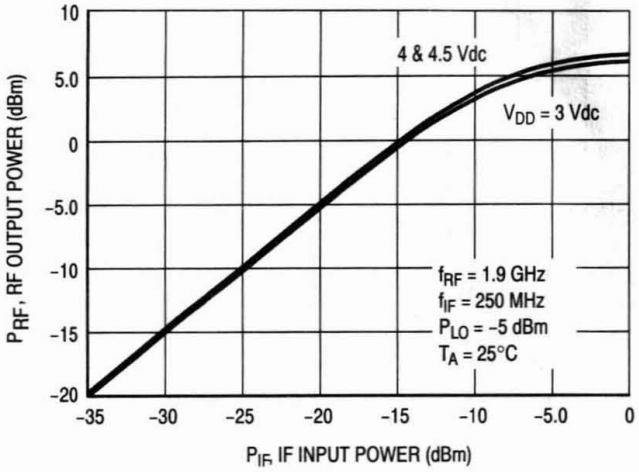


Figure 8. RF Output versus Input Power

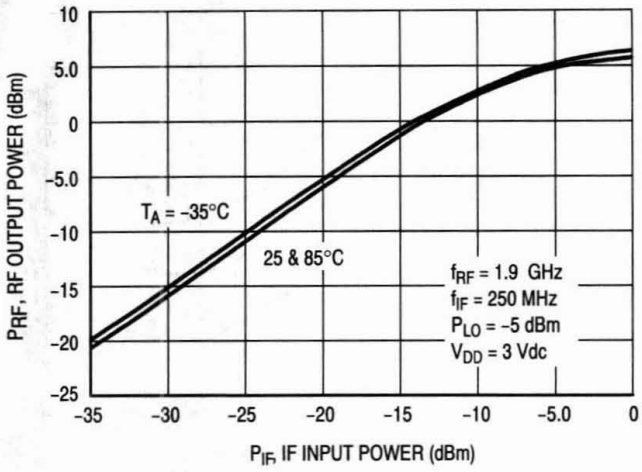


Figure 9. RF Output Power versus IF Input Power

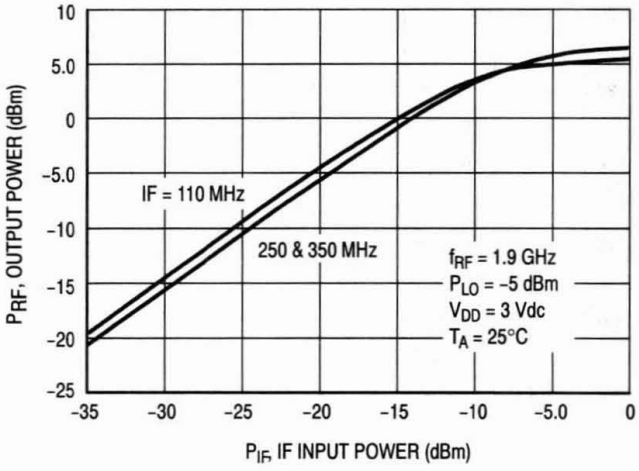


Figure 10. RF Output versus IF Input Power

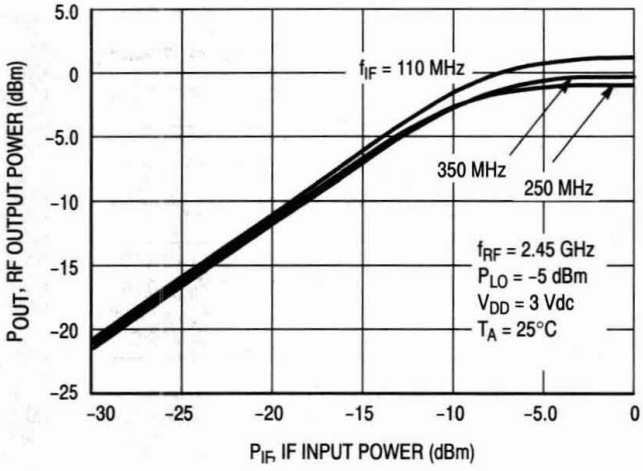


Figure 11. Output Power versus IF Input Power

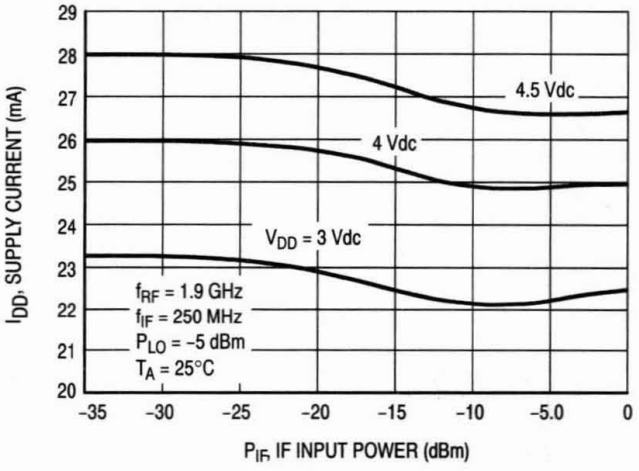


Figure 12. Supply Current versus IF Input Power

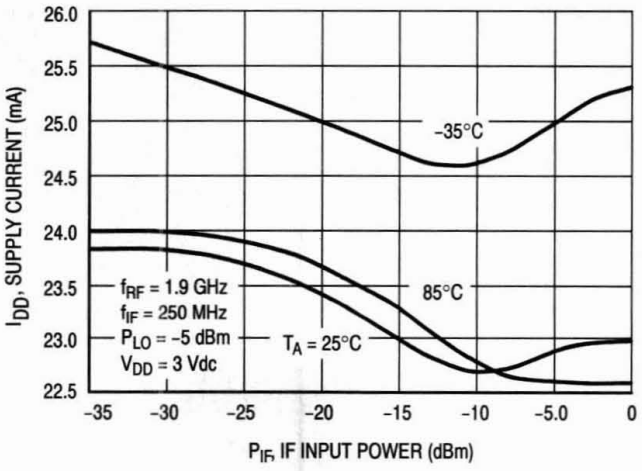


Figure 13. Supply Current versus IF Input Power

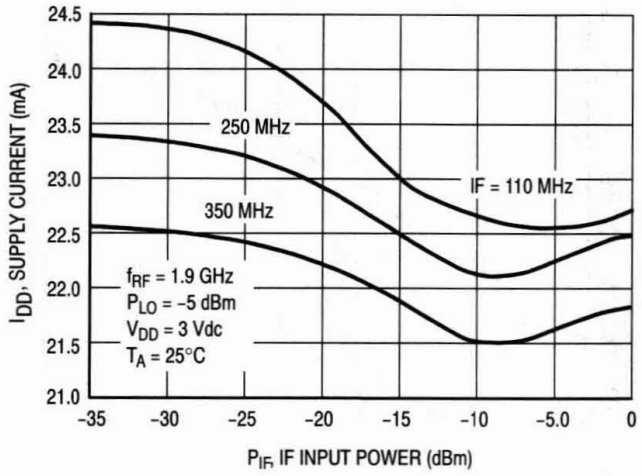


Figure 14. Supply Current versus IF Input Power

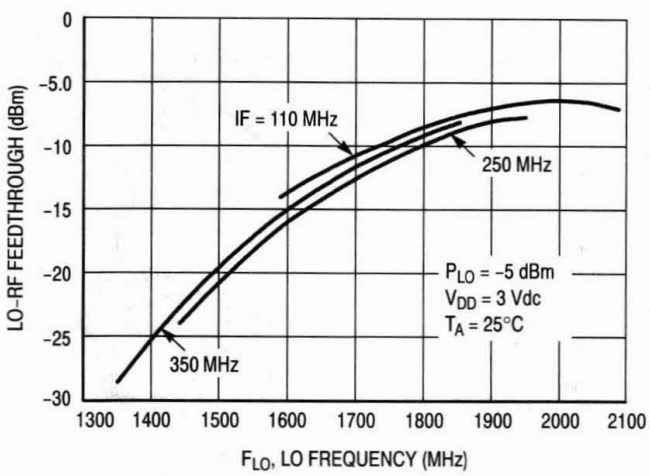


Figure 15. LO to RF Feedthrough versus LO Frequency

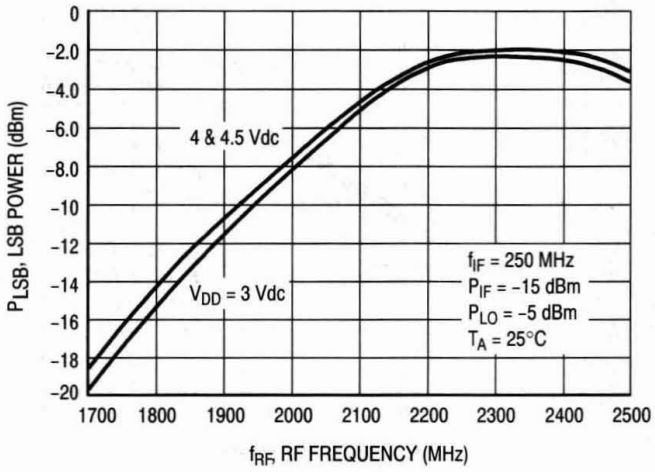


Figure 16. Lower Side Band Power versus RF Frequency

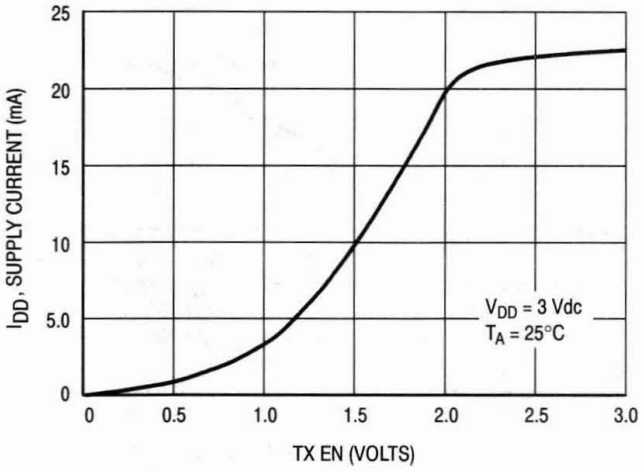


Figure 17. Supply Current versus Transmit Enable Voltage

f	IF Input		LO Input		RF Output (1)	
(MHz)	R	jX	R	jX	R	jX
70	8.3	–452.4				
100	7.3	–318.5				
150	7.1	–211.3				
200	6.6	–156.4				
250	6.5	–123.1				
300	6.1	–100.7				
350	5.7	–84.2				
1100			62.5	3.1		
1200			58.1	4.3		
1300			53.7	4.7		
1400			50.2	4.2		
1500			47.3	3.9		
1600			44.4	3.2		
1700			42.0	1.6	30.4	33.6
1800			40.6	0.5	42.6	16.9
1900			39.6	–0.7	49.1	2.3
2000			38.7	–2.2	40.6	14.2
2100			38.2	–3.6	33.8	17.7
2200			38.4	–5.1	33.3	15.7
2300			38.9	–6.5	32.9	13.7
2400			39.5	–7.8	29.6	13.2
2500					27.4	11.9

(1) Includes T1 shown in Figure 1.

Table 1. Port Impedances versus Frequency (V_{D1}, V_{D2}, V_{D3}, TX EN = 3 Vdc)

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The MRFIC1813 combines a single–balanced MESFET mixer with an exciter amplifier. It is usable for transmit frequencies from 1.7 to 2.5 GHz and IF frequencies from 70 to 350 MHz. The design is optimized for low–side local oscillator injection in hetrodyne transmit applications.

Minimal off–chip matching is required while allowing for flexibility and performance optimization. An active balun is employed at the IF port which gives good balance down to at least 70 MHz. A passive splitter is used at the LO input to complete the single–balanced configuration.

CIRCUIT CONSIDERATIONS

Figure 1 shows the application circuit used to gather the data presented in the characterization curves. As shown in Table 1, the IF port impedance is very high. Three hundred ohms was chosen for R1 to shunt the IF port as a compromise of gain and bandwidth. A 50 Ω resistor can be used and L1 and C5 eliminated to provide a broadband match. The conversion gain is reduced to about 8 dB. Microstrip inductors T1 and T2 combine with inductance internal to the device to form RF chokes. Some tuning of the RF output can be achieved with T1.

As with all RF devices, circuit layout is important. Controlled impedance lines should be used for all RF and IF interconnects. As shown in Figure 1, power supply by–passing should be used to avoid device instability. Ground vias should be included near all ground connections indicated in the schematic. Off–chip components should be mounted as close to the IC leads as possible.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" to the device type. For a complete list of currently available boards and one in development for newly introduced products, please contact your local Motorola Distributor or Sales Office.

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MRFIC1870

Product Preview

3.2 V DCS/PCS GaAs Integrated Power Amplifier

The MRFIC1870 is a single supply, RF power amplifier designed for the 2.0 W DCS/PCS handheld radios. The device is packaged in the QFN–20 package, with exposed backside pad, which allows excellent electrical and thermal performance through a solderable contact.

- Target 3.2 V Characteristics:
  RF Output Power: 32 dBm Minimum
  Efficiency: 42% Minimum
- Single Positive Supply Solution

DCS 1710 – 1785 MHz
PCS 1850 – 1910 MHz
INTEGRATED
POWER AMPLIFIER

SEMICONDUCTOR
TECHNICAL DATA

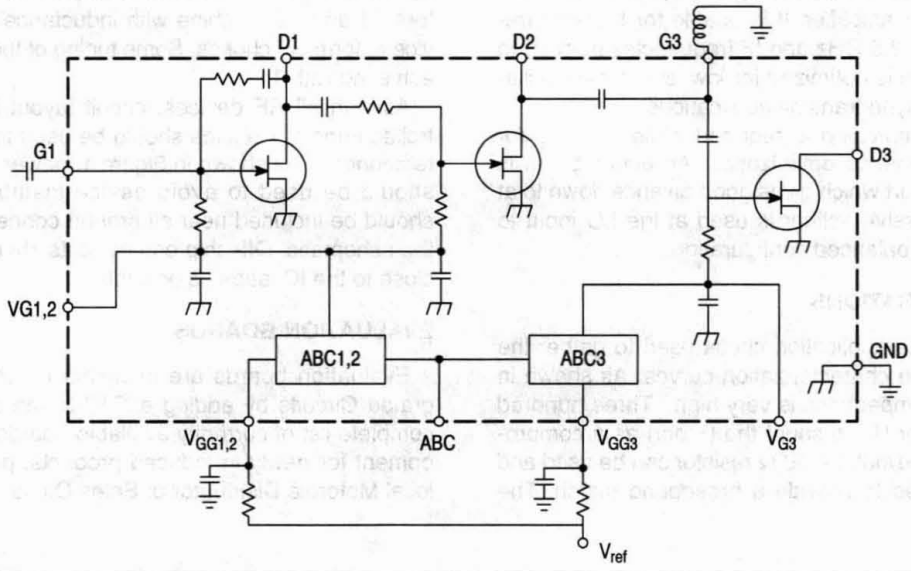
(Scale 2:1)

PLASTIC PACKAGE
CASE 1308
(QFN–20)

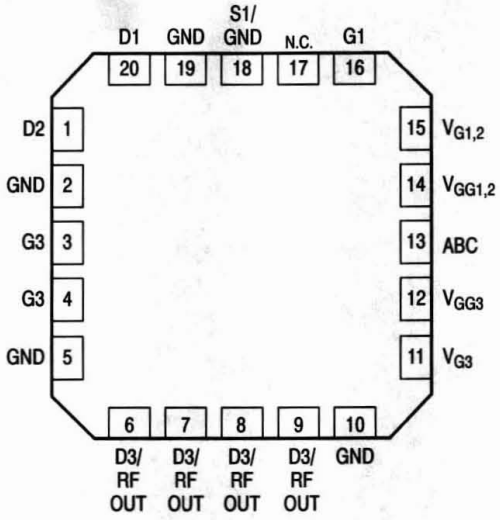
ORDERING INFORMATION

Device	Device Marking	Package
MRFIC1870	1870	QFN–20

Functional Block Diagram



CONTACT CONNECTIONS



Chapter Three
RF/IF Subsystem ICs

Section One **3.1–0**
RF/IF Subsystem ICs – Selector Guide

Section Two **3.2–0**
RF/IF Subsystem ICs – Data Sheets

Section One
Selector Guide

RF/IF Subsystems

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Miscellaneous Functions	3.1–2
ADCs/DACs	3.1–2
Encoders/Decoders	3.1–2
Packages	3.1–3

RF/IF Subsystems

Tranceivers

Product	V_{CC}	I_{CC}	GSM Receiver	TDMA/iDEN Receiver	Fractional–N PLL	Direct Launch GSM Transmitter	System Applicability	Packaging
MC13760	2.65 to 2.9 4.78 to 5.22 (Charge Pumps)	Transmit 20 mA Receive 30 mA	✓	✓	✓	✓	GSM/DCS, TDMA, iDEN, AMPS	1285/ BGA–104

Miscellaneous Functions

ADCs/DACs

Product	Function	I/O Format	Resolution	Number of Analog Channels	On–Chip Oscillator	Other Features	Suffix/ Packaging
MC144110	DAC	Serial	6 Bits	6	–	Emitter–Follower Outputs	DW/751D
MC144111				4			DW/751G

Encoders/Decoders

Product	Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Suffix/ Packaging
MC145026	Encoder	Depends on Decoder	Depends on Decoder	Depends on Decoder	Simplex	P/648, D/751B
MC145027	Decoder	5	243	4	Simplex	P/648, DW/751G
MC145028		9	19,683	0	Simplex	

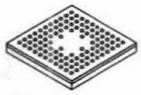
RF/IF Subsystems Packages

CASE 648
P SUFFIX
(DIP-16)

CASE 751B
D SUFFIX
(SO-16)

CASE 751D
DW SUFFIX
(SO-20L)

CASE 751G
DW SUFFIX
(SO-16W)



CASE 1285
(BGA-104)

Section Two

RF/IF Subsystems – Data Sheets

Device Number	Page Number
Transceivers	
MC13760	3.2–3
Miscellaneous Functions	
ADCs/DACs	
MC144110	3.2–8
MC144111	3.2–8
Encoders/Decoders	
MC145026	3.2–14
MC145027	3.2–14
MC145028	3.2–14

MOTOROLA
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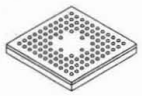
digital dna

MC13760

MULTI–PROTOCOL TRANSCEIVER

SEMICONDUCTOR TECHNICAL DATA



PLASTIC PACKAGE
CASE 1285
(BGA–104)

Product Preview

GSM/DCS/TDMA/AMPS Multi-Protocol Transceiver

The MC13760 Multi–Protocol, Multi–Band Digital Transceiver IC combines, on a single Advanced BiCMOS chip, the major building blocks required for next generation multi–purpose, multi–band wireless products. The device includes the majority of the circuitry necessary for IF signal processing between the RF front end and the DSP and backend. The MC13760 contains two fractional–N synthesizers, a re–configurable zero IF receiver with programmable bandwidth, receive A/D conversion, multi–rate data interface to the baseband DSP, direct launch digital modulator, full transmit support circuits, and general purpose support circuits such as D/A and A/D converters, battery save and tri–state control switches.

Intended for use in a combined GSM/TDMA/AMPS/iDEN portable wireless phone product in the 800/900/1800/1900 MHz bands. The MC13760 can be used over a wide range of RF and IF frequencies. The main PLL prescaler input is usable to over 2.0 GHz and the IF quadrature downconverter operates up to 400 MHz.

The MC13760 has separate receive IF inputs and a common zero–IF IQ receiver for TDMA and for GSM accommodating the receiver architectural need to use different IF frequencies and filters without the need for additional switches.

- Receiver Functions for all GSM/DCS/TDMA IS–136/AMPS Modes and Frequencies Including GPRS
- Direct Interface to Motorola Baseband Processors, such as the DSP56690 through a Common Programming and Data Interface
- Main Three Accumulator (24–Bit) Fractional–N Synthesizer
  - Resolution Capability of 6.0 Hz
  - Dual–Mode Charge Pump Output for TDMA TX VCO and all RX
  - Independent Charge Pump Output for the GSM/DCS TX VCO
  - GMSK Lookup ROM for Direct Transmission in GSM/DCS Mode
  - Digital 16–Bit Automatic Frequency Control
- Secondary Three Accumulator (24–Bit) Fractional–N Synthesizer for use as an Accurate Frequency–Corrected Clock in GSM, or as an Additional Low Frequency LO
- Coarse Tuning of the VCO(s) via a 6–Bit D/A with Adapt
- Operates at 2.75 V Deep Sleep Mode with Current as low as 50 μA
- Versatile Frequency Generation including Linear and Constant Envelope Modulation Paths, Ramp and Power Level Control, Direct Gain Control of the RFPA in the TDMA Mode
- D/A Conversion of TDMA TXI and TXQ
- Reference Crystal Oscillator with a Buffered Output, Compensation/Fine Tuning via 9–Bit D/A
- Receiver Gain Adjustment and Bandwidth Down to 6.0 kHz Programmed over the SPI Bus
- A/D Conversion of RXI and RXQ to 8–Bit or 10–Bit Resolution
- Types of Applications
  - GSM/DCS/TDMA/AMPS Global Roaming Multiband Cellular Telephone
  - VHF/UHF 2–Way or Trunked Radio, iDEN, Tetra, or Satellite Communication Radios or Telephones
  - Hand–Held Wireless PDA's
  - Wireless LAN's, Industrial Devices, ISM Band Products
  - Any New Device Containing Some Combination of the Above Functions

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13760	T_A = –40 to 85°C	BGA–104

Figure 1. MC13760 Detailed Block Diagram

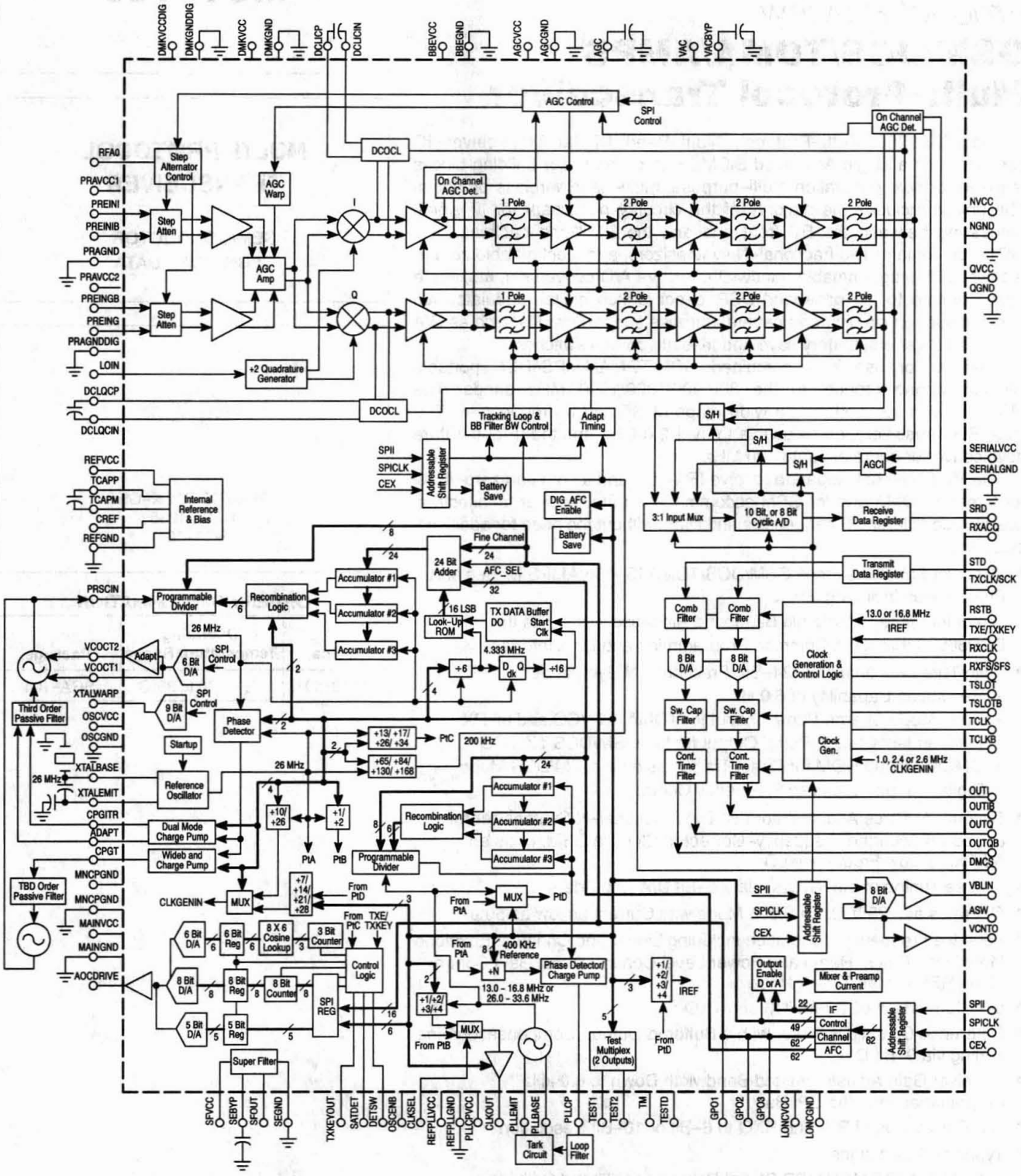


Table 1. BGA Contact Identification

BALL #	BALL NAME	DESCRIPTION	SIGNAL TYPE
A1	PRAGNDDIG	Ground for the preamp substrate.	Ground
A2	PRAGND	Ground for the preamp.	Ground
A3	PREINGB	GSM IF preamp input.	RF Input
A4	PREINIB	TDMA IF preamp input.	RF Input
A5	BBFGND	Ground for the baseband filters.	Ground
A6	DCLQCP	DC Offset Correction Loop (input) capacitor – Q channel	Analog Input
A7	CREF	Bypass capacitor for the bandgap regulator.	Analog
A8	OUTQ	TDMA Q channel analog transmit data.	Analog Output
A9	OUTIB	TDMA I channel analog transmit data.	Analog Output
A10	TSLOTB	TDMA low level transmit slot.	Analog Output
A11	TSLOT	TDMA low level transmit slot.	Analog Output
B1	RFA0	RF attenuator 0 control line. (This line is a driver for an external RF attenuator.)	Digital Output
B2	DMXGND	Ground for the mixer.	Ground
B3	PREING	GSM IF preamp input.	RF Input
B4	PREINI	TDMA IF preamp input.	RF Input
B5	PRAVCC2	Supply for the preamp output stage.	Supply 2.775 V
B6	DCLICP	DC Offset Correction Loop (input) capacitor – I channel	Analog Input
B7	GPO3/test_so2	SPI port expansion 3. Or scan data output for MODROM module.	Digital Output
B8	TCAPP	Differential reference capacitor.	Analog
B9	REFGND	Ground for the internal reference.	Ground
B10	REFVCC	Supply for the internal reference.	Supply 2.775 V
B11	TCLK	TDMA low level transmit clock.	Analog Output
C1	DMXVCC	Supply for the mixer.	Supply 2.775 V
C2	DMXGNDDIG	Ground for the mixer substrate and quadrature generator.	Ground
C3	PRAVCC1	Supply for the preamp.	Supply 2.775 V
C4	BBFVCC	Supply for the baseband filters.	Supply 2.775 V
C5	DCLICIN	DC Offset Correction Loop (output) capacitor – TDMA – I channel	Analog Output
C6	DCLQCIN	DC Offset Correction Loop (output) capacitor – TDMA – Q channel	Analog Output
C7	TCAPM	Differential reference capacitor.	Analog
C8	OUTQB	TDMA Q channel analog transmit data.	Analog Output
C9	CLKSEL	Selects the source for the clock output to the digital circuitry of the radio as either the crystal reference/divided crystal reference or the Step Up PLL/divided Step Up PLL. A low on this pin selects the crystal reference/divided crystal reference. A high on this pin selects the Step Up PLL/divided Step Up PLL. Integrated weak pulldown.	Digital Input
C10	TCLKB	TDMA low level transmit clock.	Analog Output
C11	QGND	Quiet analog ground for the PA D/A and the data processing circuits.	Ground
D1	LOIN	Input port for the second LO VCO signal.	RF Input
D2	DMXVCCDIG	Supply for the quadrature generator.	Supply 2.775 V
D3	TEST2/EERQ	Test input/MUX 2 output. (Various signals are buffered and MUX'd to this pin. Output signal is determined by programming of test bits.) Or with EER active, TDMA Q channel transmit data.	Analog Test Point
D4	TEST1/EERI	Test input/MUX 1 output. (Various signals are buffered and MUX'd to this pin. Output signal is determined by programming of test bits.) Or with EER active, TDMA I channel transmit data.	Analog Test Point
D6	PKGGND1	Ground for the package flag (no direct connection to die).	Pkg Ground
D8	OUTI	TDMA I channel analog transmit data.	Analog Output

Table 1. BGA Contact Identification (continued)

BALL #	BALL NAME	DESCRIPTION	SIGNAL TYPE
D9	TESTD/GPO4	Digital test point. (Various digital signals are MUX'd to this pin. Output is determined by programming of test bits.) Or SPI port expansion 4.	Digital Test Point Digital Output
D10	QVCC	Quiet analog supply for the PA D/A and the data processing circuits.	Supply 2.775 V
D11	NGND	Noisy analog ground for the VCO D/A, AOC D/A and the data processing circuits.	Ground
E1	VAG	Analog ground.	Analog
E2	AGCGND	Ground for the AGC.	Ground
E3	VAGBYP	Bypass capacitor for the analog ground voltage.	Analog
E9	NVCC	Noisy analog supply for the VCO D/A, AOC D/A and the data processing circuits.	Supply 2.775 V
E10	RSTB	Reset. Low true input. Integrated weak pullup.	Digital Input
E11	TM	Enable for the internal scan test.	Digital Input
F1	AGCVCC	Supply for the AGC.	Supply 2.775 V
F2	TXKEYOUT/test_so4	Conditioned TXKEY out. Or scan data output for reference clock module.	Digital Output
F3	AGC	Capacitor for the TDMA AGC.	Analog
F4	PKGGND2	Ground for the package flag (no direct connection to die).	Pkg Ground
F8	PKGGND3	Ground for the package flag (no direct connection to die).	Pkg Ground
F9	PLLCPVCC	Supply for the Step Up PLL phase detector and charge pump.	Supply 5.0 V
F10	CLKOUT	Clock output to the digital circuitry of the radio. Ranges are 13.0 to 16.8 MHz, or 26.0 to 33.6 MHz. The actual frequency provided will depend upon the configuration of the Step Up PLL and the SPI selected configuration of the MC13760.	Analog Output
F11	PLLCP	Charge pump output for the Step Up PLL.	Analog Output
G1	PRSCIN	Main LO prescaler input.	RF Input
G2	MAINGND	Ground for the main prescaler and divider.	Ground
G3	AOCDRIVE	Output to the PA bias circuitry drive input. (Output drive impedance is 620 Ohms.)	Analog Output
G9	PLLEMIT	Emitter of the oscillator transistor for the Step Up PLL.	RF Output
G10	REFPLLVCC	Supply for the Step Up PLL VCO and dividers.	Supply 2.775 V
G11	PLLBASE/vco_clk	Base of the oscillator transistor for the Step Up PLL. Or scan clock input for VCO clock zone.	RF Input
H1	SATDET/test_si4	Input indicating saturation. Or scan data input for reference clock module.	Digital Input
H2	GPO2/test_so8	SPI port expansion 2. Or Main PLL Adapt Timer output. Or scan data output for SSI module.	Digital Output
H3	MAINVCC	Supply for the main prescaler and divider.	Supply 2.775 V
H4	MNCPVCC	Supply for the main phase detector and charge pump.	Supply 5.0 V
H6	PKGGND4	Ground for the package flag (no direct connection to die).	Pkg Ground
H8	TXE/TXKEY/test_si8	Transmit slot enable in TDMA mode; digital input to start/stop the PA Control sequence in GSM mode. Or scan data input for SSI module.	Digital Input
H9	RXACQ/test_si7	Serial bus enable. Or scan data input for 5 bit and 8 bit xtal clock dividers.	Digital Input
H10	REFPLLGND	Ground for the Step Up PLL.	Ground
H11	SERIALVCC	Supply for the SSI and SPI serial communication ports.	Supply 1.8 — 2.775V
J1	GPO1/test_so1	SPI port expansion 1. Or Coarse Tune Adapt Timer output. Or scan data output for main Frac–N.	Digital Output
J2	VCOCT2	High current (ADAPT) output of the 6 bit main RX VCO Coarse Tune D/A.	Analog Output
J3	DETSW/test_si1	Output to the PA control circuitry power range input (open drain). Or scan data input for main Frac–N.	Analog Output

Table 1. BGA Contact Identification (continued)

BALL #	BALL NAME	DESCRIPTION	SIGNAL TYPE
J4	SFVCC	Supply for the super filter.	Supply 2.775 V
J5	ASW/sc_inp1	TDMA antenna switch control input. Or scan data input for reference clock Frac–N accumulator module.	Digital Input
J6	VCNTO	TDMA RFPA gain control voltage output.	Analog Output
J7	OSCVCC	Supply for the crystal oscillator.	Supply 2.775 V
J8	XTALWARP	Output of the 9 bit WARP D/A to be used for compensation/correction of the reference crystal frequency.	Analog Output
J9	OSCENB	Digital input used to control the crystal oscillator circuit. A logic low selects the internal oscillator. Integrated weak pulldown.	Digital Input
J10	RXCLK/test_so3	SSI RX clock in GSM mode; not used in TDMA mode. Or scan data output for transmit power amp control module.	Digital Output
J11	SRD/test_so6	SSI receive data. Or scan data output for Adapt Generator module.	Digital Output
K1	VCOCT1	Low current output of the 6 bit main RX VCO Coarse Tune D/A.	Analog Output
K2	MNCPGND	Ground for the main phase detector and charge pump.	Ground
K3	SFGND	Ground for the super filter.	Ground
K4	SFBYP	Bypass capacitor for the super filter. (1.0 µf)	Analog
K5	OSCGND	Ground for the crystal oscillator.	Ground
K6	XTALBASE/sc_clk26	Crystal oscillator base. Or scan clock input for xtal clock zone.	RF Input
K7	LOGICVCC	Supply for the main synthesizer logic, adapt control and test MUXs.	Supply 2.775 V
K8	CEX	Digital input that latches in the SPI data. (Low Active)	Digital Input
K9	SPICLK	SPI clock input.	Digital Input
K10	STD/test_si3	SSI transmit data. Or scan data input for transmit.	Digital Input
K11	TXCLK/SCK/test_so5	Bit clock for TX data transfer in GSM mode. Bit clock for RX and TX data transfer in TDMA mode. Or scan data output for reference clock Frac–N accumulator module.	Digital Output
L1	ADAPT	Synthesizer output to adapt the loop filter for the main PLL.	Analog Output
L2	CPGT	Charge pump output for the main TX LO (GSM).	Analog Output
L3	CPGITR	Charge pump output for the main RX LO (GSM, TDMA TX and RX).	Analog Output
L4	SFOUT	Super filter output. (45 mA max) (bypass with 0.01 µf)	Analog Output
L5	VBLIN	TDMA RFPA bias control voltage output.	Analog Output
L6	XTALEMIT	Crystal oscillator emitter.	RF Output
L7	LOGICGND	Ground for the main synthesizer logic, adapt control and test MUXs.	Ground
L8	SERIALGND	Ground for the SSI and SPI serial communication ports.	Ground
L9	SPII	SPI data input.	Digital Input
L10	DMCS/test_si2	Digital input that starts the GSM TX modulation. Or scan data input for MODROM module.	Digital Input
L11	RXFS/SFS/test_so7	RX SSI frame sync in GSM mode; SSI frame sync in TDMA mode. Or scan data output for 5 bit and 8 bit xtal clock dividers.	Digital Output

MC144110
MC144111

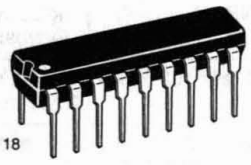
Digital-to-Analog Converters with Serial Interface
CMOS LSI

The MC144110 and MC144111 are low–cost 6–bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

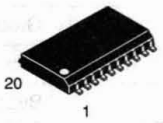
Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 V supply range, these DACs may be directly interfaced to CMOS MPUs operating at 5 V.

- Direct R–2R Network Outputs
- Buffered Emitter–Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS µP
- Wide Operating Voltage Range: 4.5 to 15 V
- Wide Operating Temperature Range: 0 to 85°C
- Software Information is Contained in Document M68HC11RM/AD

MC144110

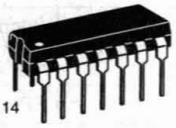


P SUFFIX
PLASTIC DIP
CASE 707

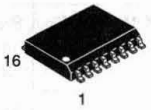


DW SUFFIX
SOG PACKAGE
CASE 751D

MC144111



P SUFFIX
PLASTIC DIP
CASE 646

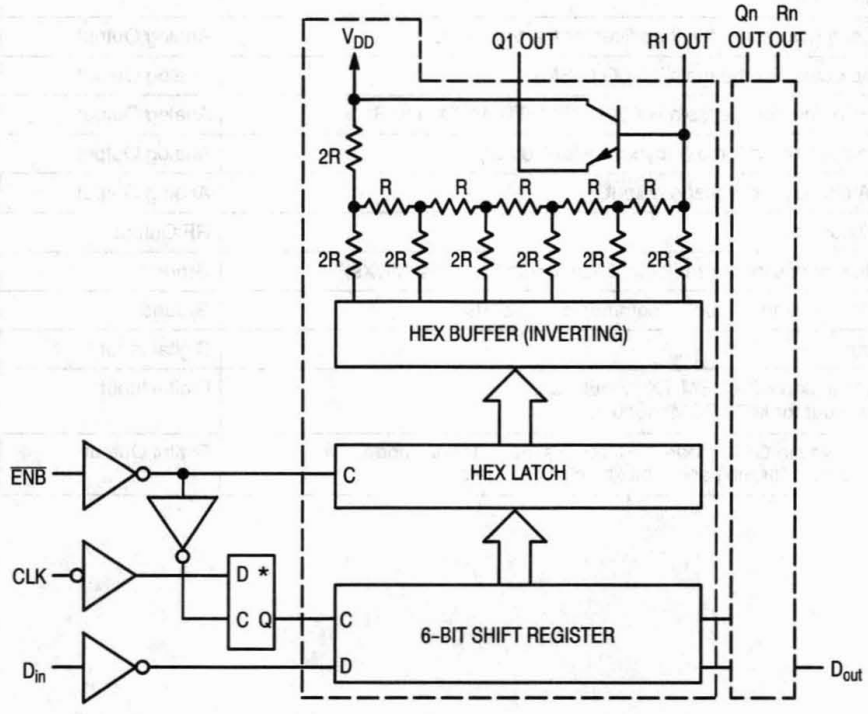


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC144110P	Plastic DIP
MC144110DW	SOG Package
MC144111P	Plastic DIP
MC144111DW	SOG Package

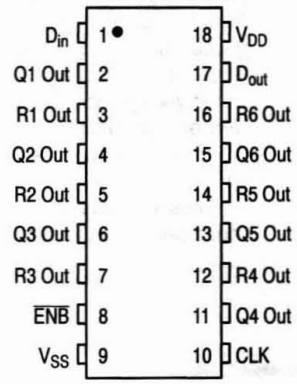
BLOCK DIAGRAM



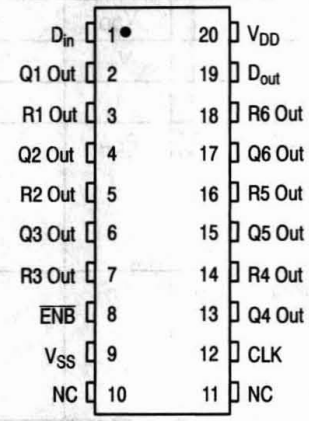
* Transparent Latch

PIN ASSIGNMENTS

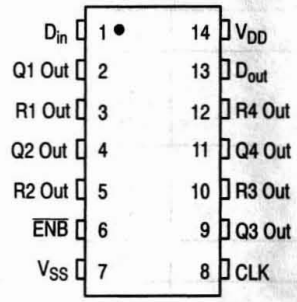
MC144110P



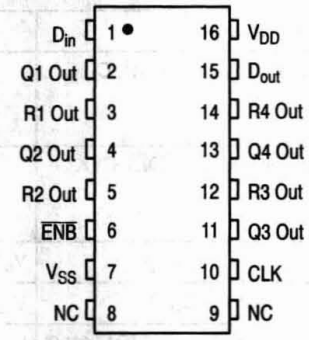
MC144110DW



MC144111P



MC144111DW



NC = NO CONNECTION

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Power Dissipation (Per Output) T_A = 70°C, MC144110 MC144111 T_A = 85°C, MC144110 MC144111	P_{OH}	 30 50 10 20	mW
Power Dissipation (Per Package) T_A = 70°C, MC144110 MC144111 T_A = 85°C, MC144110 MC144111	P_D	 100 150 25 50	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields; however, it is advised that precautions be taken to avoid application of voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

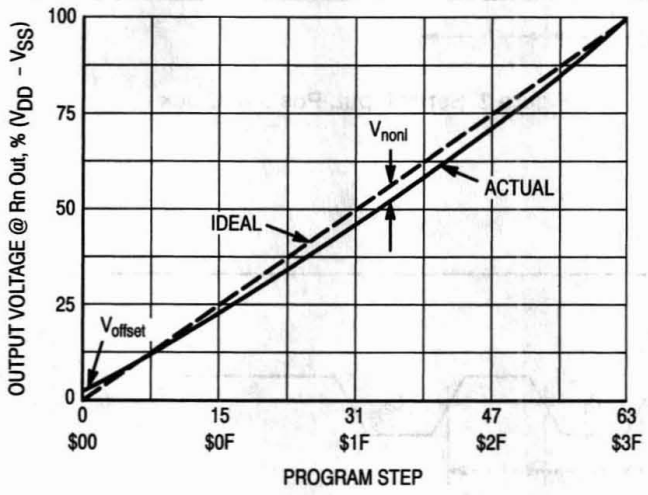
ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS}, T_A = 0 to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{IH}	High–Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		5 10 15	3.0 3.5 4	— — —	V
V_{IL}	Low–Level Input Voltage (D_{in}, $\overline{ENB}$, CLK)		5 10 15	— — —	0.8 0.8 0.8	V
I_{OH}	High–Level Output Current (D_{out})	$V_{out} = V_{DD} - 0.5$ V	5	– 200	—	µA
I_{OL}	Low–Level Output Current (D_{out})	V_{out} = 0.5 V	5	200	—	µA
I_{DD}	Quiescent Supply Current MC144110 MC144111	I_{out} = 0 µA	15 15	— —	12 8	mA
I_{in}	Input Leakage Current (D_{in}, $\overline{ENB}$, CLK)	$V_{in} = V_{DD}$ or 0 V	15	—	± 1	µA
V_{nonl}	Nonlinearity Voltage (Rn Out)	See Figure 1	5 10 15	— — —	100 200 300	mV
V_{step}	Step Size (Rn Out)	See Figure 2	5 10 15	19 39 58	137 274 411	mV
V_{offset}	Offset Voltage from V_{SS}	D_{in} = $00, See Figure 1	—	—	1	LSB
I_E	Emitter Leakage Current	$V_{Rn\ Out}$ = 0 V	15	—	10	µA
h_{FE}	DC Current Gain	I_E = 0.1 to 10.0 mA T_A = 25°C	—	40	—	—
V_{BE}	Base–to–Emitter Voltage Drop	I_E = 1.0 mA	—	0.4	0.7	V

SWITCHING CHARACTERISTICS

(Voltages referenced to V_{SS}, T_A = 0 to 85°C, C_L = 50 pF, Input $t_r = t_f$ = 20 ns unless otherwise indicated)

Symbol	Parameter	V_{DD}	Min	Max	Unit
t_{wH}	Positive Pule Width, CLK (Figures 3 and 4)	5 10 15	2 1.5 1	— — —	µs
t_{wL}	Negative Pulse Width, CLK (Figure 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_{su}	Setup Time, $\overline{ENB}$ to CLK (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_{su}	Setup Time, D_{in} to CLK (Figures 3 and 4)	5 10 15	1000 750 500	— — —	ns
t_h	Hold Time, CLK to $\overline{ENB}$ (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_h	Hold Time, CLK to D_{in} (Figures 3 and 4)	5 10 15	5 3.5 2	— — —	µs
t_r, t_f	Input Rise and Fall Times	5 – 15	—	2	µs
C_{in}	Input Capacitance	5 – 15	—	7.5	pF



LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst–case deviation of linearity of the actual transfer function from the best–fit straight line. It is normally specified in parts of an LSB.

Figure 1. D/A Transfer Function

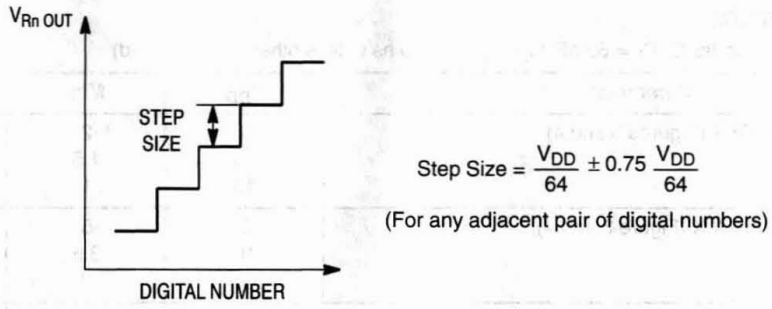


Figure 2. Definition of Step Size

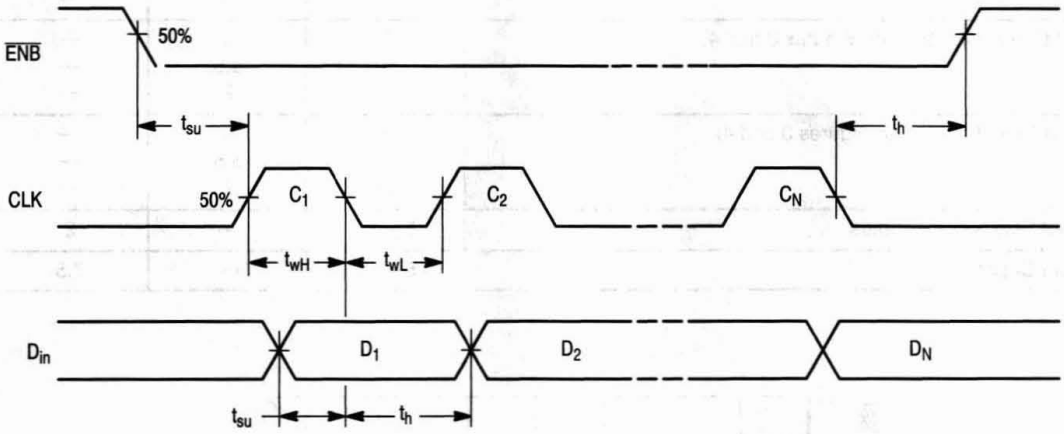


Figure 3. Serial Input, Positive Clock

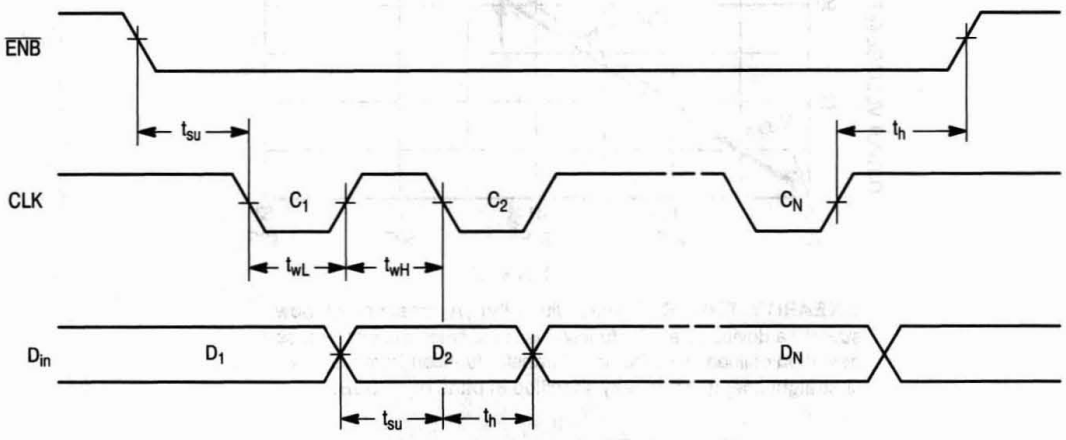


Figure 4. Serial Input, Negative Clock

PIN DESCRIPTIONS

INPUTS

D_{in}
Data Input

Six–bit words are entered serially, MSB first, into digital data input, D_{in}. Six words are loaded into the MC144110 during each D/A cycle; four words are loaded into the MC144111.

The last 6–bit word shifted in determines the output level of pins Q1 Out and R1 Out. The next–to–last 6–bit word affects pins Q2 Out and R2 Out, etc.

$\overline{ENB}$
Negative Logic Enable

The $\overline{ENB}$ pin must be low (active) during the serial load. On the low–to–high transition of $\overline{ENB}$, data contained in the shift register is loaded into the latch.

CLK
Shift Register Clock

Data is shifted into the register on the high–to–low transition of CLK. CLK is fed into the D–input of a transparent latch, which is used for inhibiting the clocking of the shift register when $\overline{ENB}$ is high.

The number of clock cycles required for the MC144110 is usually 36. The MC144111 usually uses 24 cycles. See Table 1 for additional information.

OUTPUTS

D_{out}
Data Output

The digital data output is primarily used for cascading the DACs and may be fed into D_{in} of the next stage.

R1 Out through Rn Out
Resistor Network Outputs

These are the R–2R resistor network outputs. These outputs may be fed to high–impedance input FET op amps to bypass the on–chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 kΩ.

Q1 Out through Qn Out
NPN Transistor Outputs

Buffered DAC outputs utilize an emitter–follower configuration for current–gain, thereby allowing interface to low–impedance circuits.

SUPPLY PINS

V_{SS}
Negative Supply Voltage

This pin is usually ground.

V_{DD}
Positive Supply Voltage

The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 V p–p.

Table 1. Number of Channels vs Clocks Required

Number of Channels Required	Number of Clock Cycles	Outputs Used on MC144110	Outputs Used on MC144111
1	6	Q1/R1	Q1/R1
2	12	Q1/R1, Q2/R2	Q1/R1, Q2/R2
3	18	Q1/R1, Q2/R2, Q3/R3	Q1/R1, Q2/R2, Q3/R3
4	24	Q1/R1, Q2/R2, Q3/R3, Q4/R4	Q1/R1, Q2/R2, Q3/R3, Q4/R4
5	30	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5	Not Applicable
6	36	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5, Q6/R6	Not Applicable

Encoder and Decoder Pairs
CMOS

MC145026
MC145027
MC145028

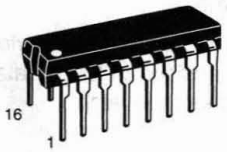
These devices are designed to be used as encoder/decoder pairs in remote control applications.

The MC145026 encodes nine lines of information and serially sends this information upon receipt of a transmit enable ($\overline{TE}$) signal. The nine lines may be encoded with trinary data (low, high, or open) or binary data (low or high). The words are transmitted twice per encoding sequence to increase security.

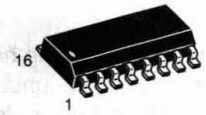
The MC145027 decoder receives the serial stream and interprets five of the trinary digits as an address code. Thus, 243 addresses are possible. If binary data is used at the encoder, 32 addresses are possible. The remaining serial information is interpreted as four bits of binary data. The valid transmission (VT) output goes high on the MC145027 when two conditions are met. First, two addresses must be consecutively received (in one encoding sequence) which both match the local address. Second, the 4 bits of data must match the last valid data received. The active VT indicates that the information at the Data output pins has been updated.

The MC145028 decoder treats all nine trinary digits as an address which allows 19,683 codes. If binary data is encoded, 512 codes are possible. The VT output goes high on the MC145028 when two addresses are consecutively received (in one encoding sequence) which both match the local address.

- Operating Temperature Range: – 40 to + 85°C
- Very–Low Standby Current for the Encoder: 300 nA Maximum @ 25°C
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- RC Oscillator, No Crystal Required
- High External Component Tolerance; Can Use ± 5% Components
- Internal Power–On Reset Forces All Decoder Outputs Low
- Operating Voltage Range: MC145026 = 2.5 to 18 V*
  MC145027, MC145028 = 4.5 to 18 V
- For Infrared Applications, See Application Note AN1016/D



P SUFFIX
PLASTIC DIP
CASE 648



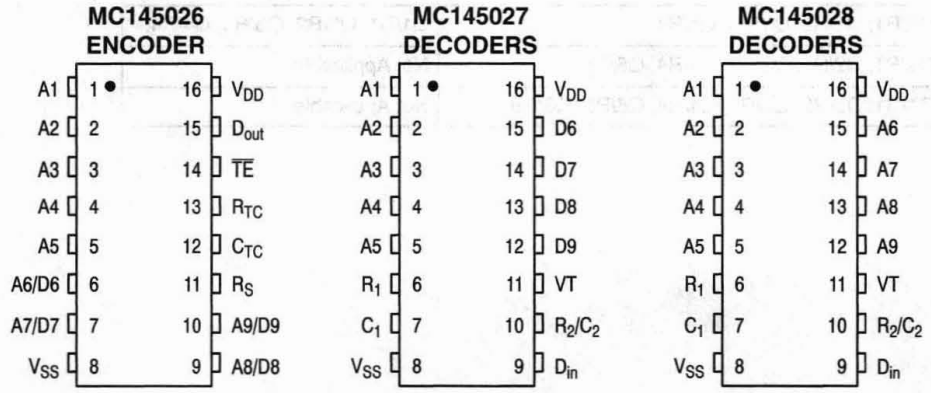
D SUFFIX
SOG PACKAGE
CASE 751B

DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC145026P	Plastic DIP
MC145026D	SOG Package
MC145027P	Plastic DIP
MC145027DW	SOG Package
MC145028P	Plastic DIP
MC145028DW	SOG Package

PIN ASSIGNMENTS



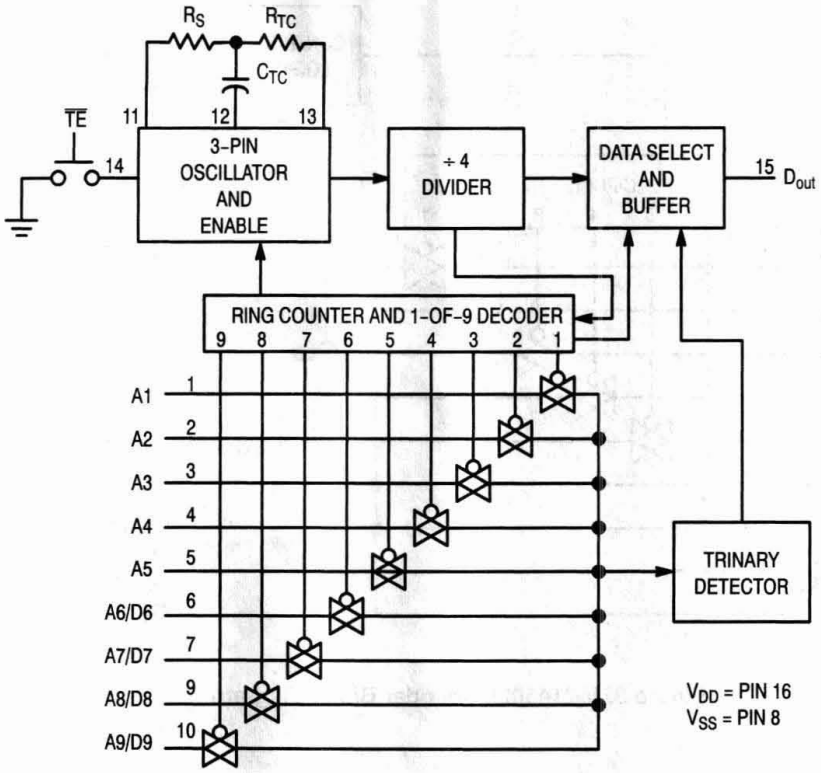


Figure 1. MC145026 Encoder Block Diagram

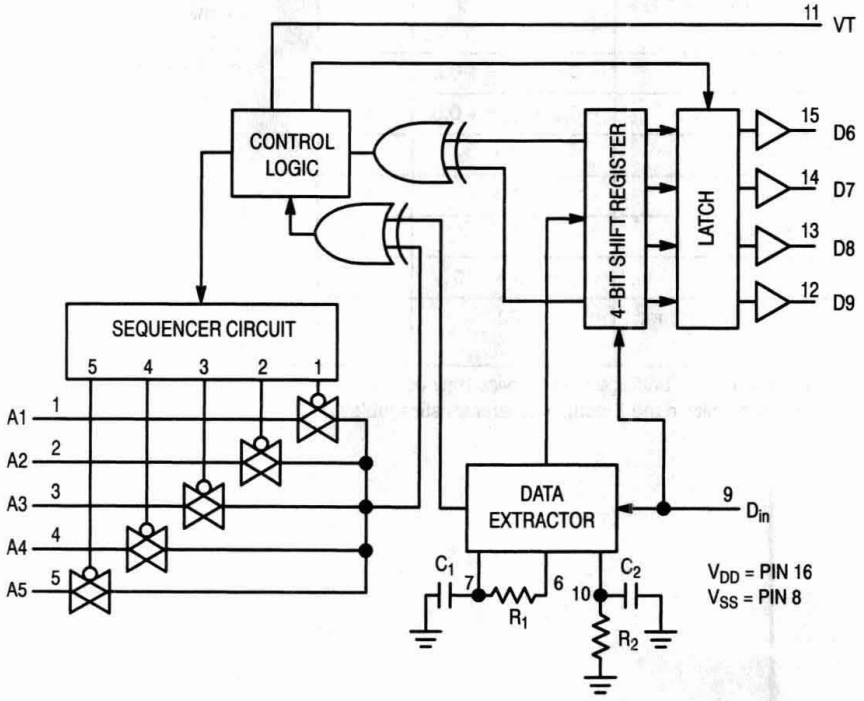


Figure 2. MC145027 Decoder Block Diagram

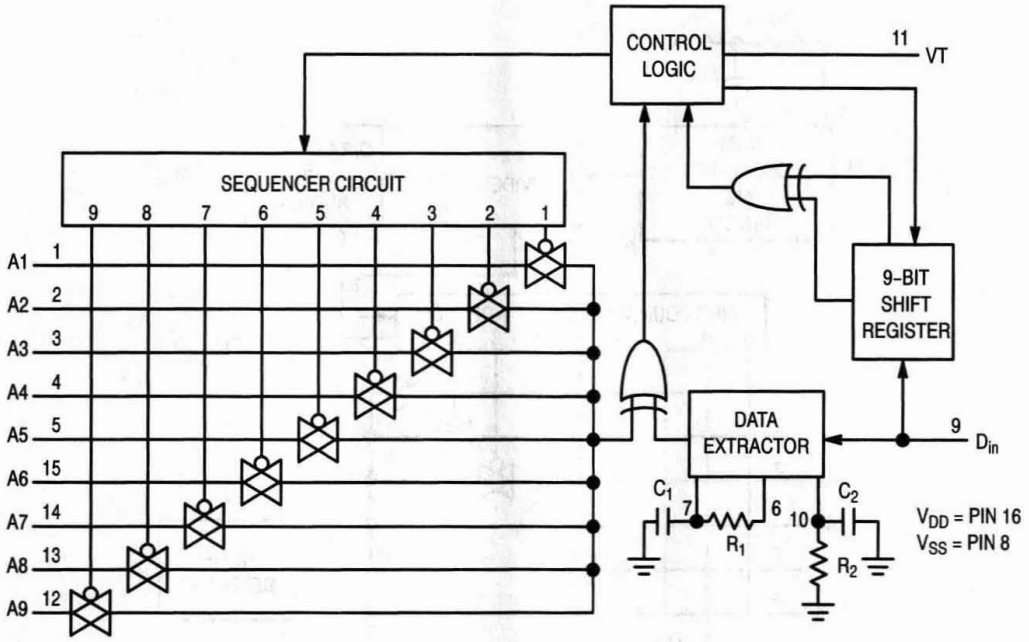


Figure 3. MC145028 Decoder Block Diagram

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
V_{DD}	DC Supply Voltage (except SC41343, SC41344)	– 0.5 to + 18	V
V_{DD}	DC Supply Voltage (SC41343, SC41344 only)	– 0.5 to + 10	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS — MC145026*, MC145027, and MC145028 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = V_{DD} or 0)	5.0	—	0.05	—	0.05	—	0.05	V
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V_{OH}	High–Level Output Voltage (V_{in} = 0 or V_{DD})	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
V_{IL}	Low–Level Input Voltage								V
	(V_{out} = 4.5 or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
	(V_{out} = 13.5 or 1.5 V)	15	—	4.0	—	4.0	—	4.0	
V_{IH}	High–Level Input Voltage								V
	(V_{out} = 0.5 or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
	(V_{out} = 1.5 or 13.5 V)	15	11	—	11	—	11	—	
I_{OH}	High–Level Output Current								mA
	(V_{out} = 2.5 V)	5.0	– 2.5	—	– 2.1	—	– 1.7	—	
	(V_{out} = 4.6 V)	5.0	– 0.52	—	– 0.44	—	– 0.36	—	
	(V_{out} = 9.5 V)	10	– 1.3	—	– 1.1	—	– 0.9	—	
	(V_{out} = 13.5 V)	15	– 3.6	—	– 3.0	—	– 2.4	—	
I_{OL}	Low–Level Output Current								mA
	(V_{out} = 0.4 V)	5.0	0.52	—	0.44	—	0.36	—	
	(V_{out} = 0.5 V)	10	1.3	—	1.1	—	0.9	—	
	(V_{out} = 1.5 V)	15	3.6	—	3.0	—	2.4	—	
I_{in}	Input Current — $\overline{TE}$	5.0	—	—	3.0	11	—	—	µA
	(MC145026, Pull–Up Device)	10	—	—	16	60	—	—	
		15	—	—	35	120	—	—	
I_{in}	Input Current	15	—	± 0.3	—	± 0.3	—	± 1.0	µA
	R_S (MC145026), D_{in} (MC145027, MC145028)								
I_{in}	Input Current								µA
	A1 – A5, A6/D6 – A9/D9 (MC145026),	5.0	—	—	—	± 110	—	—	
	A1 – A5 (MC145027),	10	—	—	—	± 500	—	—	
	A1 – A9 (MC145028)	15	—	—	—	± 1000	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current — MC145026	5.0	—	—	—	0.1	—	—	µA
		10	—	—	—	0.2	—	—	
		15	—	—	—	0.3	—	—	
I_{DD}	Quiescent Current — MC145027, MC145028	5.0	—	—	—	50	—	—	µA
		10	—	—	—	100	—	—	
		15	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current — MC145026	5.0	—	—	—	200	—	—	µA
	(f_c = 20 kHz)	10	—	—	—	400	—	—	
		15	—	—	—	600	—	—	
I_{dd}	Dynamic Supply Current — MC145027, MC145028	5.0	—	—	—	400	—	—	µA
	(f_c = 20 kHz)	10	—	—	—	800	—	—	
		15	—	—	—	1200	—	—	

* Also see next Electrical Characteristics table for 2.5 V specifications.

ELECTRICAL CHARACTERISTICS — MC145026 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			– 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	—	0.05	—	0.05	—	0.05	V
V_{OH}	High–Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	2.45	—	2.45	—	2.45	—	V
V_{IL}	Low–Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	—	0.3	—	0.3	—	0.3	V
V_{IH}	High–Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	2.2	—	2.2	—	2.2	—	V
I_{OH}	High–Level Output Current (V_{out} = 1.25 V)	2.5	0.28	—	0.25	—	0.2	—	mA
I_{OL}	Low–Level Output Current (V_{out} = 0.4 V)	2.5	0.22	—	0.2	—	0.16	—	mA
I_{in}	Input Current ($\overline{TE}$ — Pull–Up Device)	2.5	—	—	0.09	1.8	—	—	µA
I_{in}	Input Current (A1–A5, A6/D6–A9/D9)	2.5	—	—	—	± 25	—	—	µA
I_{DD}	Quiescent Current	2.5	—	—	—	0.05	—	—	µA
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.5	—	—	—	40	—	—	µA

SWITCHING CHARACTERISTICS — MC145026*, MC145027, and MC145028 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4,8	5.0 10 15	— — —	200 100 80	ns
t_r	D_{in} Rise Time — Decoders	5	5.0 10 15	— — —	15 15 15	µs
t_f	D_{in} Fall Time — Decoders	5	5.0 10 15	— — —	15 5.0 4.0	µs
f_{osc}	Encoder Clock Frequency	6	5.0 10 15	0.001 0.001 0.001	2.0 5.0 10	MHz
f	Decoder Frequency — Referenced to Encoder Clock	12	5.0 10 15	1.0 1.0 1.0	240 410 450	kHz
t_w	$\overline{TE}$ Pulse Width — Encoders	7	5.0 10 15	65 30 20	— — —	ns

* Also see next Switching Characteristics table for 2.5 V specifications.

SWITCHING CHARACTERISTICS — MC145026 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	2.5	—	450	ns
f_{osc}	Encoder Clock Frequency	6	2.5	1.0	250	kHz
t_w	$\overline{TE}$ Pulse Width	7	2.5	1.5	—	µs

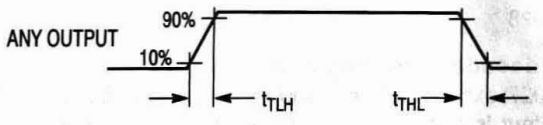


Figure 4.

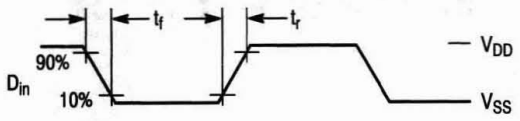


Figure 5.

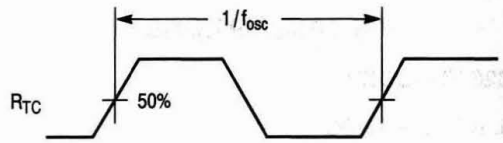


Figure 6.

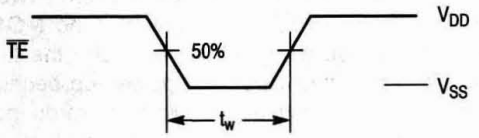
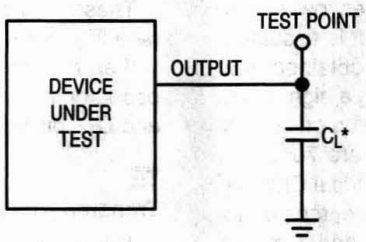


Figure 7.



* Includes all probe and fixture capacitance.

Figure 8. Test Circuit

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits trinary data as defined by the state of the A1 – A5 and A6/D6 – A9/D9 input pins. These pins may be in either of three states (low, high, or open) allowing 19,683 possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Upon power–up, the MC145026 can continuously transmit as long as $\overline{TE}$ remains low (also, the device can transmit two–word sequences by pulsing $\overline{TE}$ low). However, no MC145026 application should be designed to rely upon the first data word transmitted immediately after power–up because this word may be invalid. Between the two data words, no signal is sent for three data periods (see Figure 10).

Each transmitted trinary digit is encoded into pulses (see Figure 11). A logic 0 (low) is encoded as two consecutive short pulses, a logic 1 (high) as two consecutive long pulses, and an open (high impedance) as a long pulse followed by a short pulse. The input state is determined by using a weak "output" device to try to force each input high then low. If only a high state results from the two tests, the input is assumed to be hardwired to V_{DD}. If only a low state is obtained, the input is assumed to be hardwired to V_{SS}. If both a high and a low can be forced at an input, an open is assumed and is encoded as such. The "high" and "low" levels are 70% and 30% of the supply voltage as shown in the Electrical Characteristics table. The weak "output" device sinks/sources up to 110 μA at a 5 V supply level, 500 μA at 10 V, and 1 mA at 15 V.

The $\overline{TE}$ input has an internal pull–up device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high and the second–word transmission has timed out, the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the D_{out} pin.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical words, is examined bit by bit during reception. The first five trinary digits are assumed to be the address. If the received address matches the local address, the next four (data) bits are internally stored, but are not transferred to the output data latch. As the second encoded word is received, the address must again match. If a match occurs, the new data bits are checked against the previously stored data bits. If the two nibbles of data (four bits each) match, the data is transferred to the output data latch by VT and remains until new data replaces it. At the same time, the VT output pin is brought high and remains high until an error is received or until no input signal is received for four data periods (see Figure 10).

Although the address information may be encoded in trinary, the data information must be either a 1 or 0. A trinary (open) data line is decoded as a logic 1.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address lines are used and no data output is available. The VT output is used to indicate that a valid address has been received. For transmission security, two identical transmitted words must be consecutively received before a VT output signal is issued.

The MC145028 allows 19,683 addresses when trinary levels are used. 512 addresses are possible when binary levels are used.

PIN DESCRIPTIONS

MC145026 ENCODER

A1 – A5, A6/D6 – A9/D9
Address, Address/Data Inputs (Pins 1 – 7, 9, and 10)

These address/data inputs are encoded and the data is sent serially from the encoder via the D_{out} pin.

R_S, C_{TC}, R_{TC}
(Pins 11, 12, and 13)

These pins are part of the oscillator section of the encoder (see Figure 9).

If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$
Transmit Enable (Pin 14)

This active–low transmit enable input initiates transmission when forced low. An internal pull–up device keeps this input normally high. The pull–up current is specified in the Electrical Characteristics table.

D_{out}
Data Out (Pin 15)

This is the output of the encoder that serially presents the encoded data word.

V_{SS}
Negative Power Supply (Pin 8)

The most–negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most–positive power supply pin.

MC145027 AND MC145028 DECODERS

A1 – A5, A1 – A9
Address Inputs (Pins 1 – 5) — MC145027,
Address Inputs (Pins 1 – 5, 15, 14, 13, 12) — MC145028

These are the local address inputs. The states of these pins must match the appropriate encoder inputs for the VT pin to go high. The local address may be encoded with trinary or binary data.

D6 – D9
Data Outputs (Pins 15, 14, 13, 12) — MC145027 Only

These outputs present the binary information that is on encoder inputs A6/D6 through A9/D9. Only binary data is

acknowledged; a trinary open at the MC145026 encoder is decoded as a high level (logic 1).

D_{in}
Data In (Pin 9)

This pin is the serial data input to the decoder. The input voltage must be at CMOS logic levels. The signal source driving this pin must be dc coupled.

R_1, C_1
Resistor 1, Capacitor 1 (Pins 6, 7)

As shown in Figures 2 and 3, these pins accept a resistor and capacitor that are used to determine whether a narrow pulse or wide pulse has been received. The time constant $R_1 \times C_1$ should be set to 1.72 encoder clock periods:

$$R_1 C_1 = 3.95 R_{TC} C_{TC}$$

R_2/C_2
Resistor 2/Capacitor 2 (Pin 10)

As shown in Figures 2 and 3, this pin accepts a resistor and capacitor that are used to detect both the end of a received word and the end of a transmission. The time constant $R_2 \times C_2$ should be 33.5 encoder clock periods (four data periods per Figure 11): $R_2 C_2 = 77 R_{TC} C_{TC}$. This time constant is used to determine whether the D_{in} pin has remained low for four data periods (end of transmission). A separate on–chip comparator looks at the voltage–equivalent two data periods ($0.4 R_2 C_2$) to detect the dead time between received words within a transmission.

VT
Valid Transmission Output (Pin 11)

This valid transmission output goes high after the second word of an encoding sequence when the following conditions are satisfied:

1. the received addresses of both words match the local decoder address, and
2. the received data bits of both words match.

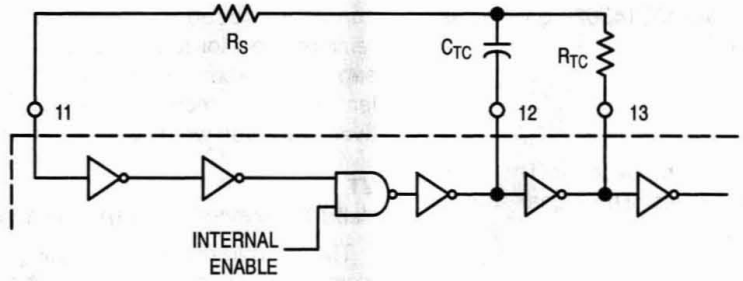
VT remains high until either a mismatch is received or no input signal is received for four data periods.

V_{SS}
Negative Power Supply (Pin 8)

The most–negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most–positive power supply pin.



This oscillator operates at a frequency determined by the external RC network; i.e.,

$$f \approx \frac{1}{2.3\ R_{TC}\ C_{TC}'} \quad (Hz)$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC}' = C_{TC} + C_{layout} + 12$ pF

$R_S \approx 2\ R_{TC}$

$R_S \geq 20$ k

$R_{TC} \geq 10$ k

400 pF < C_{TC} < 15 μF

The value for R_S should be chosen to be ≥ 2 times R_{TC}. This range ensures that current through R_S is insignificant compared to current through R_{TC}. The upper limit for R_S must ensure that R_S x 5 pF (input capacitance) is small compared to R_{TC} x C_{TC}.

For frequencies outside the indicated range, the formula is less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

Figure 9. Encoder Oscillator Information

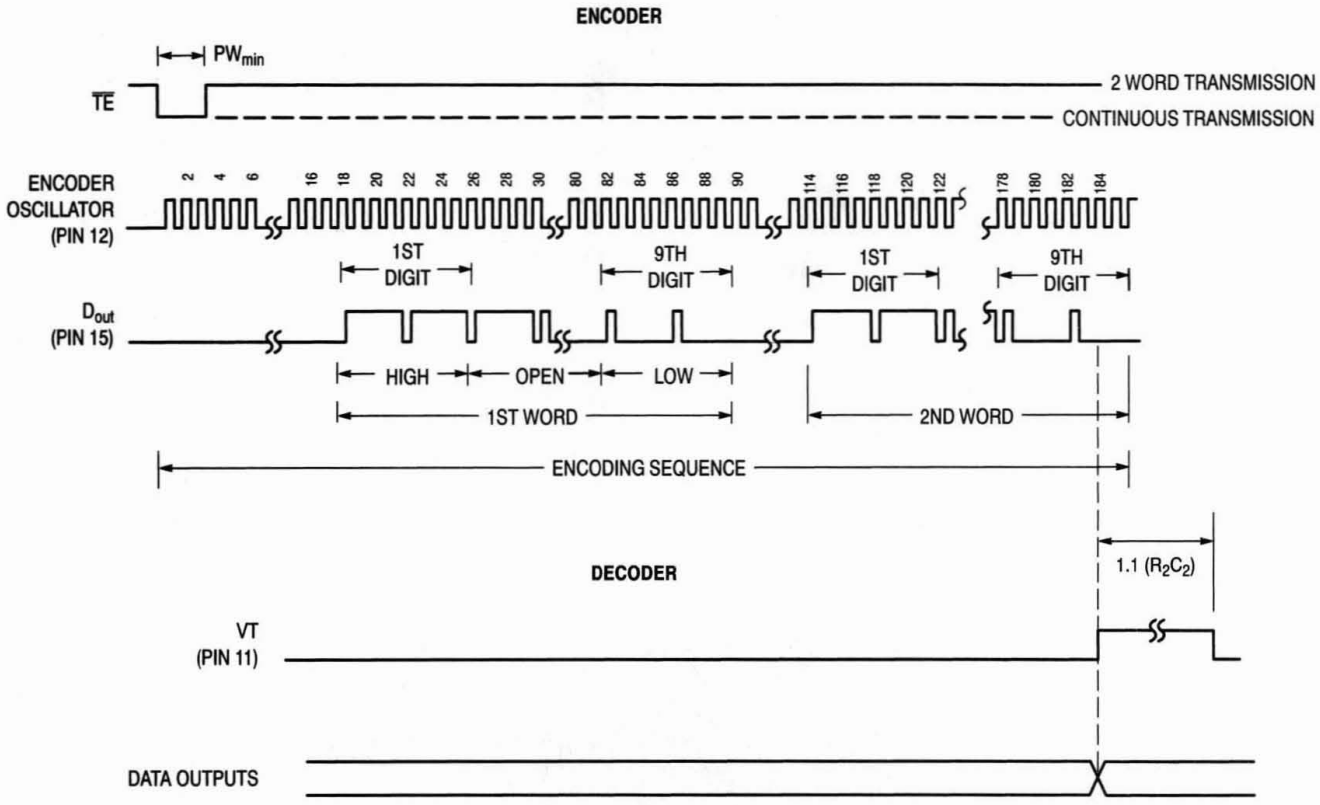


Figure 10. Timing Diagram

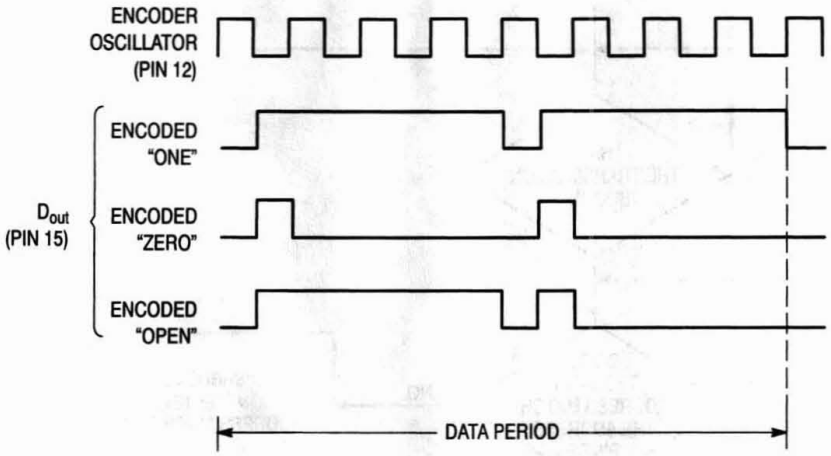


Figure 11. Encoder Data Waveforms

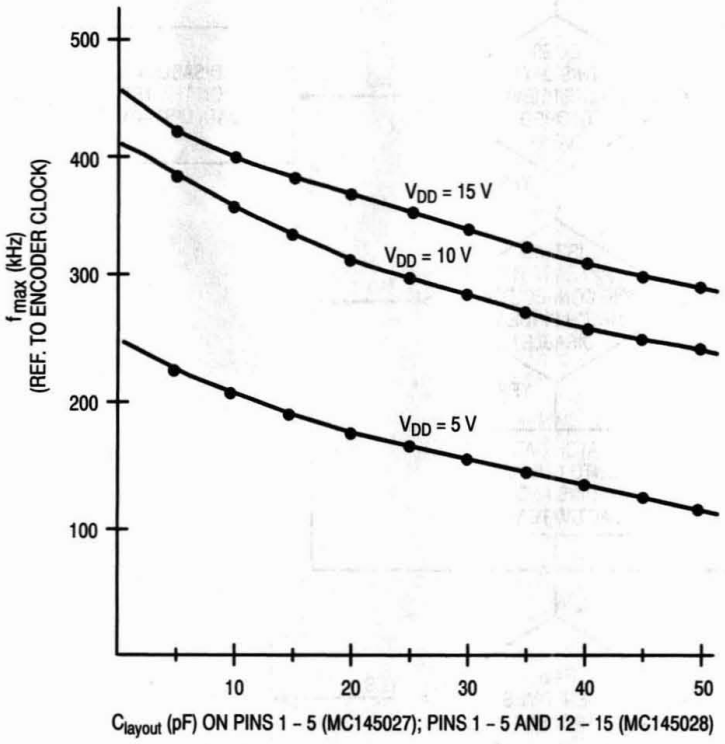


Figure 12. f_{max} vs C_{layout} — Decoders Only

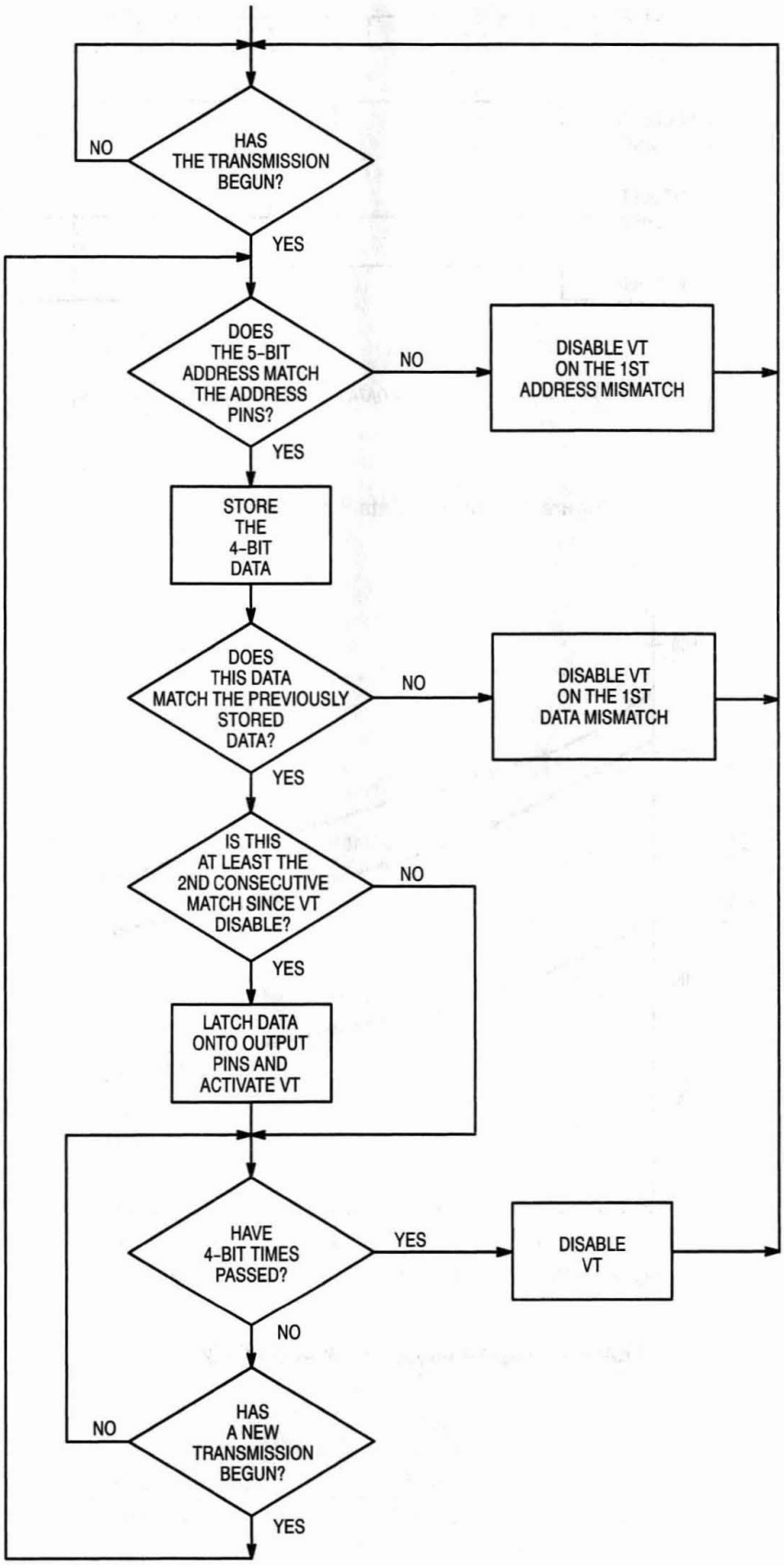


Figure 13. MC145027 Flowchart

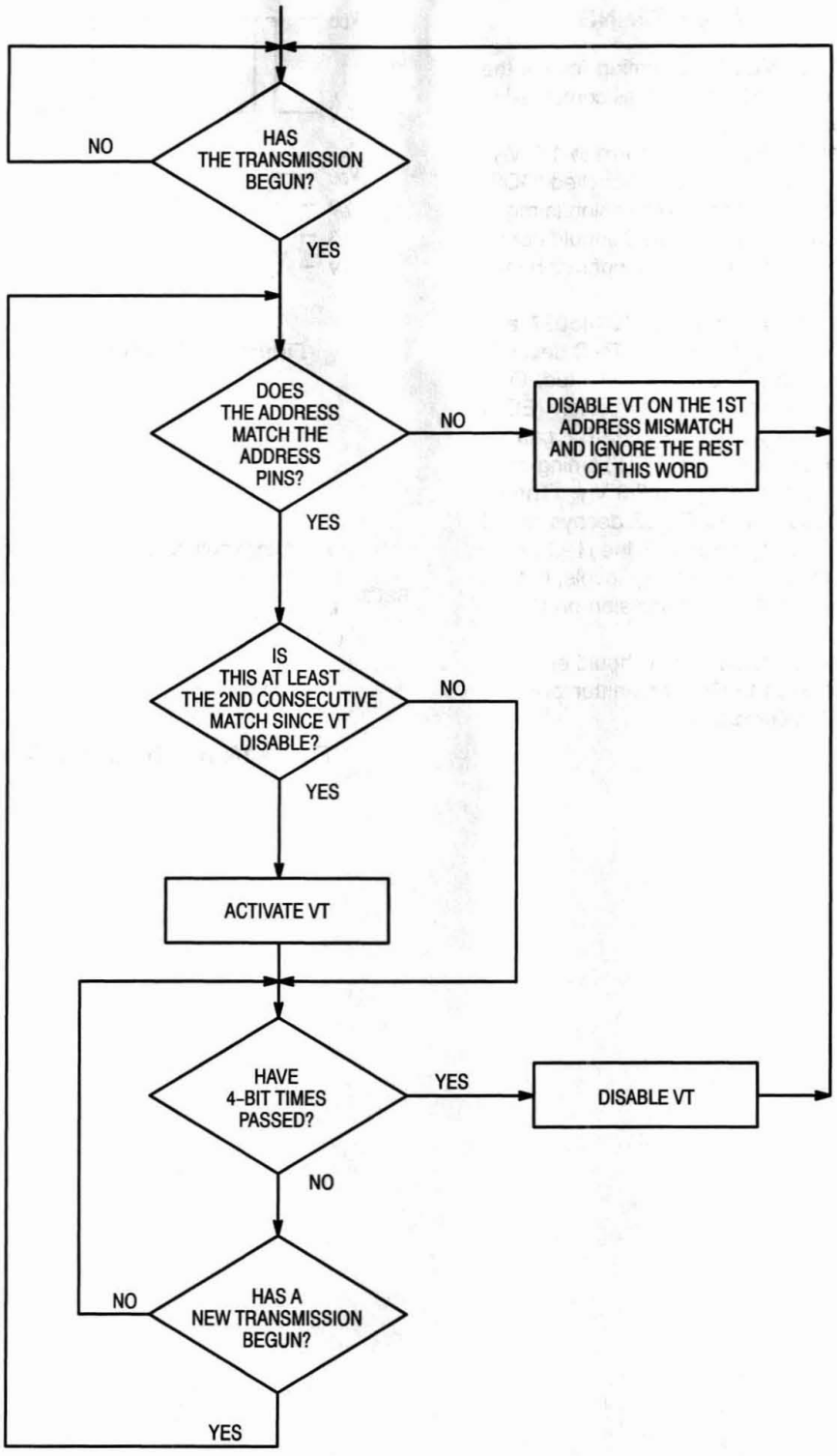


Figure 14. MC145028 Flowchart

MC145027 AND MC145028 TIMING

To verify the MC145027 or MC145028 timing, check the waveforms on C1 (Pin 7) and R2/C2 (Pin 10) as compared to the incoming data waveform on D_{in} (Pin 9).

The R–C decay seen on C1 discharges down to 1/3 V_{DD} before being reset to V_{DD}. This point of reset (labelled "DOS" in Figure 15) is the point in time where the decision is made whether the data seen on D_{in} is a 1 or 0. DOS should not be too close to the D_{in} data edges or intermittent operation may occur.

The other timing to be checked on the MC145027 and MC145028 is on R2/C2 (see Figure 16). The R–C decay is continually reset to V_{DD} as data is being transmitted. Only between words and after the end–of–transmission (EOT) does R2/C2 decay significantly from V_{DD}. R2/C2 can be used to identify the internal end–of–word (EOW) timing edge which is generated when R2/C2 decays to 2/3 V_{DD}. The internal EOT timing edge occurs when R2/C2 decays to 1/3 V_{DD}. When the waveform is being observed, the R–C decay should go down between the 2/3 and 1/3 V_{DD} levels, but not too close to either level before data transmission on D_{in} resumes.

Verification of the timing described above should ensure a good match between the MC145026 transmitter and the MC145027 and MC145028 receivers.

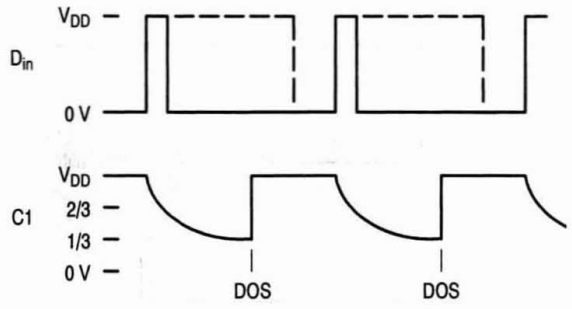


Figure 15. R–C Decay on Pin 7 (C1)

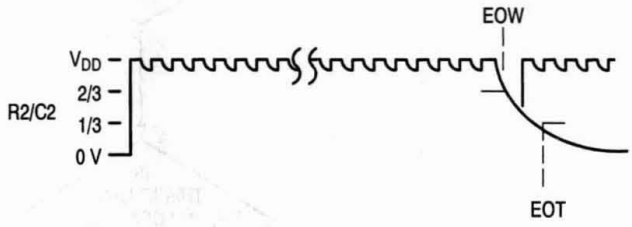
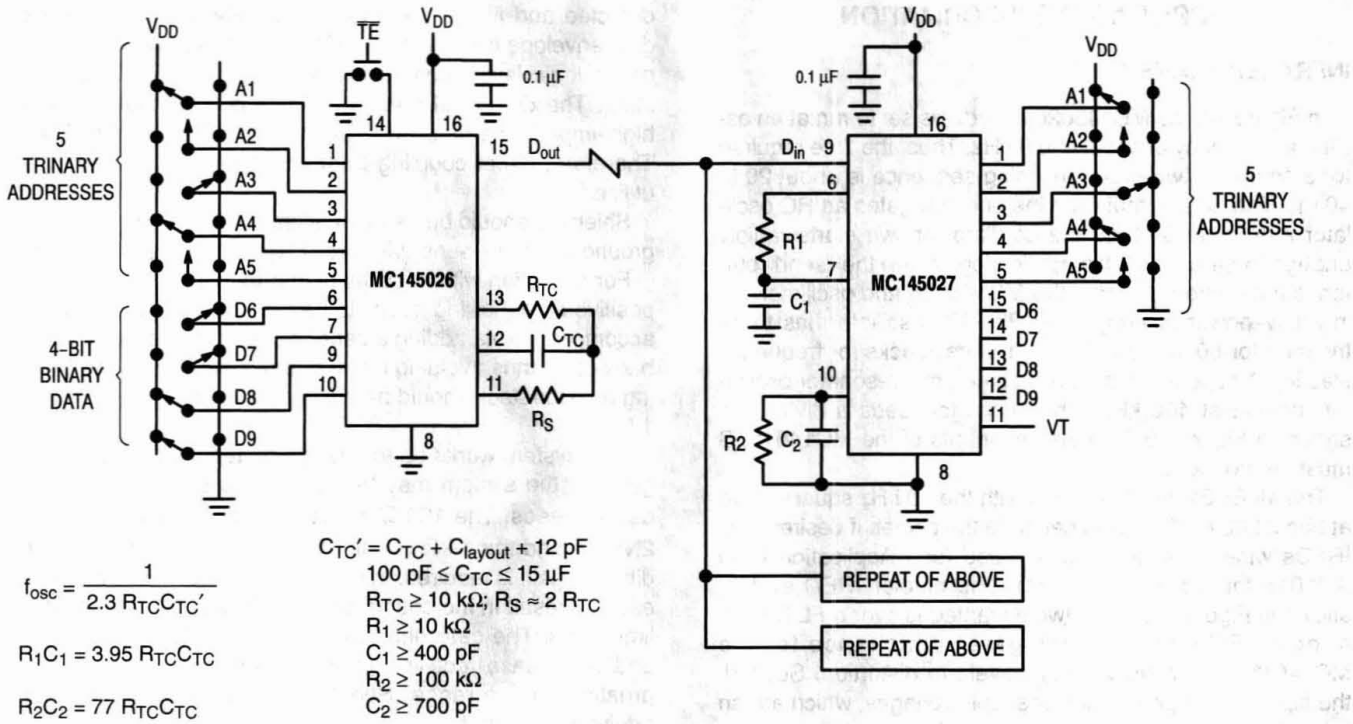


Figure 16. R–C Decay on Pin 10 (R2/C2)



$$f_{osc} = \frac{1}{2.3\ R_{TC}C_{TC'}}$$

$R_1C_1 = 3.95\ R_{TC}C_{TC}$

$R_2C_2 = 77\ R_{TC}C_{TC}$

$C_{TC'} = C_{TC} + C_{layout} + 12\ pF$

$100\ pF \le C_{TC} \le 15\ \mu F$

$R_{TC} \ge 10\ k\Omega$; $R_S \approx 2\ R_{TC}$

$R_1 \ge 10\ k\Omega$

$C_1 \ge 400\ pF$

$R_2 \ge 100\ k\Omega$

$C_2 \ge 700\ pF$

Example R/C Values (All Resistors and Capacitors are ± 5%)

($C_{TC'} = C_{TC} + 20\ pF$)

f_{osc} (kHz)	R_{TC}	$C_{TC'}$	R_S	R_1	C_1	R_2	C_2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

Figure 17. Typical Application

APPLICATIONS INFORMATION

INFRARED TRANSMITTER

In Figure 18, the MC145026 encoder is set to run at an oscillator frequency of about 4 to 9 kHz. Thus, the time required for a complete two–word encoding sequence is about 20 to 40 ms. The data output from the encoder gates an RC oscillator running at 50 kHz; the oscillator shown starts rapidly enough to be used in this application. When the "send" button is not depressed, both the MC145026 and oscillator are in a low–power standby state. The RC oscillator has to be trimmed for 50 kHz and has some drawbacks for frequency stability. A superior system uses a ceramic resonator oscillator running at 400 kHz. This oscillator feeds a divider as shown in Figure 19. The unused inputs of the MC14011UB must be grounded.

The MLED81 IRED is driven with the 50 kHz square wave at about 200 to 300 mA to generate the carrier. If desired, two IREDs wired in series can be used (see Application Note AN1016 for more information). The bipolar IRED switch, shown in Figure 18, offers two advantages over a FET. First, a logic FET has too much gate capacitance for the MC14011UB to drive without waveform distortion. Second, the bipolar drive permits lower supply voltages, which are an advantage in portable battery–powered applications.

The configuration shown in Figure 18 operates over a supply range of 4.5 to 18 V. A low–voltage system which operates down to 2.5 V could be realized if the oscillator section of a MC74HC4060 is used in place of the MC14011UB. The data output of the MC145026 is inverted and fed to the RESET pin of the MC74HC4060. Alternately, the MC74HCU04 could be used for the oscillator.

Information on the MC14011UB is in book number DL131/D. The MC74HCU04 and MC74HC4060 are found in book number DL129/D.

INFRARED RECEIVER

The receiver in Figure 20 couples an IR–sensitive diode to input preamp A1, followed by band–pass amplifier A2 with a gain of about 10. Limiting stage A3 follows, with an output of about 800 mV p–p. The limited 50 kHz burst is detected by comparator A4 that passes only positive pulses, and peak–detected and filtered by a diode/RC network to extract the data envelope from the burst. Comparator A5 boosts the signal to logic levels compatible with the MC145027/28 data input. The D_{in} pin of these decoders is a standard CMOS high–impedance input which must ***not*** be allowed to float. Therefore, direct coupling from A5 to the decoder input is utilized.

Shielding should be used on at least A1 and A2, with good ground and high–sensitivity circuit layout techniques applied.

For operation with supplies higher than + 5 V, limiter A4's positive output swing needs to be limited to 3 to 5 V. This is accomplished via adding a zener diode in the negative feedback path, thus avoiding excessive system noise. The biasing resistor stack should be adjusted such that V3 is 1.25 to 1.5 V.

This system works up to a range of about 10 meters. The gains of the system may be adjusted to suit the individual design needs. The 100 Ω resistor in the emitter of the first 2N5088 and the 1 kΩ resistor feeding A2 may be altered if different gain is required. In general, more gain does not necessarily result in increased range. This is due to noise floor limitations. The designer should increase transmitter power and/or increase receiver aperature with Fresnal lensing to greatly improve range. See Application Note AN1016 for additional information.

Information on the MC34074 is in data book DL128/D.

TRINARY SWITCH MANUFACTURERS

Midland Ross–Electronic Connector Div.
Greyhill
Augat/Alcoswitch
Aries Electronics

The above companies may not have the switches in a DIP. For more information, call them or consult *eem Electronic Engineers Master Catalog* or the *Gold Book*. ***Ask for SPDT with center OFF.***

Alternative: An SPST can be placed in series between a SPDT and the Encoder or Decoder to achieve trinary action.

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of trinary switch manufacturers.

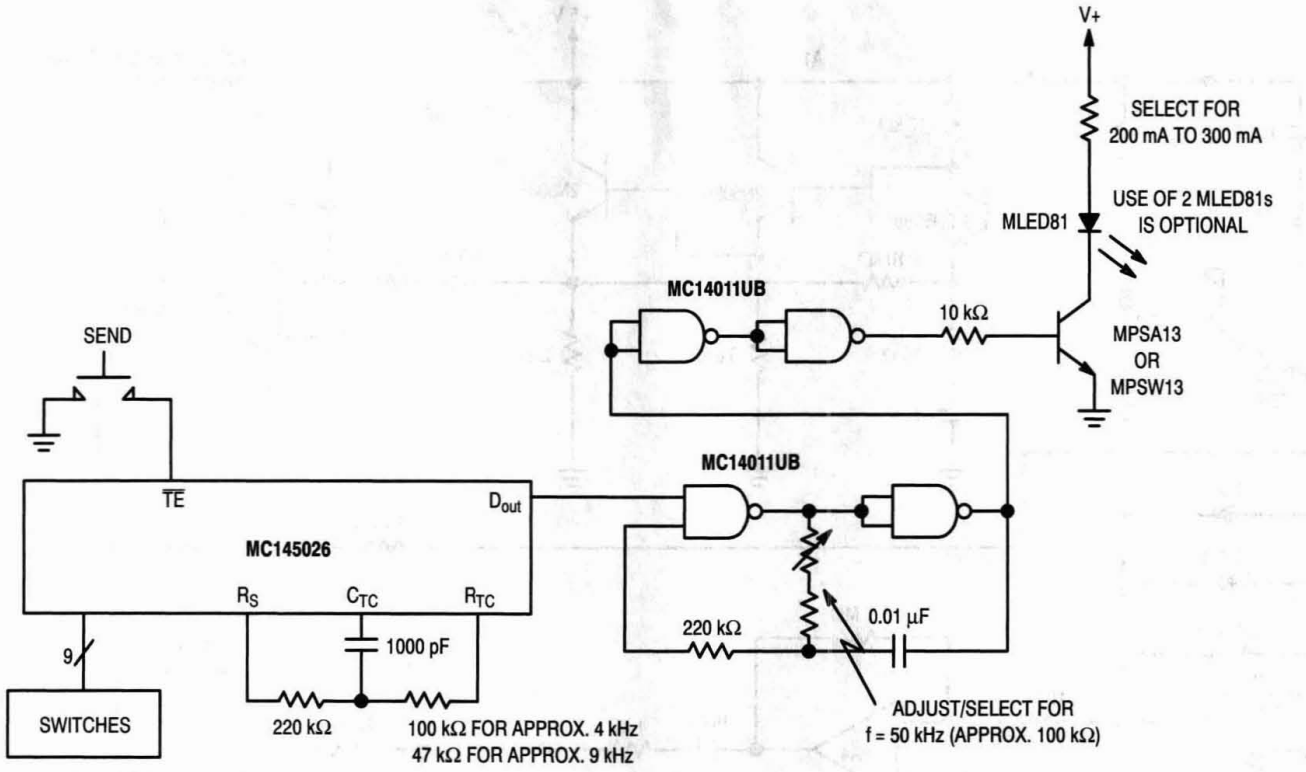


Figure 18. IRED Transmitter Using RC Oscillator to Generate Carrier Frequency

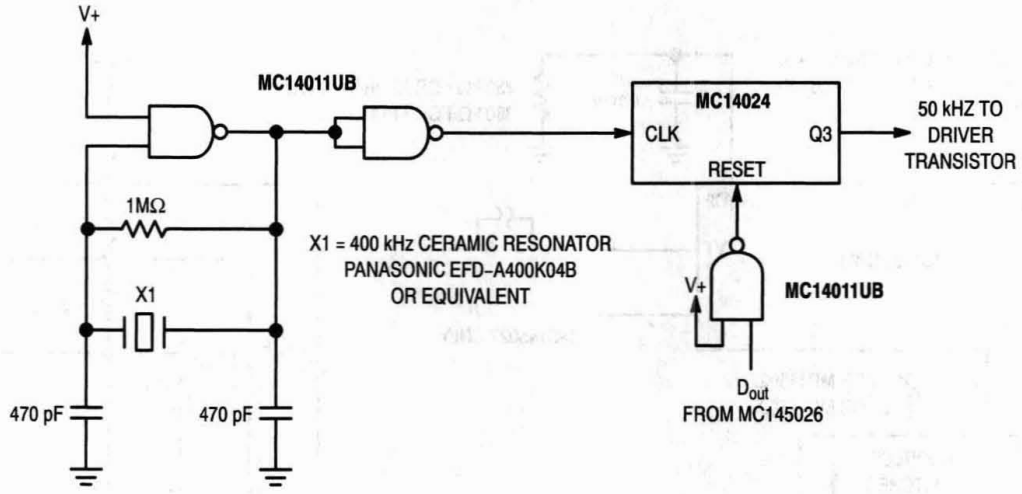


Figure 19. Using a Ceramic Resonator to Generate Carrier Frequency

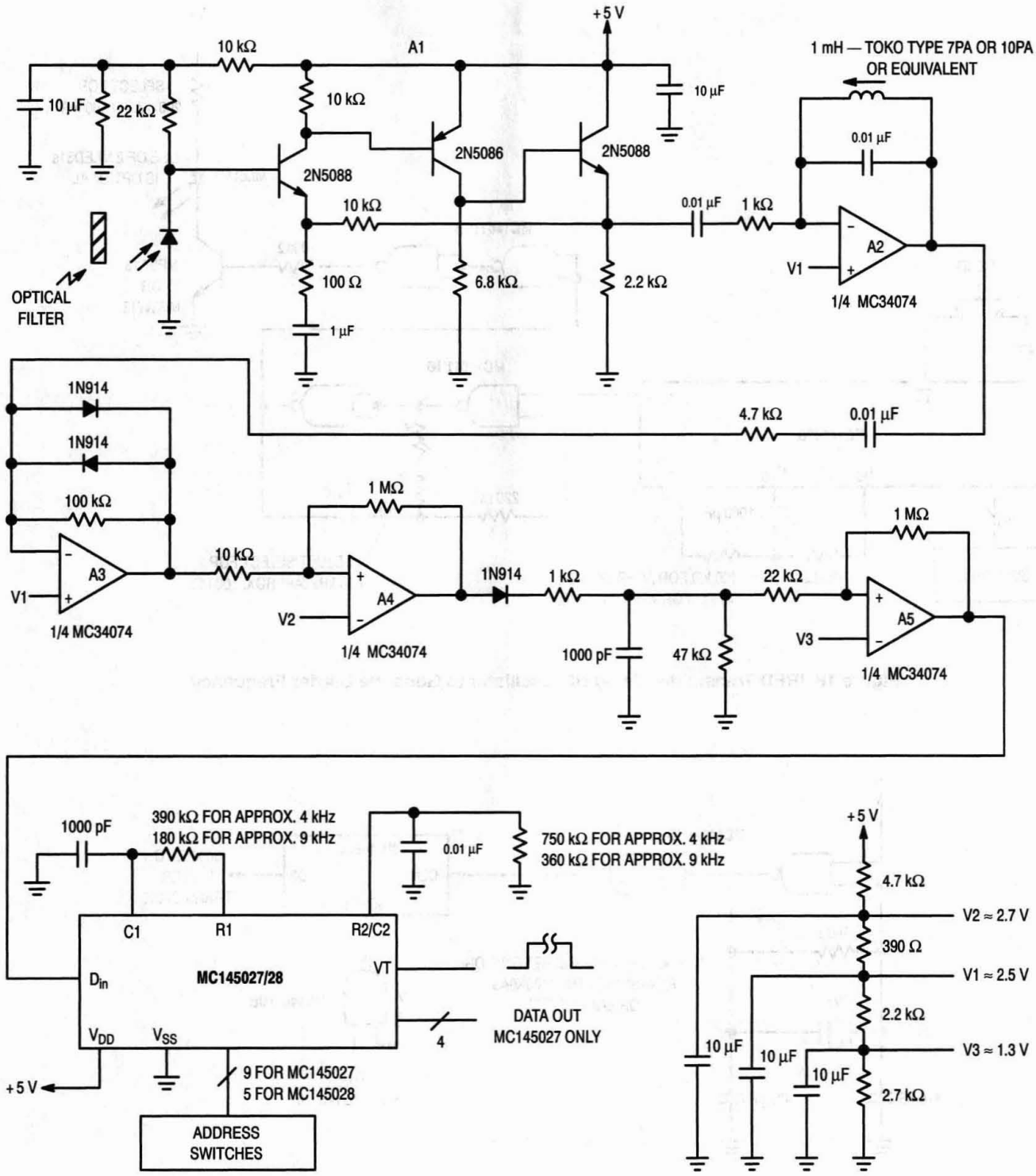


Figure 20. Infrared Receiver

Chapter Four
Frequency Synthesis

Section One **4.1–0**
Frequency Synthesis – Selector Guide

Section Two **4.2–0**
Frequency Synthesis – Data Sheets

Section One
Selector Guide

Frequency Synthesis

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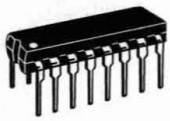
	Page
Single PLL Synthesizers	4.1–2
Packages	4.1–2

Frequency Synthesis

Single PLL Synthesizers

Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Features	Product	Suffix/ Packaging
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface	MC145151–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface, Uses External Dual–Modulus Prescaler	MC145152–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface	MC145157–2	DW/751G
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface, Uses External Dual–Modulus Prescaler	MC145158–2	DW/751G
100 @ 3.0 V 185 @ 4.5 V	2.7 to 5.5	2 @ 3 V 6 @ 5 V	Serial Interface, Auxiliary Reference Divider, Evaluation Kit – MC145170EVK	MC145170–2	P/648, D/751B, DT/948C

Frequency Synthesis Packages



CASE 648
P SUFFIX
(DIP-16)

CASE 751B
D SUFFIX
(SO-16)

CASE 751F
DW SUFFIX
(SO-28L)

CASE 751G
DW SUFFIX
(SO-16W)

CASE 948C
DT SUFFIX
(TSSOP-16)

Section Two

Frequency Synthesis – Data Sheets

Device Number	Page Number
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Single	
MC145151–2	4.2–4
MC145152–2	4.2–7
MC145157–2	4.2–11
MC145158–2	4.2–14
MC145170–2	4.2–26

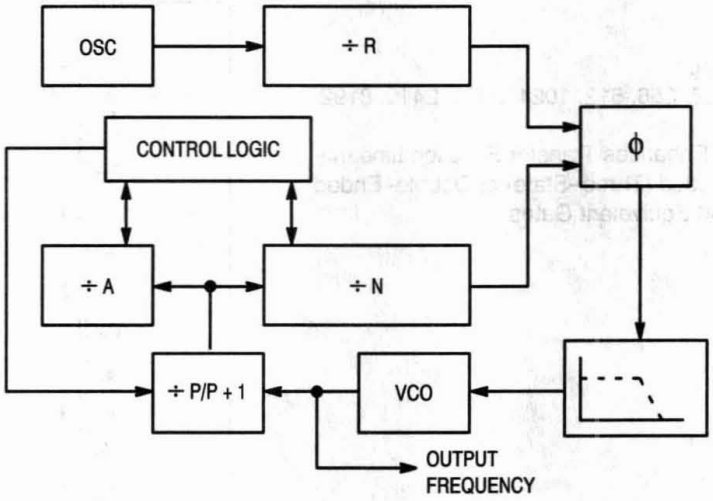
MC145151-2
MC145152-2
MC145157-2
MC145158-2

PLL Frequency Synthesizer Family
CMOS

The devices described in this document are typically used as low–power, phase–locked loop frequency synthesizers. When combined with an external low–pass filter and voltage–controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two–Way Radios	Amateur Radio



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DEVICE DETAIL SHEETS

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MC145152–2 Parallel–Input, Dual–Modulus 4.2–7
MC145157–2 Serial–Input, Single–Modulus 4.2–11
MC145158–2 Serial–Input, Dual–Modulus 4.2–14

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AC Electrical Characteristics 4.2–19
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Frequency Characteristics 4.2–21
Phase Detector/Lock Detector Output Waveforms 4.2–21

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Crystal Oscillator Considerations 4.2–23
Dual–Modulus Prescaling 4.2–24

REV 4
12/99

MC145151-2

Parallel-Input PLL Frequency Synthesizer

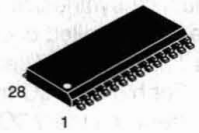
Interfaces with Single–Modulus Prescalers

The MC145151–2 is programmed by 14 parallel–input data lines for the N counter and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, and 14–bit programmable divide–by–N counter.

The MC145151–2 is an improved–performance drop–in replacement for the MC145151–1. The power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates

P SUFFIX
PLASTIC DIP
CASE 710

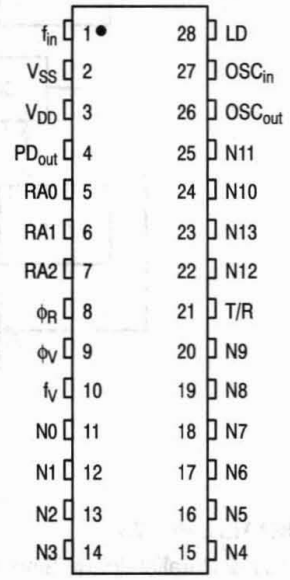


DW SUFFIX
SOG PACKAGE
CASE 751F

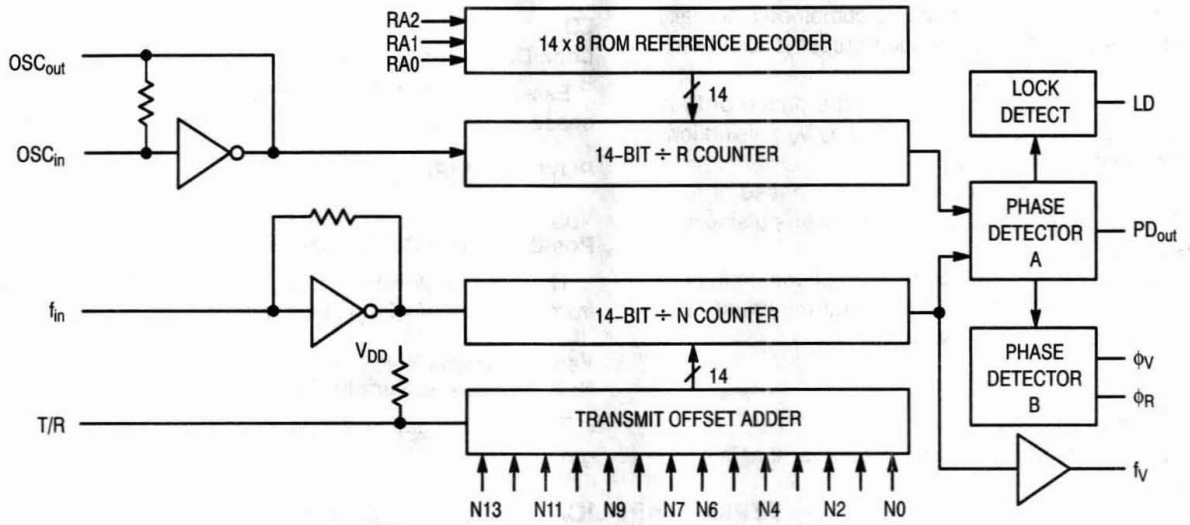
ORDERING INFORMATION

MC145151P2	Plastic DIP
MC145151DW2	SOG Package

PIN ASSIGNMENT



MC145151–2 BLOCK DIAGRAM



NOTE: N0 – N13 inputs and inputs RA0, RA1, and RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0 – RA2
Reference Address Inputs (Pins 5, 6, 7)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N0 – N11
N Counter Programming Inputs (Pins 11 – 20, 22 – 25)

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant and N13 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only an SPST switch to alter data to the zero state.

T/R
Transmit/Receive Offset Adder Input (Pin 21)

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pull–up resistor ensures that no connection will appear as a logic 1 causing no offset addition.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 4)

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 8, 9)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V
N Counter Output (Pin 10)

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS

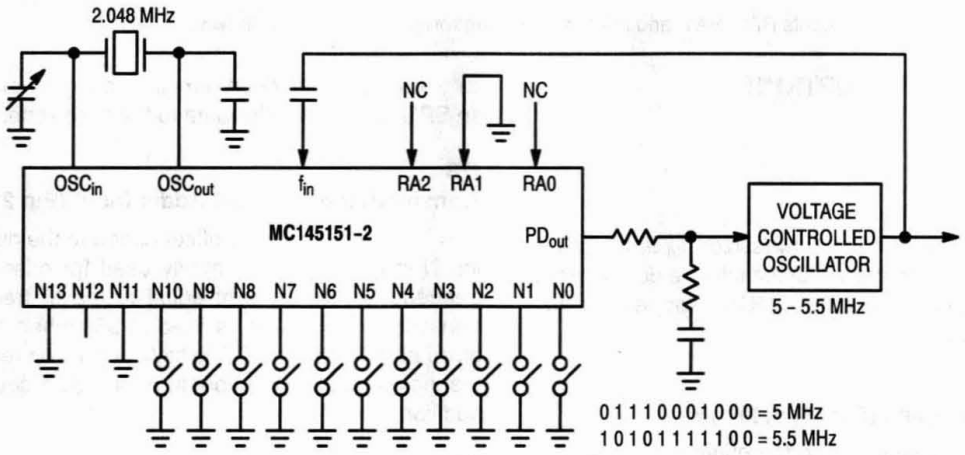
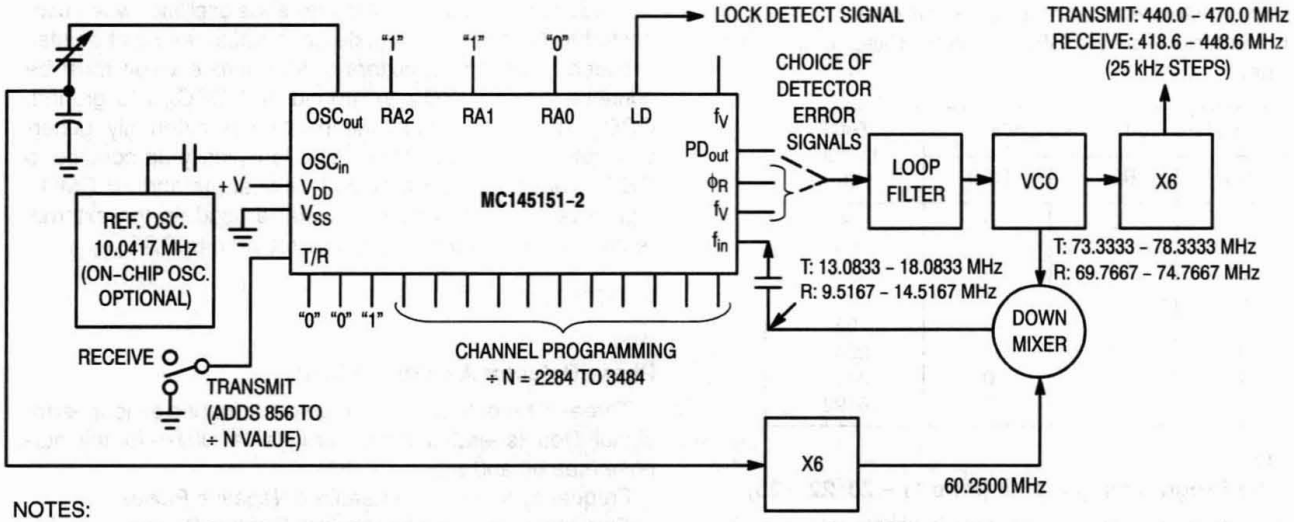


Figure 1. 5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz



NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440 – 470 MHz band. Similar implementation applies to the 406 – 440 MHz band. For 470 – 512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Figure 2. Synthesizer for Land Mobile Radio UHF Bands

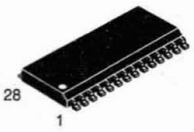
MC145151–2 Data Sheet Continued on Page 4.2–17

MC145152-2

Parallel-Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

P SUFFIX
PLASTIC DIP
CASE 710



DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

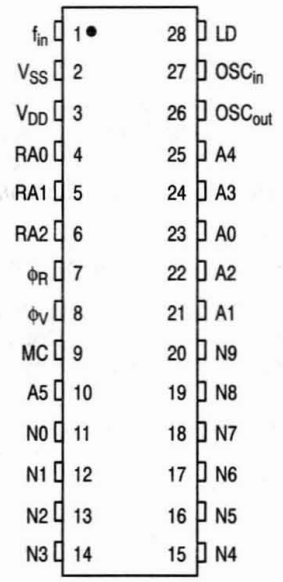
MC145152P2	Plastic DIP
MC145152DW2	SOG Package

The MC145152–2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, two–output phase detector, 10–bit programmable divide–by–N counter, and 6–bit programmable ÷ A counter.

The MC145152–2 is an improved–performance drop–in replacement for the MC145152–1. Power consumption has decreased and ESD and latch–up performance have improved.

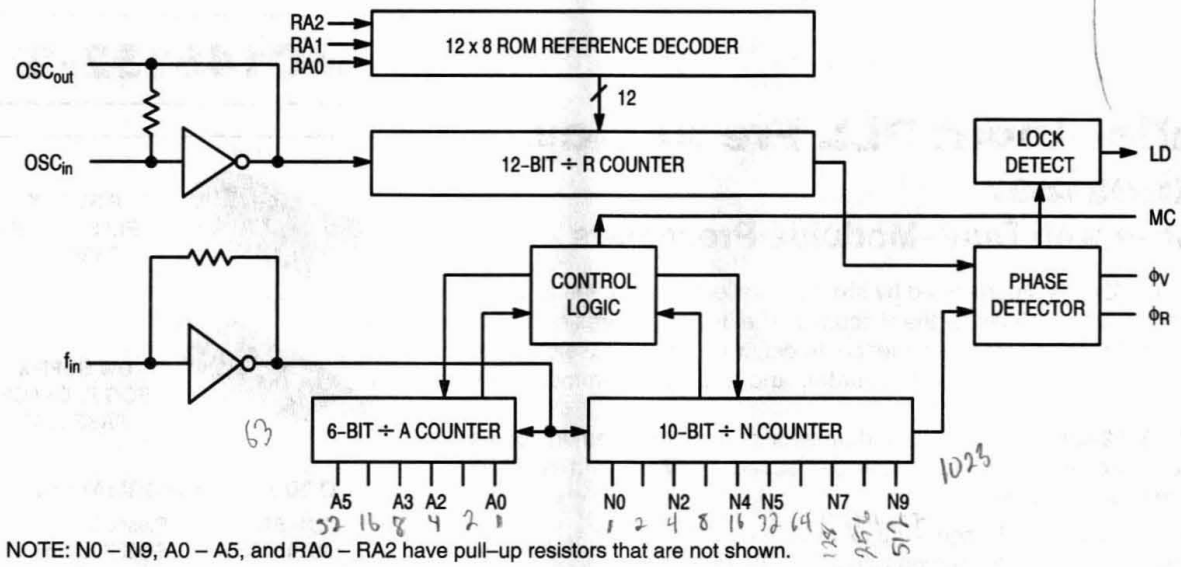
- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates
- See Application Note AN980

PIN ASSIGNMENT



REV 1
8/95

MC145152–2 BLOCK DIAGRAM



NOTE: N0 – N9, A0 – A5, and RA0 – RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual–modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2
Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

N0 – N9
N Counter Programming Inputs (Pins 11 – 20)

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

A0 – A5
A Counter Programming Inputs (Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of f_{in} that require a logic 0 on the MC output (see **Dual–Modulus Prescaling** section). The A inputs all have internal pull–up resistors that ensure that inputs left open will remain at a logic 1.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 7, 8)

These phase detector outputs can be combined externally for a loop–error signal.

If the frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 9)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first

portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

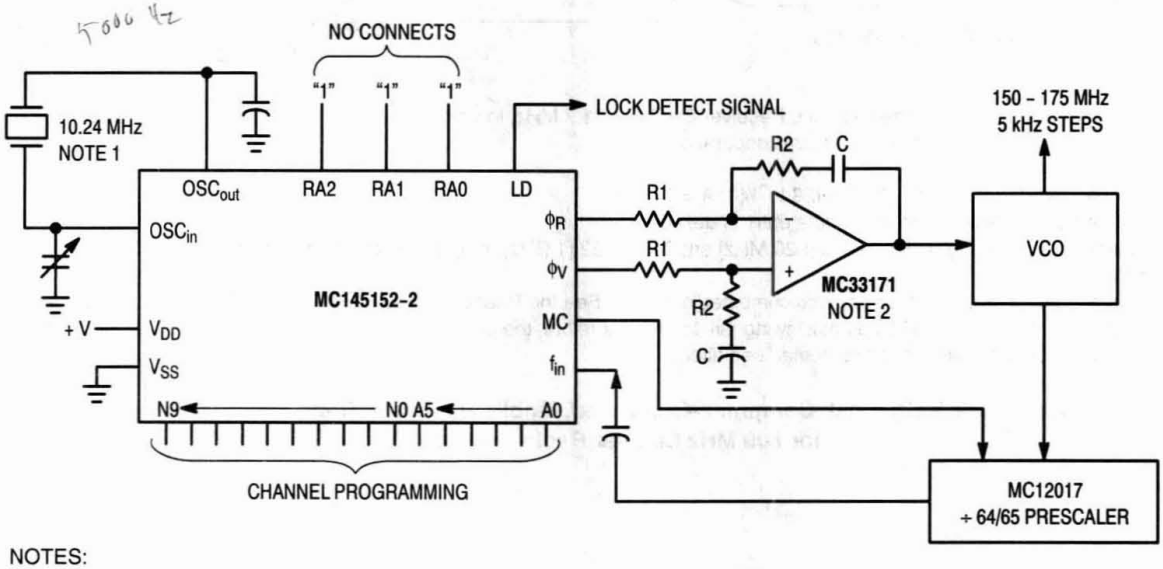
V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

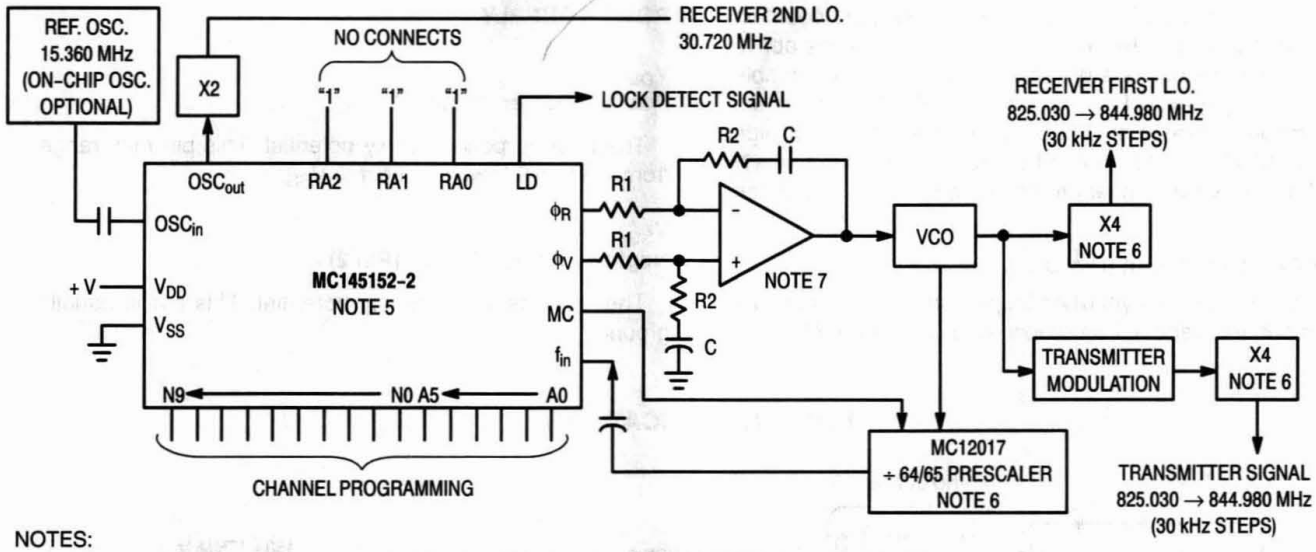
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



NOTES:
1. Off–chip oscillator optional.
2. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. Synthesizer for Land Mobile Radio VHF Bands



NOTES:

1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receiver/transmit separation.
3. f_R = 7.5 kHz; ÷ R = 2048.
4. N_{total} = N • 64 + A = 27501 to 28166; N = 429 to 440; A = 0 to 63.
5. MC145158–2 may be used where serial data entry is desired.
6. High frequency prescalers (e.g., MC12018 [520 MHz] and MC12022 [1 GHz]) may be used for higher frequency VCO and f_{ref} implementations.
7. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 2. 666–Channel, Computer–Controlled, Mobile Radiotelephone Synthesizer for 800 MHz Cellular Radio Systems

MC145152–2 Data Sheet Continued on Page 4.2–17

MC145157-2

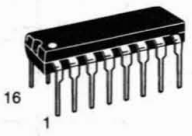
Serial-Input PLL Frequency Synthesizer

Interfaces with Single–Modulus Prescalers

The MC145157–2 has a fully programmable 14–bit reference counter, as well as a fully programmable ÷ N counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145157–2 is an improved–performance drop–in replacement for the MC145157–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



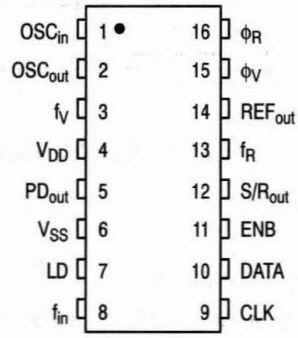
P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC145157P2	Plastic DIP
MC145157DW2	SOG Package

PIN ASSIGNMENT



REV 1
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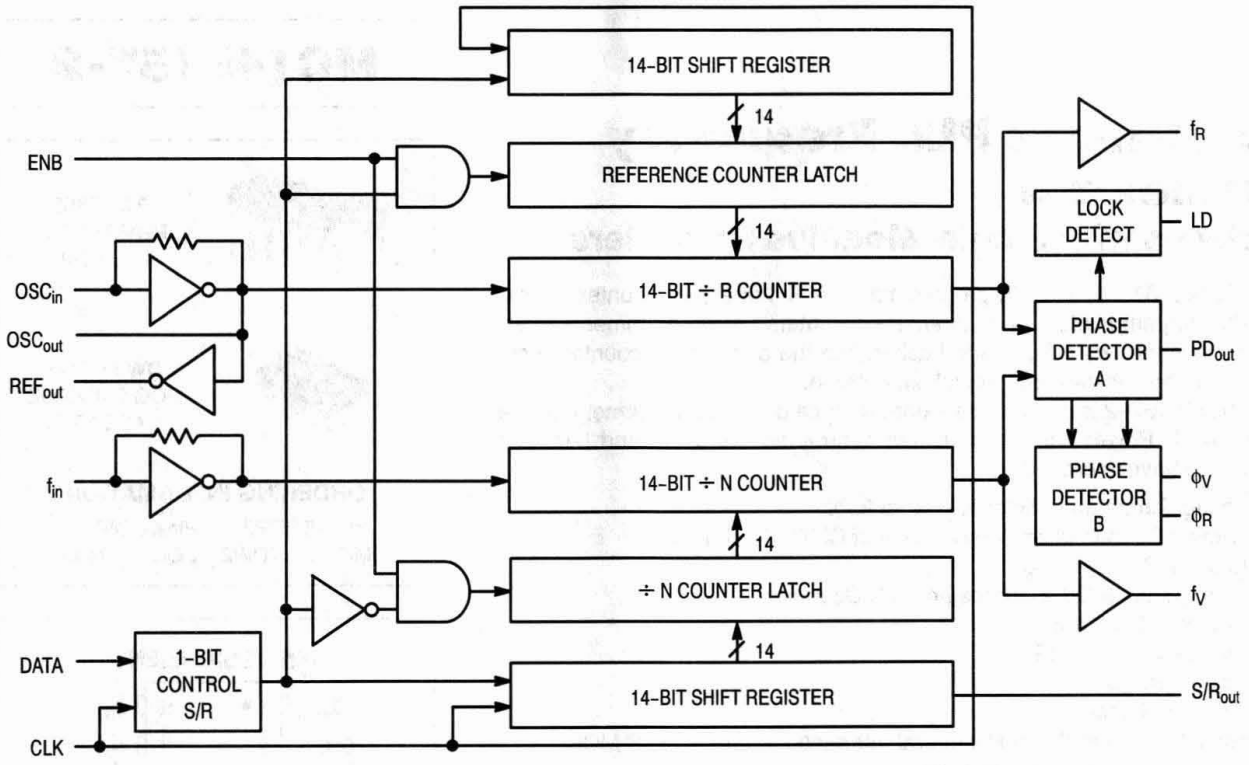
MC145157–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the clock shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ N counter latch. The entry format is as follows:

ENB
Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Single–Ended Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Double–Ended Phase Detector B Outputs (Pins 16, 15)

These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R, f_V
R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

S/R_{out}
Shift Register Output (Pin 12)

This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

MC145157–2 Data Sheet Continued on Page 4.2–17

MC145158-2

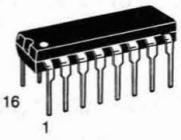
Serial-Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

The MC145158–2 has a fully programmable 14–bit reference counter, as well as fully programmable ÷ N and ÷ A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145158–2 is an improved–performance drop–in replacement for the MC145158–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 1023
- Dual Modulus Capability; ÷ A Range = 0 to 127
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single–Ended (Three–State) or Double–Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



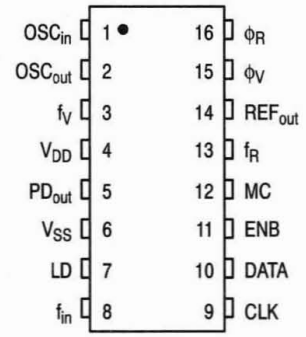
P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG PACKAGE
CASE 751G

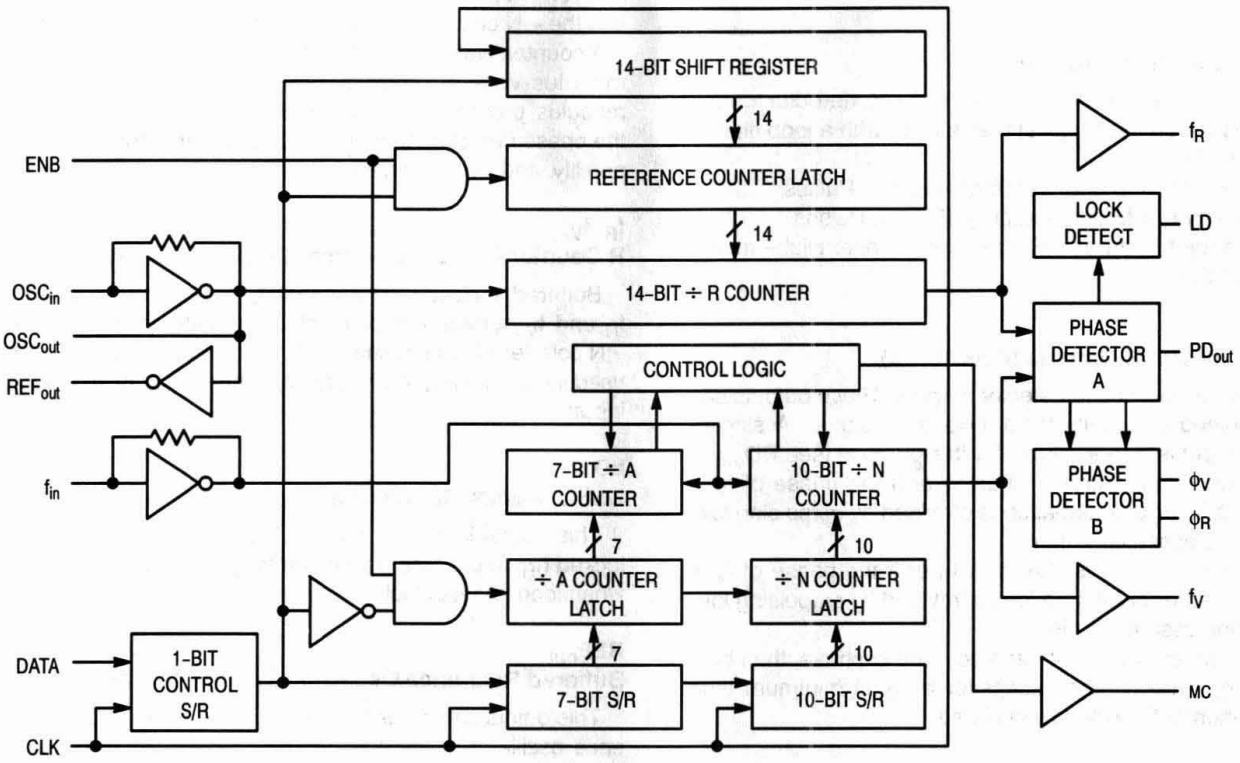
ORDERING INFORMATION

MC145158P2	Plastic DIP
MC145158DW2	SOG Package

PIN ASSIGNMENT



MC145158–2 BLOCK DIAGRAM



PIN DESCRIPTIONS

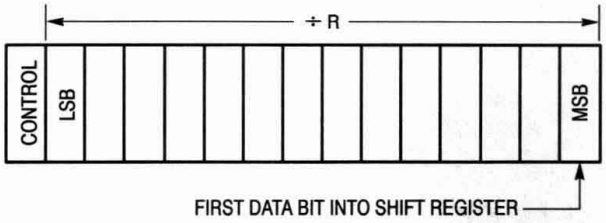
INPUT PINS

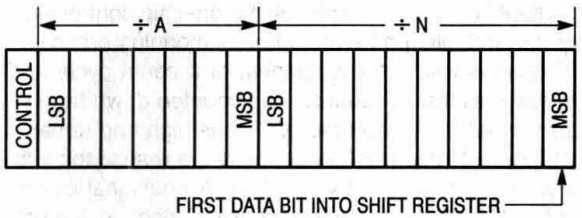
f_{in}
Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ A and ÷ N counters. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p–p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low–to–high transition of the CLK shifts one bit of data into the on–chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ A, ÷ N counter latch. The data entry format is as follows:





ENB
Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 5)

This single–ended (three–state) phase detector output produces a loop–error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 16, 15)

Double–ended phase detector outputs. These outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 12)

This output generates a signal by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual–modulus version offers a distinct advantage. The dual–modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

f_R, f_V
R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually ground.

MC14515X–2 FAMILY CHARACTERISTICS AND DESCRIPTIONS

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage (DC or Transient), SW1, SW2 ($R_{pull-up}$ = 4.7 kΩ)	– 0.5 to + 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: – 12 mW/°C from 65 to 85°C
SOG Package: – 7 mW/°C from 65 to 85°C

These devices contain protection circuitry to protect against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull–up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3	9	3	9	3	9	V
I_{ss}	Dynamic Supply Current	f_{in} = OSC_{in} = 10 MHz, 1 V p–p ac coupled sine wave R = 128, A = 32, N = 128	3 5 9	— — —	3.5 10 30	— — —	3 7.5 24	— — —	3 7.5 24	mA
I_{SS}	Quiescent Supply Current (not including pull–up current component)	V_{in} = V_{DD} or V_{SS} I_{out} = 0 µA	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac coupled sine wave	—	500	—	500	—	500	—	mV p–p
V_{IL}	Low–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input dc $V_{out} \ge 3.5$ V coupled $V_{out} \ge 6.3$ V square wave	3 5 9	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High–Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input dc $V_{out} \le 1.5$ V coupled $V_{out} \le 2.7$ V square wave	3 5 9	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low–Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High–Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	V_{in} = V_{DD} or V_{SS}	9	± 2	± 50	± 2	± 25	± 2	± 22	µA
I_{IL}	Input Leakage Current (Data, CLK, ENB — without pull–ups)	V_{in} = V_{SS}	9	—	– 0.3	—	– 0.1	—	– 1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	V_{in} = V_{DD}	9	—	0.3	—	0.1	—	1.0	µA

(continued)

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
I_{IL}	Pull–up Current (all inputs with pull–ups)	$V_{in} = V_{SS}$	9	– 20	– 400	– 20	– 200	– 20	– 170	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High–Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High–Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
$V_{(BR)DSS}$	Drain–to–Source Breakdown Voltage — SW1, SW2	$R_{pull-up}$ = 4.7 kΩ	—	15	—	15	—	15	—	V
I_{OL}	Low–Level Sinking Current — MC	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	mA
I_{OH}	High–Level Sourcing Current — MC	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3 5 9	– 0.60 – 0.90 – 1.50	— — —	– 0.50 – 0.75 – 1.25	— — —	– 0.30 – 0.50 – 0.80	— — —	mA
I_{OL}	Low–Level Sinking Current — LD	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3 5 9	0.25 0.64 1.30	— — —	0.20 0.51 1.00	— — —	0.15 0.36 0.70	— — —	mA
I_{OH}	High–Level Sourcing Current — LD	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3 5 9	– 0.25 – 0.64 – 1.30	— — —	– 0.20 – 0.51 – 1.00	— — —	– 0.15 – 0.36 – 0.70	— — —	mA
I_{OL}	Low–Level Sinking Current — SW1, SW2	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.05	— — —	mA
I_{OL}	Low–Level Sinking Current — Other Outputs	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	mA
I_{OH}	High–Level Sourcing Current — Other Outputs	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3 5 9	– 0.44 – 0.64 – 1.30	— — —	– 0.35 – 0.51 – 1.00	— — —	– 0.22 – 0.36 – 0.70	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	± 0.3	—	± 0.1	—	± 1.0	µA
I_{OZ}	Output Leakage Current — SW1, SW2	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	± 0.3	—	± 0.1	—	± 3.0	µA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three–State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC (Figures 1 and 4)	3 5 9	110 60 35	120 70 40	ns
t_{PHL}	Maximum Propagation Delay, ENB to SW1, SW2 (Figures 1 and 5)	3 5 9	160 80 50	180 95 60	ns
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figures 2 and 4)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD (Figures 3 and 4)	3 5 9	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 4)	3 5 9	160 80 60	175 100 65	ns

SWITCHING WAVEFORMS

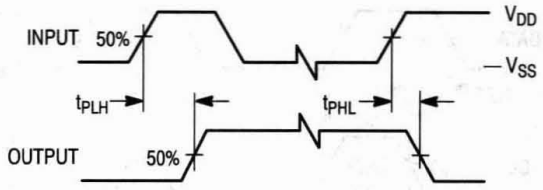
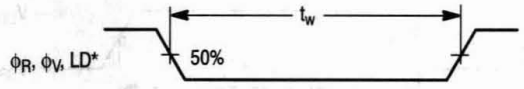


Figure 1.



* f_R in phase with f_V.

Figure 2.

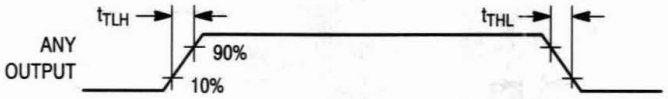
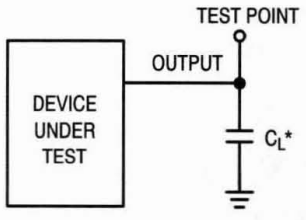
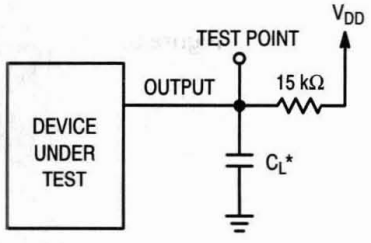


Figure 3.



* Includes all probe and fixture capacitance.

Figure 4. Test Circuit



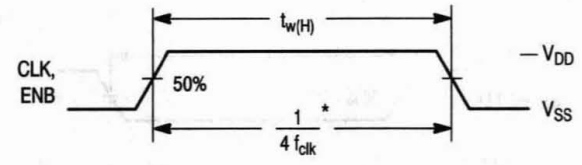
* Includes all probe and fixture capacitance.

Figure 5. Test Circuit

TIMING REQUIREMENTS (Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to CLK $t_{w(H)}$ below (Figure 6)	3 5 9	dc to 5.0 dc to 7.1 dc to 10	dc to 3.5 dc to 7.1 dc to 10	MHz
t_{su}	Minimum Setup Time, Data to CLK (Figure 7)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, CLK to Data (Figure 7)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, CLK to ENB (Figure 7)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, ENB to CLK (Figure 7)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, CLK and ENB (Figure 6)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times — Any Input (Figure 8)	3 5 9	5 4 2	5 4 2	µs

SWITCHING WAVEFORMS



*Assumes 25% Duty Cycle.

Figure 6.

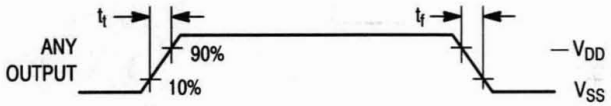


Figure 8.

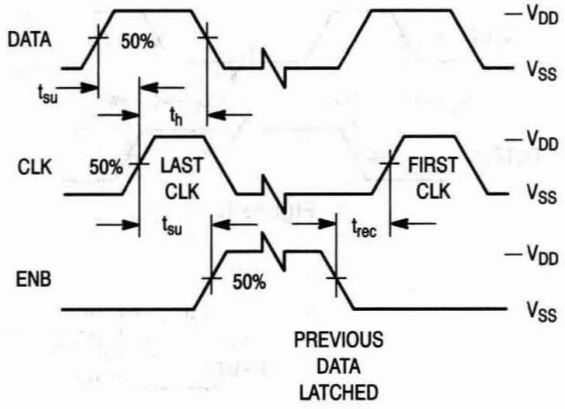
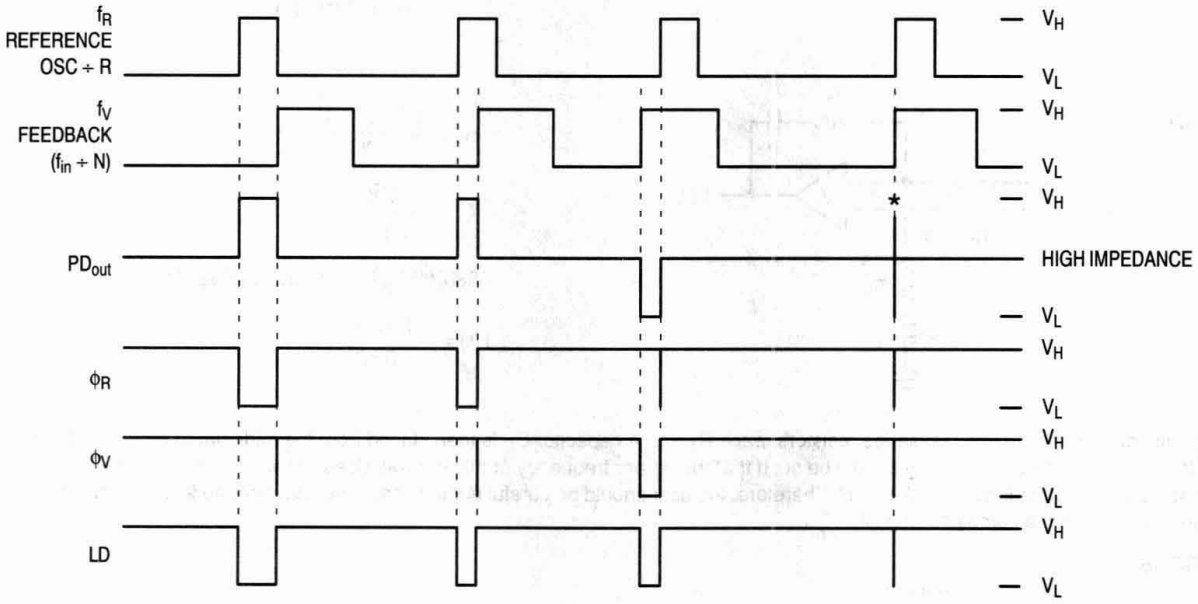


Figure 7.

FREQUENCY CHARACTERISTICS (Voltages References to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ =10 ns unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1 V p–p ac coupled sine wave	3 5 9	— — —	12 22 25	— — —	12 20 22	— — —	7 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc coupled square wave	3 5 9	— — —	13 25 25	— — —	12 22 25	— — —	8 22 25	MHz

NOTE: Usually, the PLL's propagation delay from f_{in} to MC plus the setup time of the prescaler determines the upper frequency limit of the system. The upper frequency limit is found with the following formula: $f = P/(t_P + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual modulus prescaler ratios, t_P is the f_{in} to MC propagation delay in seconds, and t_{set} is the prescaler setup time in seconds.
For example, with a 5 V supply, the f_{in} to MC delay is 70 ns. If the MC12028A prescaler is used, the setup time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P/(t_P + t_{set}) = 64/(70 + 16) = 744$ MHz.



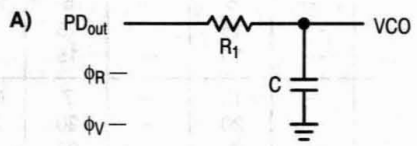
V_H = High Voltage Level.
V_L = Low Voltage Level.
* At this point, when both f_R and f_V are in phase, the output is forced to near mid–supply.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency the output is high and the voltage at this pin is determined by the low–pass filter capacitor.

Figure 9. Phase Detector/Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

A)

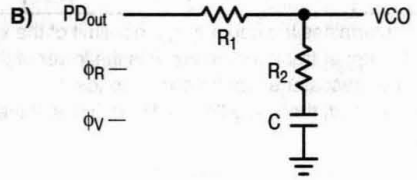


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

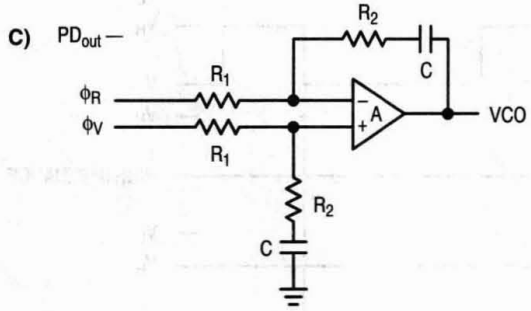


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

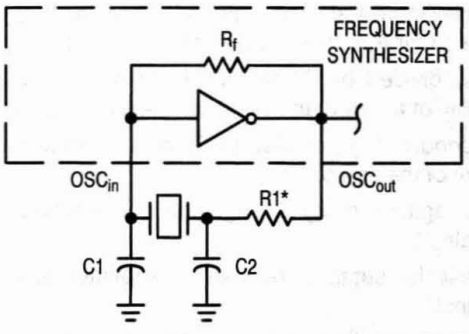
For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

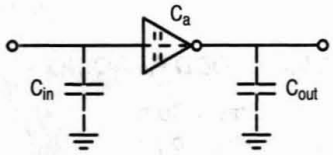
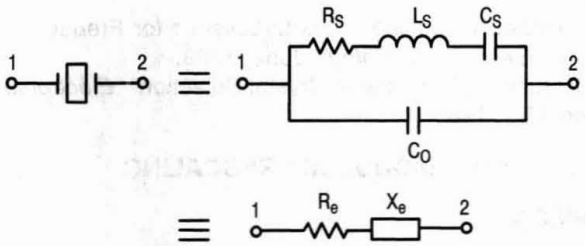


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).

Table 1. Partial List of Crystal Manufacturers

Motorola — Internet Address *http://motorola.com* (Search for resonators)
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

DUAL–MODULUS PRESCALING

OVERVIEW

The technique of dual–modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low–frequency programmable counters to be used as high–frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single–modulus) divider is used for the prescaler.

In dual–modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual–modulus frequency synthesizers contain this feature and can be used with a variety of dual–modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual–modulus prescaler approaches suitable for use with the MC145152–2, MC145156–2, or MC145158–2 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12028A	÷ 32/33 or ÷ 64/65	1.1 GHz
MC12052A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12054A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application:

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual–modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint N ≥ A always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\ P + A$ or $(P - 1)\ P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual–modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its MC is low.

For the maximum frequency into the prescaler (f_{VCOmax}), the value used for P must be large enough such that:

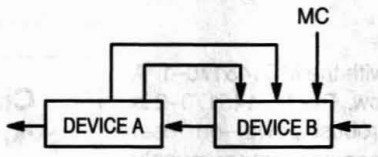
1. f_{VCOmax} divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual–modulus prescaler.
   b. Prescaler setup or release time relative to its MC signal.
   c. Propagation time from f_{in} to the MC output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.

3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual–modulus values are achievable (shown in Figure 13).



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

Figure 13. Dual–Modulus Values

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MC145170-2

PLL Frequency Synthesizer with Serial Interface

The new MC145170–2 is pin–for–pin compatible with the MC145170–1. A comparison of the two parts is shown in the table below. The MC145170–2 is recommended for new designs and has a more robust power–on reset (POR) circuit that is more responsive to momentary power supply interruptions. The two devices are actually the same chip with mask options for the POR circuit. The more robust POR circuit draws approximately 20 µA additional supply current. Note that the maximum specification of 100 µA quiescent supply current has not changed.

The MC145170–2 is a single–chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL easy to program. Either a bit– or byte–oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2–byte serial transfer to the 16–bit N register.

The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on–chip support of an external crystal, a programmable reference output, and both single– and double–ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

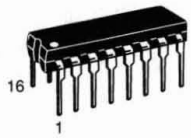
In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam–load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam–loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.7 to 5.5 V
- Maximum Operating Frequency:
  185 MHz @ V_{in} = 500 mVpp, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mVpp, 3.0 V Minimum Supply
- Operating Supply Current:
  0.6 mA @ 3.0 V, 30 MHz
  1.5 mA @ 3.0 V, 100 MHz
  3.0 mA @ 5.0 V, 50 MHz
  5.8 mA @ 5.0 V, 185 MHz
- Operating Temperature Range: –40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI Serial Data Port
- See Application Notes AN1207/D and AN1671/D
- See web site *mot–sps.com* for MC145170 control software. Select in order, Products, Wireless Semiconductor, Download, then PLL Demo Software. Choose PLLGEN.EXE.

BitGrabber is a trademark of Motorola Inc.

CMOS PLL FREQUENCY SYNTHESIZER WITH SERIAL INTERFACE

SEMICONDUCTOR TECHNICAL DATA

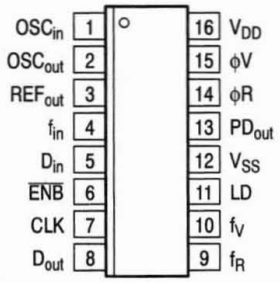


P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SOG–16)

DT SUFFIX
PLASTIC PACKAGE
CASE 948C
(TSSOP–16)

PIN CONNECTIONS



(Top View)

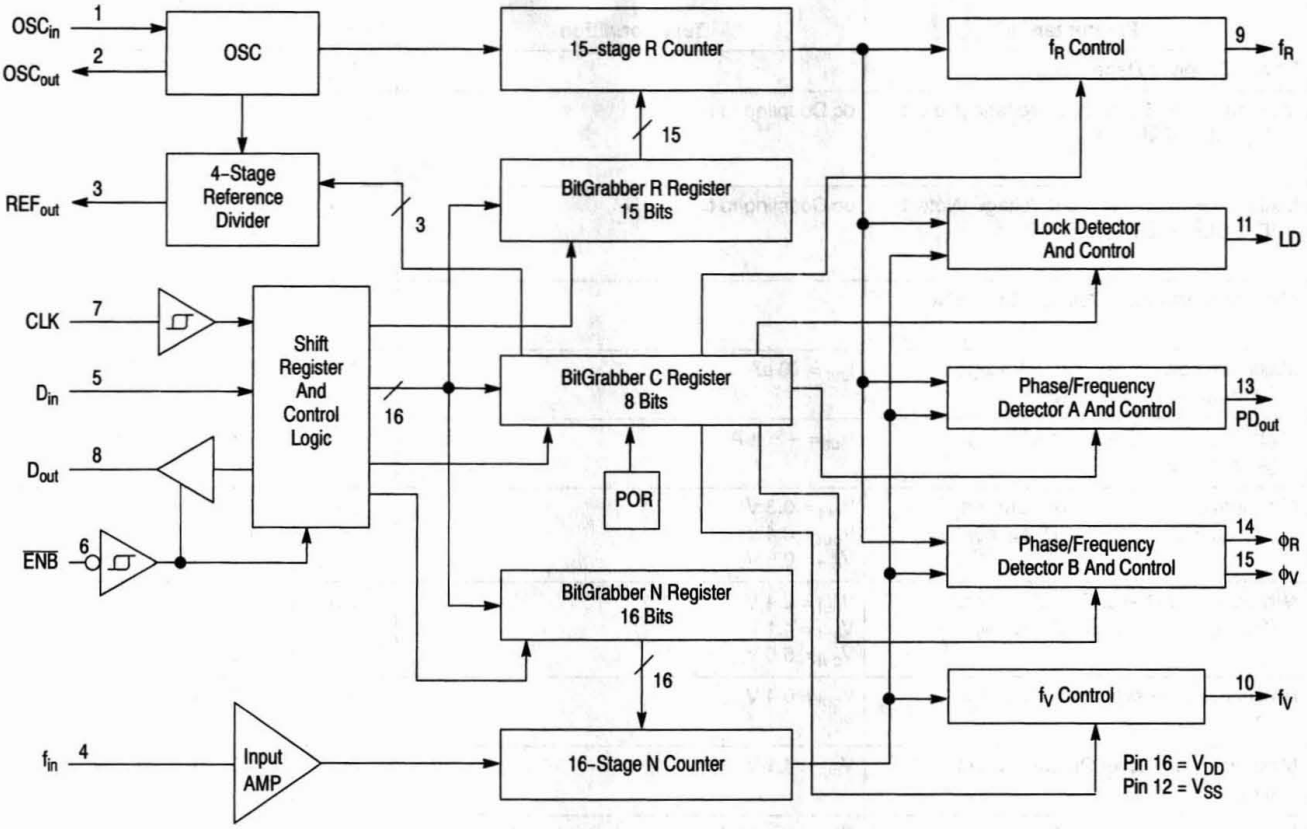
COMPARISION OF THE PLL FREQUENCY SYNTHESIZERS

Parameter	MC145170–2	MC145170–1
Minimum Supply Voltage	2.7 V	2.5 V
Maximum Input Current, f_{in}	150 µA	120 µA
Dynamic Characteristics, f_{in} (Figure 23)	Unchanged	–
Power–On Reset Circuit	Improved	–

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC145170P2	T_A = –40 to 85°C	Plastic DIP
MC145170D2		SOG–16
MC145170DT2		TSSOP–16

BLOCK DIAGRAM



This device contains 4,800 active transistors.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 5.5	V
DC Input Voltage	V_{in}	–0.5 to V_{DD} + 0.5	V
DC Output Voltage	V_{out}	–0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
DC Output Current, per Pin	I_{out}	±20	mA
DC Supply Current, V_{DD} and V_{SS} Pins	I_{DD}	±30	mA
Power Dissipation, per Package	P_D	300	mW
Storage Temperature	T_{stg}	–65 to 150	°C
Lead Temperature, 1 mm from Case for 10 seconds	T_L	260	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD data available upon request.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = –40 to 85°C)

Parameter	Test Condition	Symbol	V_{DD} V	Guaranteed Limit	Unit
Power Supply Voltage Range		V_{DD}	–	2.7 to 5.5	V
Maximum Low–Level Input Voltage [Note 1] (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IL}	2.7 4.5 5.5	0.54 1.35 1.65	V
Minimum High–Level Input Voltage [Note 1] (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IH}	2.7 4.5 5.5	2.16 3.15 3.85	V
Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		V_{Hys}	2.7 5.5	0.15 0.20	V
Maximum Low–Level Output Voltage (Any Output)	I_{out} = 20 µA	V_{OL}	2.7 5.5	0.1 0.1	V
Minimum High–Level Output Voltage (Any Output)	I_{out} = – 20 µA	V_{OH}	2.7 5.5	2.6 5.4	V
Minimum Low–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	2.7 4.5 5.5	0.12 0.36 0.36	mA
Minimum High–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.4 V V_{out} = 4.1 V V_{out} = 5.0 V	I_{OH}	2.7 4.5 5.5	–0.12 –0.36 –0.36	mA
Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	I_{OL}	4.5	1.6	mA
Minimum High–Level Output Current (D_{out})	V_{out} = 4.1 V	I_{OH}	4.5	–1.6	mA
Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±1.0	µA
Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±150	µA
Maximum Output Leakage Current (PD_{out})	V_{in} = V_{DD} or V_{SS}, Output in High–Impedance State	I_{OZ}	5.5	±100	nA
(D_{out})			5.5	±5.0	µA
Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	I_{DD}	5.5	100	µA
Maximum Operating Supply Current	f_{in} = 500 mVpp; OSC_{in} = 1.0 MHz @ 1.0 Vpp; LD, f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out} = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	I_{dd}	–	[Note 2]	mA

NOTES: 1. When dc coupling to the OSC_{in} pin is used, the pin must be driven rail–to–rail. In this case, OSC_{out} should be floated.
2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

AC INTERFACE CHARACTERISTICS (T_A = –40 to 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	f_{clk}	1	2.7 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
Maximum Propagation Delay, CLK to D_{out}	t_{PLH}, t_{PHL}	1, 5	2.7 4.5 5.5	150 85 85	ns
Maximum Disable Time, D_{out} Active to High Impedance	t_{PLZ}, t_{PHZ}	2, 6	2.7 4.5 5.5	300 200 200	ns
Access Time, D_{out} High Impedance to Active	t_{PZL}, t_{PZH}	2, 6	2.7 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
Maximum Output Transition Time, D_{out} CL = 50 pF	t_{TLH}, t_{THL}	1, 5	2.7 4.5 5.5	150 50 50	ns
CL = 200 pF		1, 5	2.7 4.5 5.5	900 150 150	ns
Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK	C_{in}		–	10	pF
Maximum Output Capacitance – D_{out}	C_{out}		–	10	pF

TIMING REQUIREMENTS (T_A = –40 to 85°C, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Minimum Setup and Hold Times, D_{in} vs CLK	t_{su}, t_h	3	2.7 4.5 5.5	55 40 40	ns
Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	t_{su}, t_h, t_{rec}	4	2.7 4.5 5.5	135 100 100	ns
Minimum Inactive–High Pulse Width, $\overline{ENB}$	$t_{w(H)}$	4	2.7 4.5 5.5	400 300 300	ns
Minimum Pulse Width, CLK	t_w	1	2.7 4.5 5.5	166 125 125	ns
Maximum Input Rise and Fall Times, CLK	t_r, t_f	1	2.7 4.5 5.5	100 100 100	µs

SWITCHING WAVEFORMS

Figure 1.

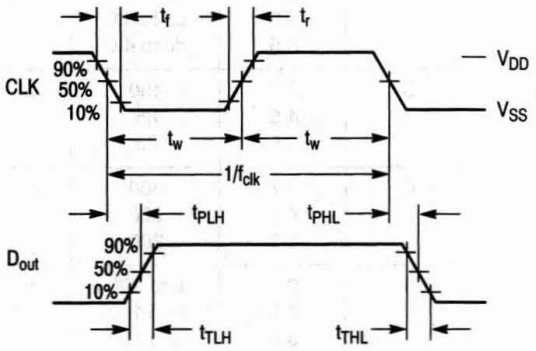


Figure 2.

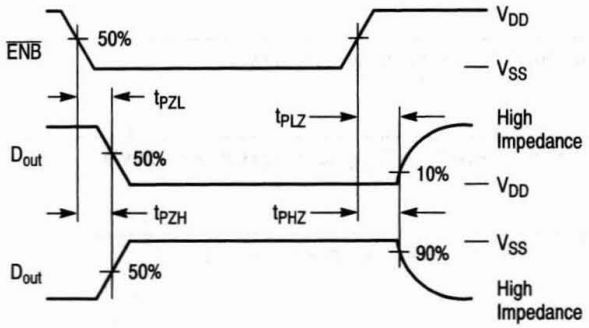


Figure 3.

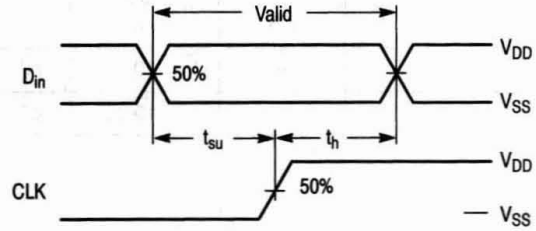


Figure 4.

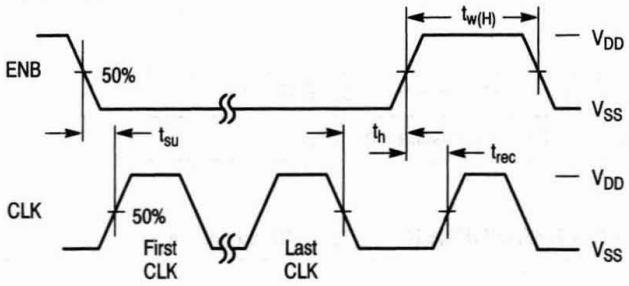
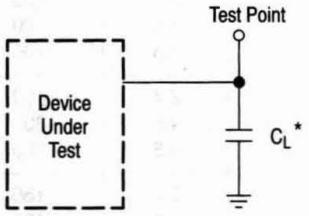
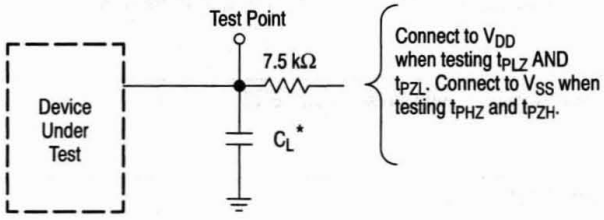


Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit



* Includes all probe and fixture capacitance.

LOOP SPECIFICATIONS (T_A = –40 to 85°C)

Parameter	Test Condition	Symbol	Figure No.	V_{DD} V	Guaranteed Range Min	Guaranteed Range Max	Unit
Input Frequency, f_{in} [Note}	V_{in} ≥ 500 mVpp Sine Wave, N Counter Set to Divide Ratio Such that f_V ≤ 2.0 MHz	f	7	2.7 3.0 4.5 5.5	5.0 5.0 25 45	80 100 185 185	MHz
Input Frequency, OSC_{in} Externally Driven with ac–coupled Signal	V_{in} ≥ 1.0 V_{pp} Sine Wave, OSC_{out} = No Connect, R Counter Set to Divide Ratio Such that f_R ≤ 2 MHz	f	8a	2.7 3.0 4.5 5.5	1.0* 1.0* 1.0* 1.0*	22 25 30 35	MHz
Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	f_{XTAL}	9	2.7 3.0 4.5 5.5	2.0 2.0 2.0 2.0	12 12 15 15	MHz
Output Frequency, REF_{out}	C_L = 30 pF	f_{out}	10, 12	2.7 4.5 5.5	dc dc dc	– 10 10	MHz
Operating Frequency of the Phase Detectors		f		2.7 4.5 5.5	dc dc dc	– 2.0 2.0	MHz
Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	t_w	11, 12	2.7 4.5 5.5	– 20 16	– 100 90	ns
Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	t_{TLH}, t_{THL}	11, 12	2.7 4.5 5.5	– – –	– 65 60	ns
Input Capacitance f_{in} OSC_{in}		C_{in}	– –	– –	– –	7.0 7.0	pF

* IF lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac–coupled case. Also, see Figure 22 for dc coupling.

Figure 7. Test Circuit, f_{in}

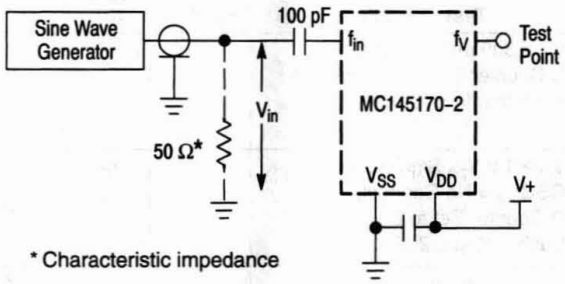


Figure 8.

Figure 8a. Test Circuit, OSC Circuit Externally Driven [Note]

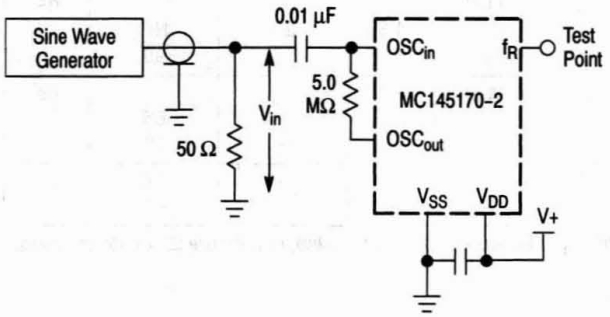


Figure 8b. Circuit to Eliminate Self–Oscillation, OSC Circuit Externally Driven [Note]

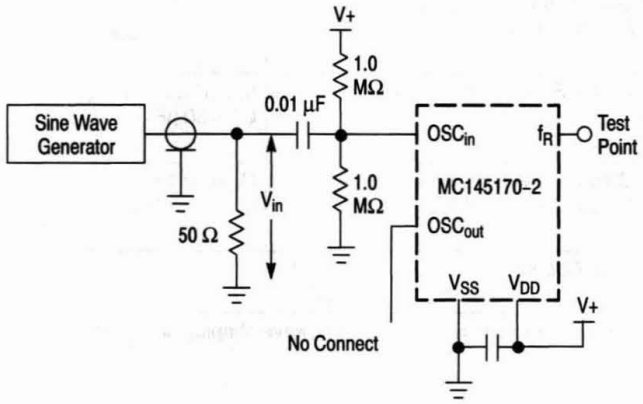


Figure 9. Test Circuit, OSC Circuit with Crystal

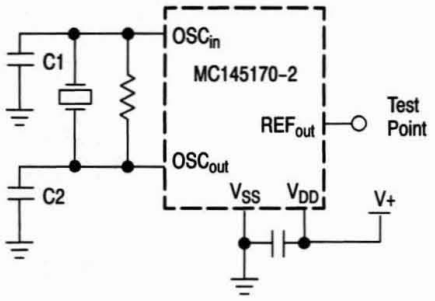


Figure 10. Switching Waveform

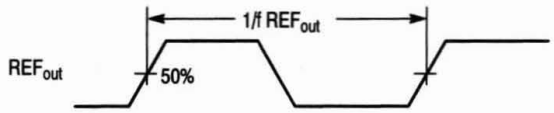


Figure 11. Switching Waveform

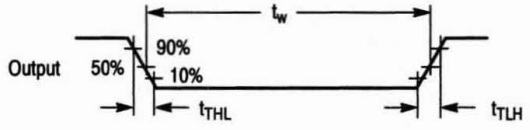
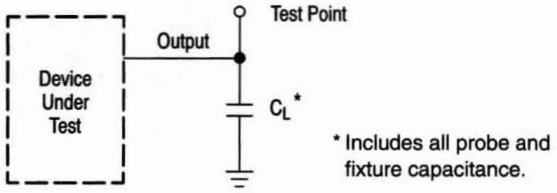


Figure 12. Test Load Circuit



NOTE: Use the circuit of Figure 8b to eliminate self–oscillation of the OSC_{in} pin when the MC145170–2 has power applied with no external signal applied at V_{in}. (Self–oscillation is not harmful to the MC145170–2 and does not damage the IC.)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}

Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15–bit transfer (see Table 1). An optional pattern which resets the device is shown in Figure 13. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 13, 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
9 to 13	See Figure 13	(Reset)
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤ 32	None	
Values > 32	See Figures 24 — 31	

CLK

Serial Data Clock Input (Pin 7)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 16–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four to eight clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, 15, and 16). For cascaded devices, see Figures 24 to 31.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.7 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 13 must be used.

$\overline{ENB}$

Active–Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}

Three–State Serial Data Output (Pin 8)

Data is transferred out of the 16–1/2–stage shift register through D_{out} on the high–to–low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in–line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

REFERENCE PINS

OSC_{in}/OSC_{out}

Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1.0 to 5.0 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 µF coupling capacitor is used for measurement purposes and is the minimum size

recommended for applications. An external feedback resistor of approximately 5 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case (see Figure 8a or alternate circuit 8b). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V p–p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings virtually rail–to–rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc–coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 22.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 14).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on–chip power–on–initialize circuit forces REF_{out} to the OSC_{in} divided–by–8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUT PINS

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15–stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 15). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high. The pulse width is 4.5 cycles of the OSC_{in} pin signal, except when a divide ratio of 1 is selected. When 1 is selected, the OSC_{in} signal is buffered and appears at the f_R pin.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16–stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

LOOP PINS

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on–chip amplifier which drives the N counter. This signal is normally sourced from an external voltage–controlled oscillator (VCO), and is ac–coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 22.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 13)

This is a three–state output for use as a loop error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double–Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 17).

This output can be enabled and disabled via the C register (patented). Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

V_{DD}
Most Positive Supply Potential (Pin 16)

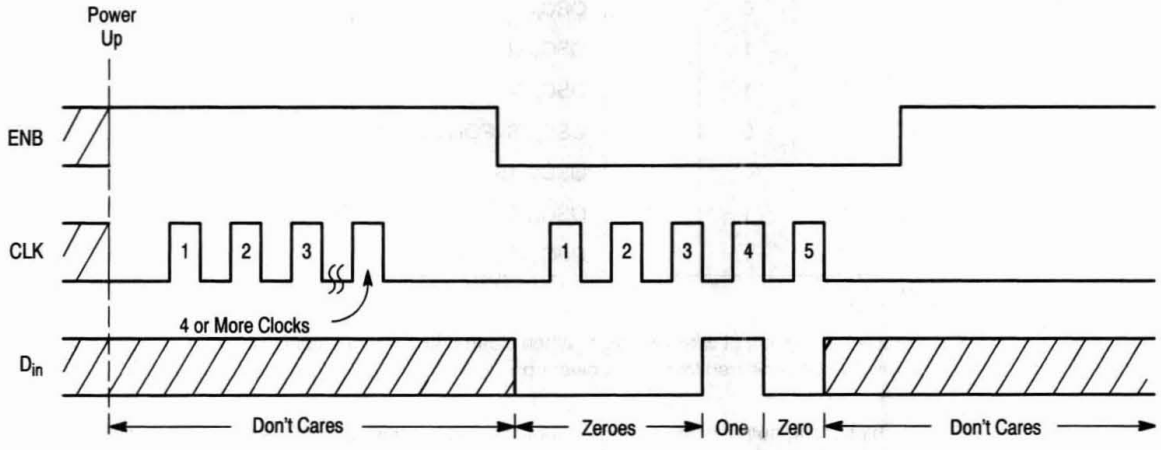
This pin may range from 2.7 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

V_{SS}
Most Negative Supply Potential (Pin 12)

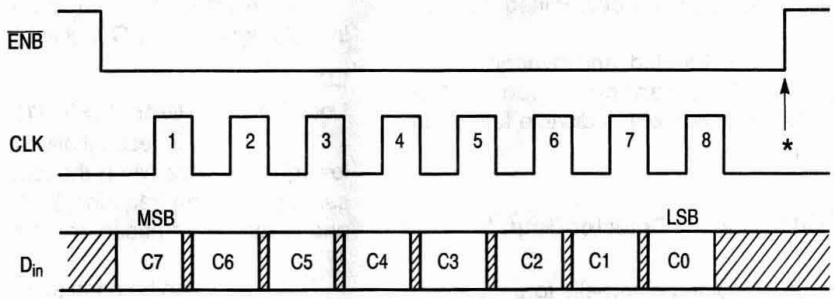
This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.

Figure 13. Reset Sequence



NOTE: This initialization sequence is usually not necessary because the on–chip power–on reset circuit performs the initialization function. However, this initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (Pin 7) toggles or floats upon power up, use the above sequence to reset the device. Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.7 V, but not down to at least 1 V (for example, the supply drops down to 2 V). This is necessary because the on–chip power–on reset is only activated when the supply ramps up from a voltage below approximately 1.0 V.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

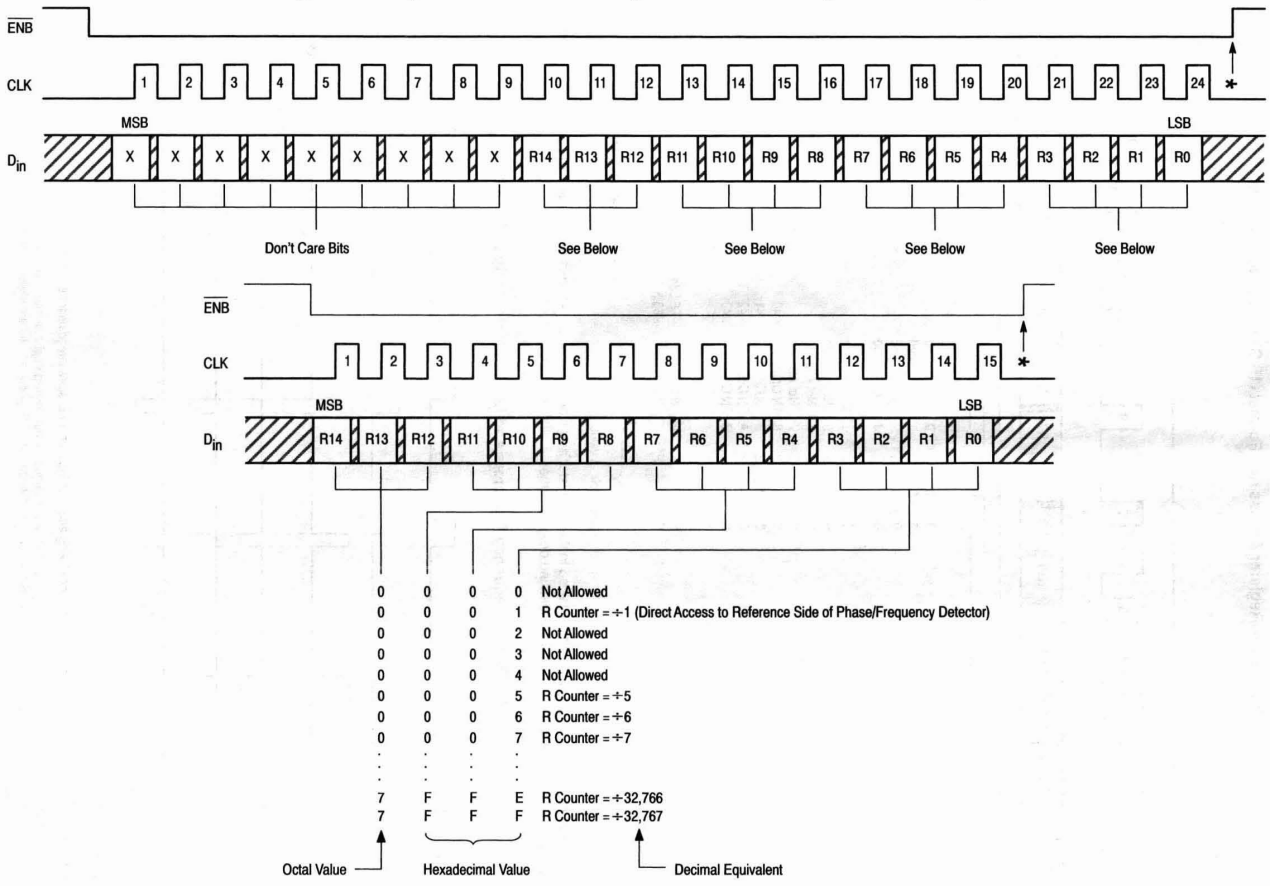
C4 – C2, OSC2 – OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$ (POR Default)
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 — f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

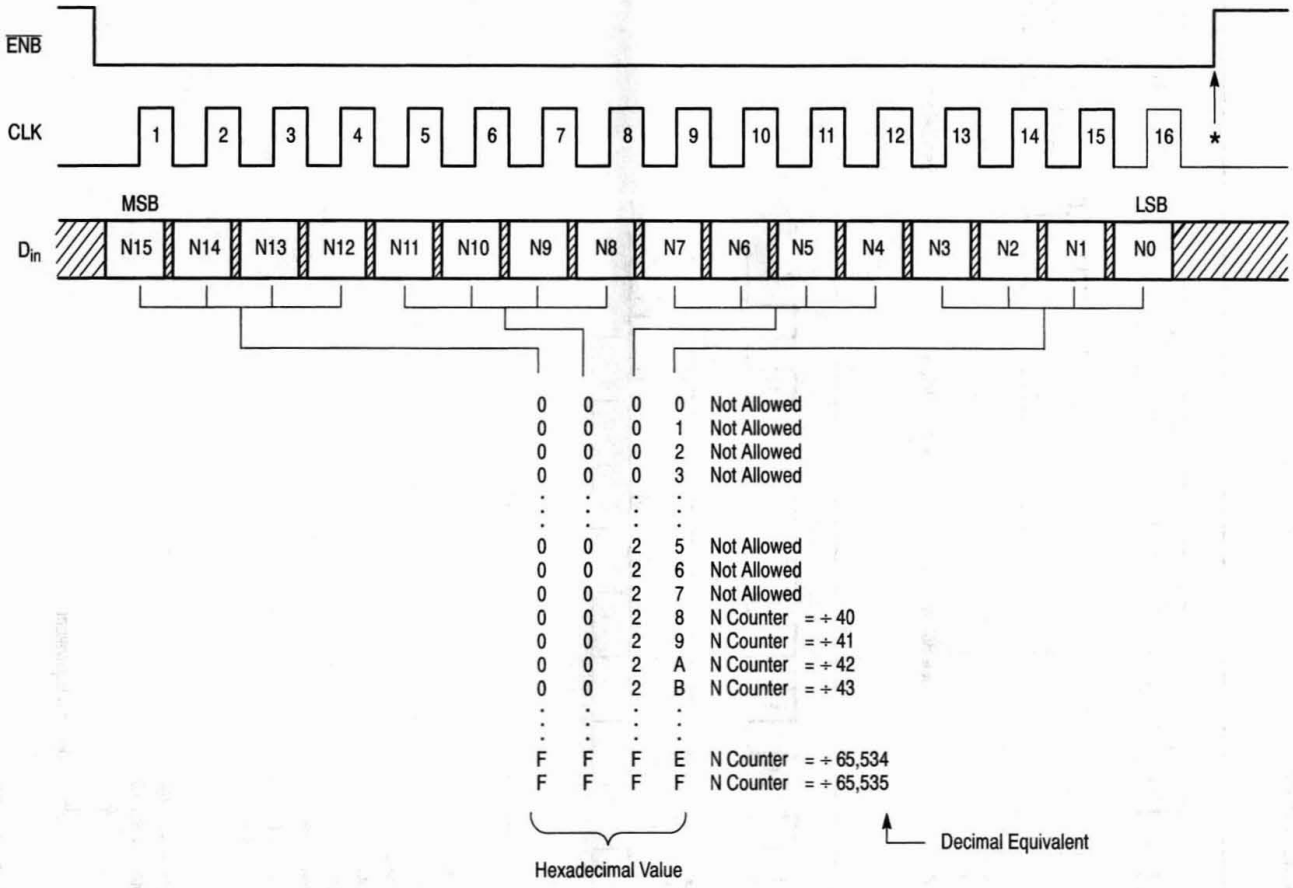
C0 — f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 15. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)



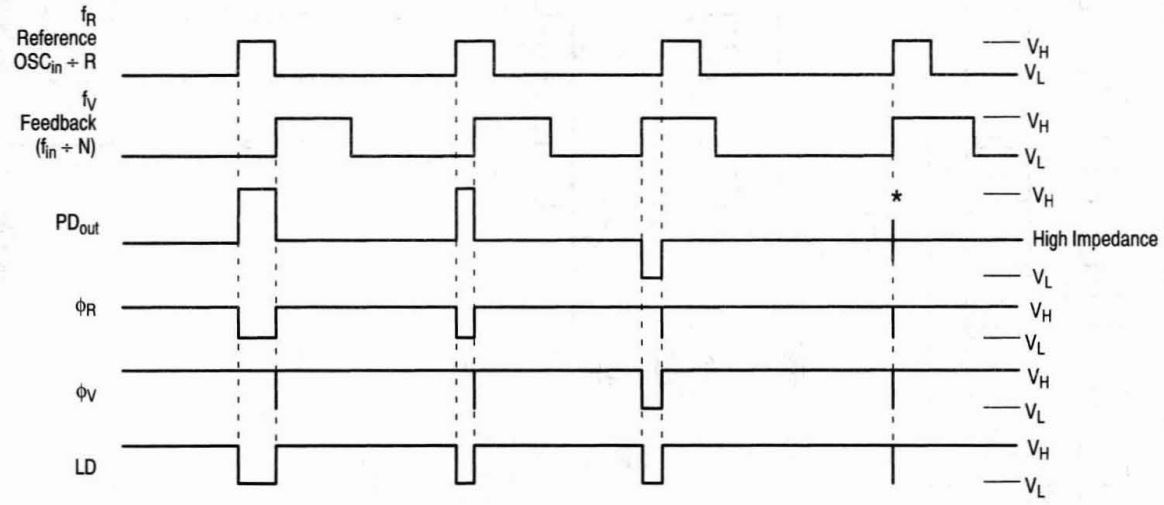
* At this point, the new data is transferred to the R register and stored. No other registers are affected.

Figure 16. N Register Access and Format (16 Clock Cycles Are Used)



* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam–loaded and begin counting down together.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.

NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figures 8a and 8b).

For additional information about TCXOs, visit *motorola.com* on the world wide web.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in the **Loop Specifications** table. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \times C2}{C1 + C2}$$

where

C_{in} = 5.0 pF (see Figure 19)
C_{out} = 6.0 pF (see Figure 19)
C_a = 1.0 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

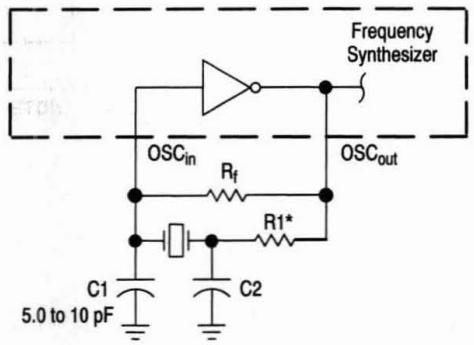
A good design practice is to pick a small value for C1, such as 5 to 10 pF. Next, C2 is calculated. C1 < C2 results in a more robust circuit for start–up and is more tolerant of crystal parameter variations.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).

Figure 18. Pierce Crystal Oscillator Circuit



* May be needed in certain cases. See text.

Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}

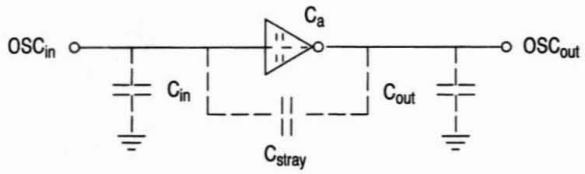
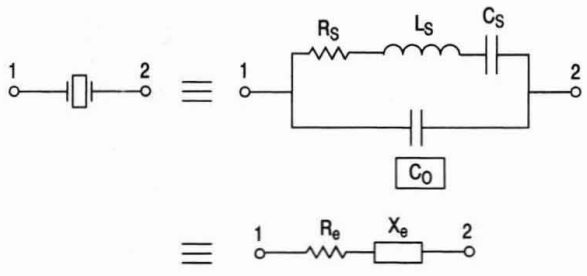


Figure 20. Equivalent Crystal Networks



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

See web site *mot–sps.com* for MC145170–2 control software. Select in order, Products, Wireless Semiconductor, Download, then PLL Demo Software. Choose PLLGEN.EXE.

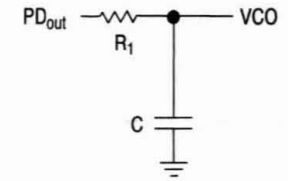
Table 2. Partial List of Crystal Manufacturers

CTS Corp.
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW PASS FILTER DESIGN

(A)

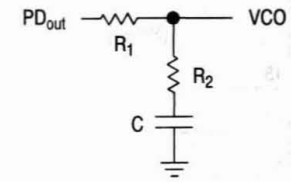


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

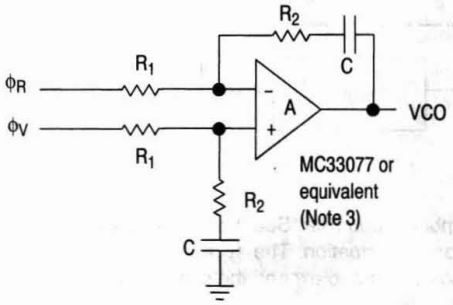


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming Gain A Is Very Large, Then:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTES:

8 For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

9 The ϕR and ϕV outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp.

10 For the latest information on MC33077 or equivalent, see the Motorola Analog IC web site at *http://www.mot–sps.com/analog*.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ volts per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ volts per radian for ϕ_V and ϕ_R

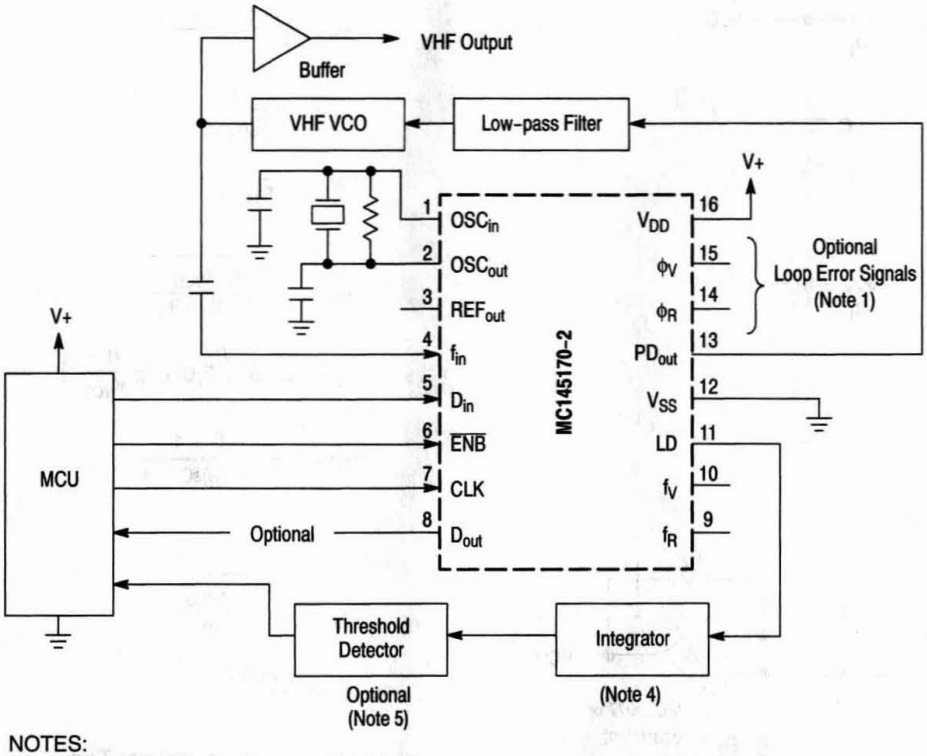
$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design*. New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN*. March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.
AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.
AN1671, MC145170 PSpice Modeling Kit, Motorola Semiconductor Products, Inc., 1998.

Figure 21. Example Application



NOTES:

1 The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

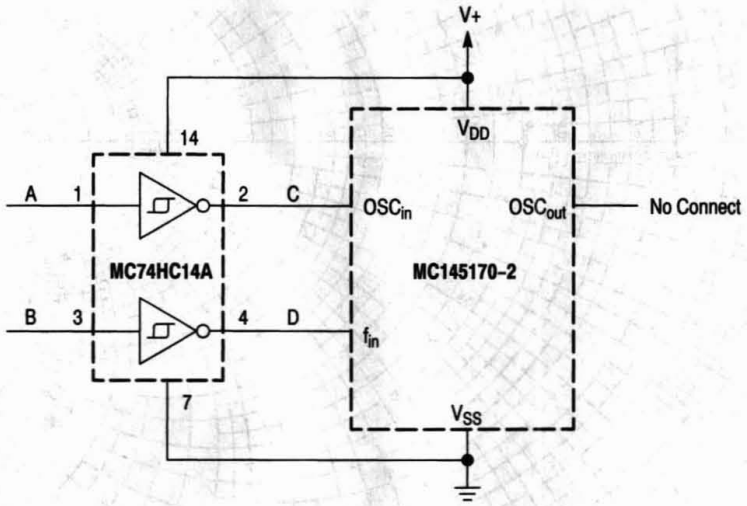
2 For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low–inductance capacitors.

3 The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, where N is the divide value of the N counter.

4 May be an R–C low–pass filter.

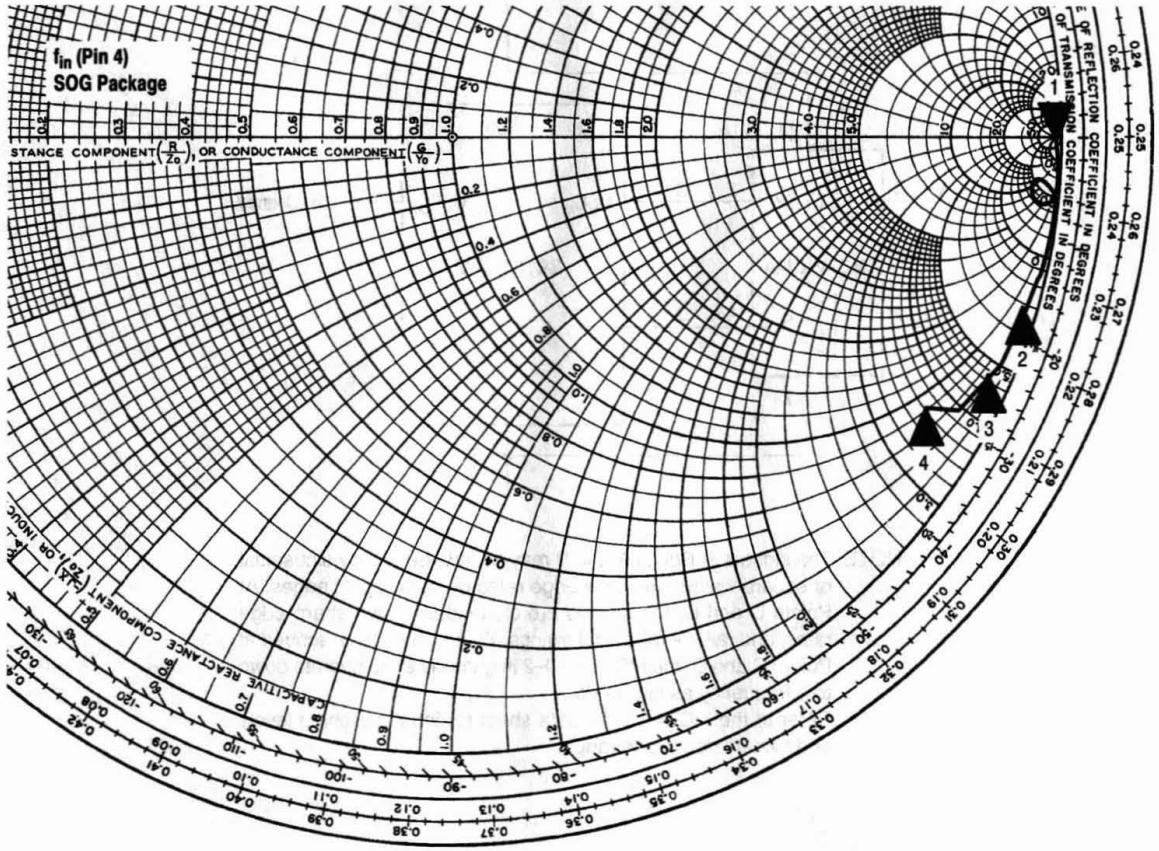
5 May be a bipolar transistor.

Figure 22. Low Frequency Operation Using dc Coupling



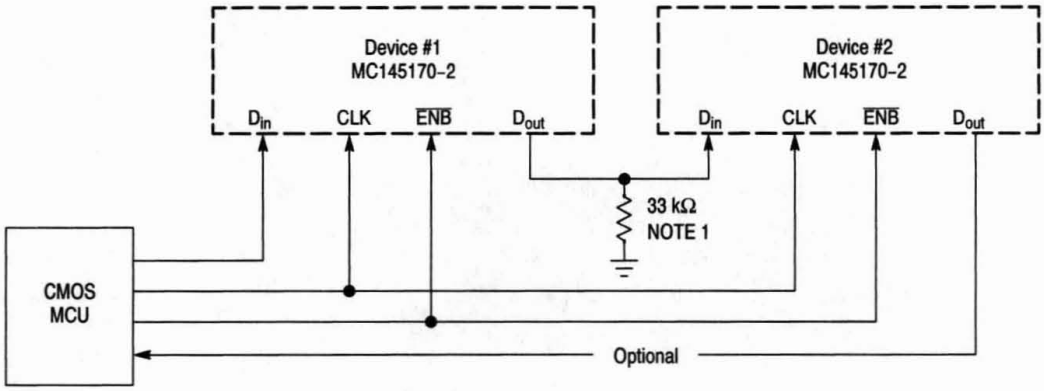
NOTE: The signals at Points A and B may be low–frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail–to–rail signal swings. With signals as described at Points C and D, the MC145170–2 is guaranteed to operate down to a frequency as low as dc.
Refer to the MC74HC14A data sheet for input switching levels and hysteresis voltage range.

Figure 23. Input Impedance at f_{in} — Series Format (R + jX)
(5.0 MHz to 185 MHz)



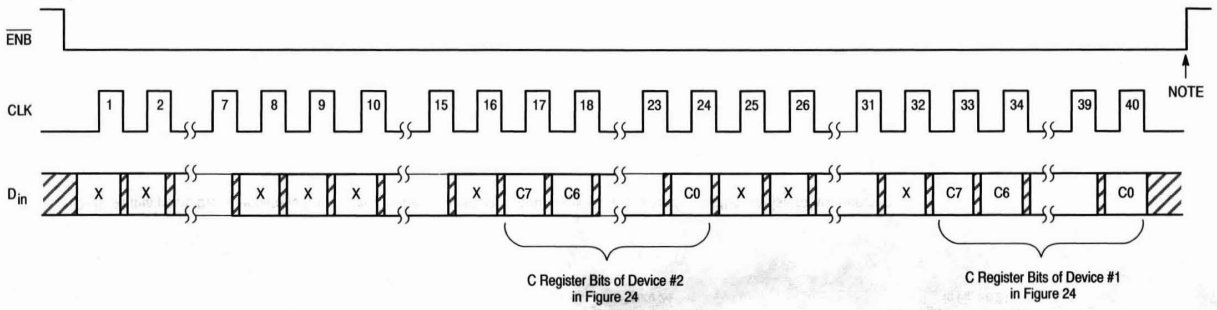
Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	- 5900	5.39
2	100	39.2	- 347	4.58
3	150	25.8	- 237	4.48
4	185	42.6	- 180	4.79

Figure 24. Cascading Two MC145170–2 Devices



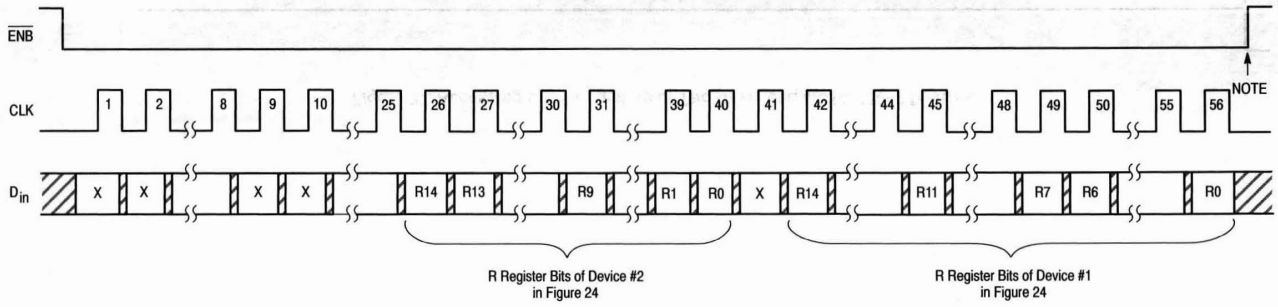
NOTES:
1 The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2 See related Figures 25, 26, and 27.

Figure 25. Accessing the C Registers of Two Cascaded MC145170–2 Devices



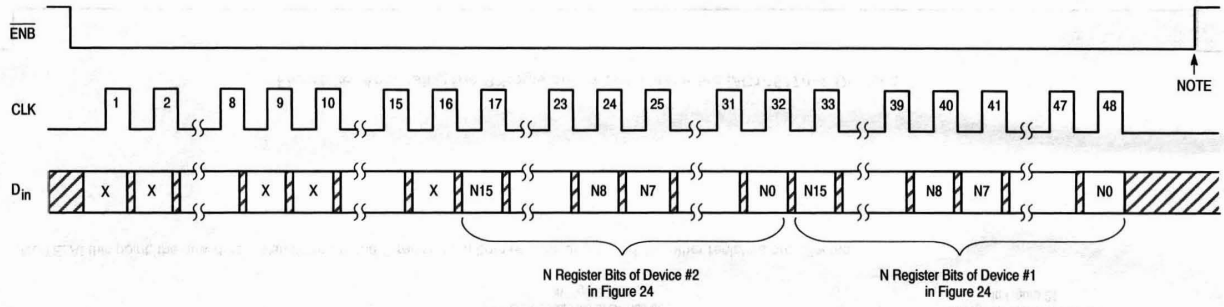
NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 26. Accessing the R Registers of Two Cascaded MC145170–2 Devices



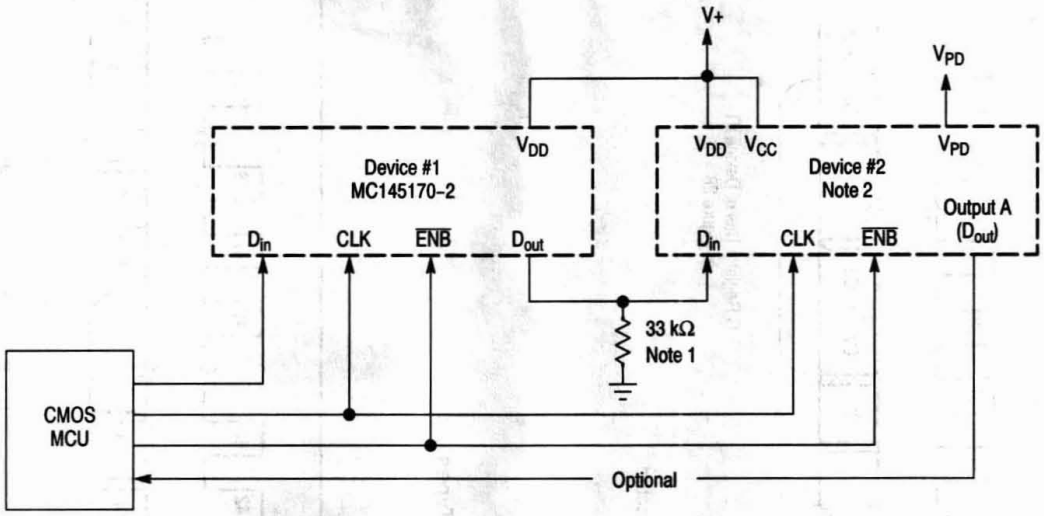
NOTE: At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

Figure 27. Accessing the N Registers of Two Cascaded MC145170–2 Devices



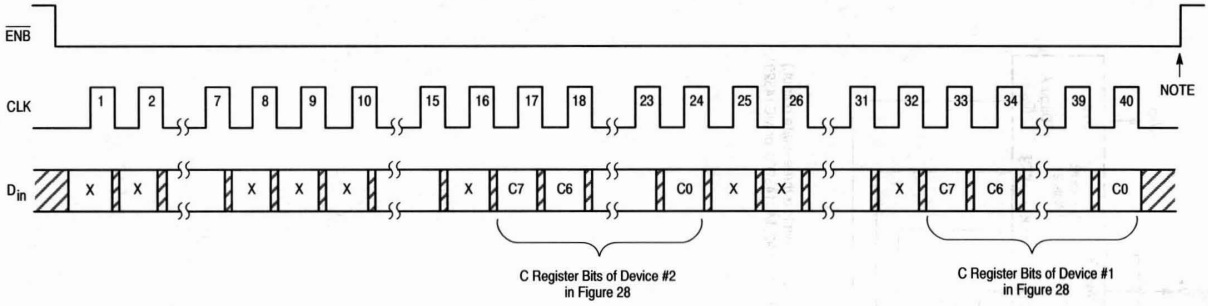
NOTE: At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

Figure 28. Cascading Two Different Device Types



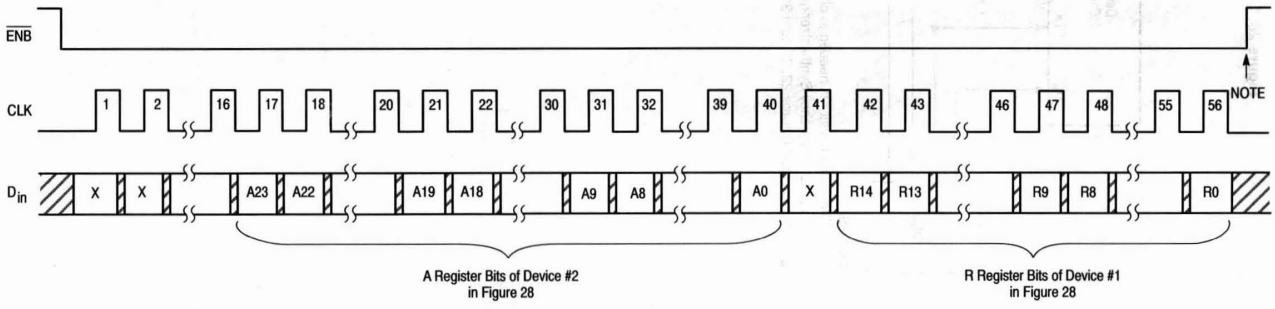
NOTES:
1 The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2 This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3 See related Figures 29, 30, and 31.

Figure 29. Accessing the C Registers of Two Different Device Types



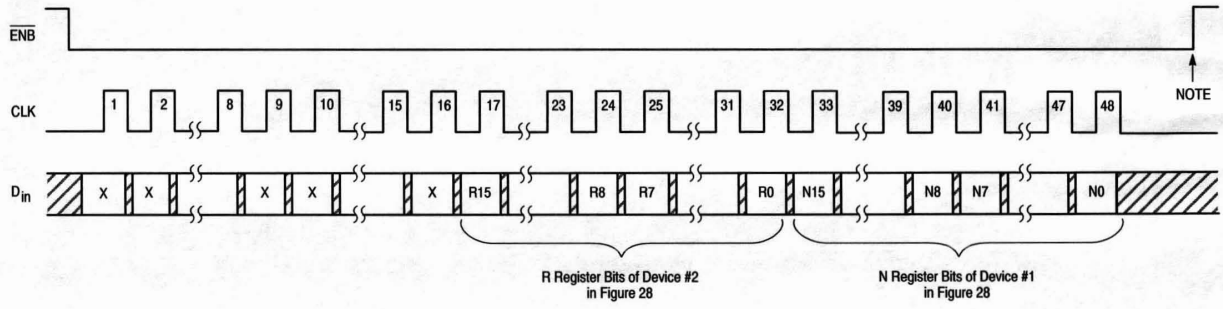
NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 30. Accessing the A and R Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.

Figure 31. Accessing the R and N Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.

Chapter Five
RF Transistors

Section One **5.1–0**
RF Transistors – Selector Guide

Section Two **5.2–0**
RF Transistors – Data Sheets

Section One
Selector Guide

Motorola RF Transistors

Motorola continues to be an industry leader in RF transistor technology. Our current portfolio ranges from high gain and low noise devices at microwave frequencies to high power devices for fixed RF and microwave applications. Technical innovation combined with world–class manufacturing capability allows Motorola to offer world class product, service and support to its customers.

From our LDMOS and GaAs portfolio, the user can choose from a variety of packages. They include plastic and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.

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Motorola RF Transistors

RF High Power LDMOS Transistors

Motorola LDMOS technology is ideally suited for RF power amplifier applications. Several families of products have been targeted for specific markets including VHF and UHF portable/land mobile, 900 MHz linear cellular, GSM, TDMA and CDMA, digital television, GSM EDGE, PCS, UMTS, and W–CDMA.

With the unique LDMOS characteristics, these parts offer superior thermal performance. This is due to the simplified package design, which offers excellent Class AB intermodulation performance under medium peak–to–average ratios providing a superior device choice for advanced digital modulations formats or high gain applications.

Table 1. Mobile – To 520 MHz

Designed for broadband VHF and UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 12.5/7.5 volt mobile, portable and base station operation.

Product	Frequency Band[37]		P_{out} Watts	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Package/Style
VHF & UHF, Land Mobile Radio, Class AB								
MRF1511T1[18f]	U	136–175	8	7.5	11.5/175	55	2.0	466/1
MRF1517T1[18f]	U	430–520	8	7.5	11/520	55	2.0	466/1
MRF1513T1[18f]	U	400–520	3	7.5/12.5	11/520	55	4.0	466/1
MRF1518T1[18f]	U	400–520	8	12.5	11/520	55	2.0	466/1
MRF1535T1[18j]	U	400–520	35	12.5	10(Min)/520	50(Min)	0.90	1264/1
MRF1550T1[18j]	U	136–175	50	12.5	10(Min)/175	50(Min)	0.75	1264/1

Table 2. TV Broadcast – To 1.0 GHz

Product	Frequency Band[37]		P_{out} Watts	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	IMD dBc	Package/Style
470 – 1000 MHz, Class AB									
MRF373A★	U	470–860	75 CW	32	18.2/860	60	0.89	—	360B/1
MRF373AS★	U	470–860	75 CW	32	18.2/860	60	0.63	—	360C/1
MRF374A★	U	470–860	130 PEP	32	17.3/860	41	0.58	–31	375F/1
MRF372	M	470–860	180 PEP	32	17/860	36	0.5	–35	375G/1
MRF377[46b]	M	470–860	240 PEP	32	16/860	40	0.5	–30	375G/1

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

★New Product

Table 3. Cellular – To 1.0 GHz

Product	Frequency Band[37]	P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
800 – 1.0 GHz, Class AB								
MRF9002R2[18e]★	U	960	(3x) 2 PEP[41]	2–Tone	26	16/960	50	12	978/–
MRF9030MBR1[18a,46b]	U	945	30 PEP	2–Tone	26	19.2/945	41	1.08	1337/1
MRF9030MR1[18a]★	U	945	30 PEP	2–Tone	26	19.2/945	41	1.08	1265/1
MRF9030★	U	945	30 PEP	2–Tone	26	19/945	41.5	1.9	360B/1
MRF9030S★	U	945	30 PEP	2–Tone	26	19/945	41.5	1.5	360C/1
MRF9030SR1[18a]★	U	945	30 PEP	2–Tone	26	19/945	41.5	1.5	360C/1
MRF9045MBR1[18a]★	U	945	45 PEP	2–Tone	28	19/945	41	0.85	1337/1
MRF9045MR1[18a]	U	945	45 PEP	2–Tone	28	19/945	41	0.85	1265/1
MRF9045	U	945	45 PEP	2–Tone	28	18.8/945	42	1.4	360B/1
MRF9045S	U	945	45 PEP	2–Tone	28	18.8/945	42	1.0	360C/1
MRF9045SR1[18a]	U	945	45 PEP	2–Tone	28	18.8/945	42	1.0	360C/1
MRF9060MBR1[18a]★	U	945	60 PEP	2–Tone	26	18/945	40	0.56	1337/1
MRF9060MR1[18a,46b]	U	945	60 PEP	2–Tone	26	18/945	40	0.56	1265/1
MRF9060★	U	945	60 PEP	2–Tone	26	17/945	40	1.1	360B/1
MRF9060S★	U	945	60 PEP	2–Tone	26	17/945	40	0.8	360C/1
MRF9060SR1[18a]★	U	945	60 PEP	2–Tone	26	17/945	40	0.8	360C/1
MRF6522–70	M	921–960	70 CW	1–Tone	26	16/921,960	58	1.1	465D/1
MRF6522–70R3[18i]	M	921–960	70 CW	1–Tone	26	16/921,960	58	1.1	465D/1
MRF9080	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465/1
MRF9080R3[18i]	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465/1
MRF9080S	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465A/1
MRF9080SR3[18i]	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465A/1
MRF9080LSR3[18i]★	M	921–960	75 CW	1–Tone	26	18.5/921,960	55	0.7	465A/1
MRF9085	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465/1
MRF9085R3[18i]	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465/1
MRF9085S	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465A/1
MRF9085SR3[18i]	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465A/1
MRF9085LS★	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465A/1
MRF9085LSR3[18i]★	M	880	90 PEP	2–Tone	26	17.9/880	40	0.7	465A/1
MRF9100[46a]	M	921–960	100 CW	1–Tone	26	17/960	51	1.0	465/1
MRF9100R3[18i,46a]	M	921–960	100 CW	1–Tone	26	17/960	51	1.0	465/1
MRF9100S[46a]	M	921–960	100 CW	1–Tone	26	17/960	51	1.0	465A/1
MRF9100SR3[18i,46a]	M	921–960	100 CW	1–Tone	26	17/960	51	1.0	465A/1
MRF9120★	M	880	120 PEP	2–Tone	26	16.5/880	39	0.45	375B/1
MRF9120S★	M	880	120 PEP	2–Tone	26	16.5/880	39	0.45	375H/1
MRF9130L[46b]	M	921–960	130 CW	1–Tone	28	16/921,960	48	0.6	465/1
MRF9130LR3[18i,46b]	M	921–960	130 CW	1–Tone	28	16/921,960	48	0.6	465/1
MRF9130LS[46b]	M	921–960	130 CW	1–Tone	28	16/921,960	48	0.6	465A/1
MRF9130LSR3[18i,46b]	M	921–960	130 CW	1–Tone	28	16/921,960	48	0.6	465A/1
MRF9135L[46a]	M	880	25 AVG	N–CDMA	26	17/880	25	0.6	465/1
MRF9135LR3[18i,46a]	M	880	25 AVG	N–CDMA	26	17/880	25	0.6	465/1
MRF9135LS[46a]	M	880	25 AVG	N–CDMA	26	17/880	25	0.6	465A/1
MRF9135LSR3[18i,46a]	M	880	25 AVG	N–CDMA	26	17/880	25	0.6	465A/1
MRF9180	M	880	170 PEP	2–Tone	26	17.5/880	39	0.45	375D/1
MRF9180S	M	880	170 PEP	2–Tone	26	17.5/880	39	0.45	375E/1
MRF9210[46b]	M	880	200 PEP	2–Tone	26	15/880	39	0.5	375G/1

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[41]Three individual transistors in a single package.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

★New Product

Table 4. PCS and 3G – To 2.1 GHz

Product	Frequency Band[37]		P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
1805 – 1990 MHz, Class AB (GSM1800, GSM1900, GSM EDGE and PCS TDMA)									
MRF18030A★	M	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465E/1
MRF18030AR3[18i]★	M	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465E/1
MRF18030AS★	M	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465F/1
MRF18030ASR3[18i]★	M	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465F/1
MRF18030B★	M	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465E/1
MRF18030BR3[18i]★	M	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465E/1
MRF18030BS★	M	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465F/1
MRF18030BSR3[18i]★	M	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465F/1
MRF18060A	M	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465/1
MRF18060AR3[18i]	M	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465/1
MRF18060AS	M	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465A/1
MRF18060ASR3[18i]	M	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465A/1
MRF18060B	M	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465/1
MRF18060BR3[18i]	M	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465/1
MRF18060BS	M	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465A/1
MRF18060BSR3[18i]	M	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465A/1
MRF18085A[46b]	M	1805–1880	85 CW	1–Tone	26	13/1805,1880	53	0.64	465/1
MRF18085AS[46b]	M	1805–1880	85 CW	1–Tone	26	13/1805,1880	53	0.64	465A/1
MRF18085B[46a]	M	1930–1990	85 CW	1–Tone	26	13/1930,1990	52	0.64	465/1
MRF18085BS[46b]	M	1930–1990	85 CW	1–Tone	26	13/1930,1990	52	0.64	465A/1
MRF18090A	M	1805–1880	90 CW	1–Tone	26	13.5/1805,1880	52	0.7	465B/1
MRF18090AS	M	1805–1880	90 CW	1–Tone	26	13.5/1805,1880	52	0.7	465C/1
MRF18090B	M	1930–1990	90 CW	1–Tone	26	13.5/1930,1990	45	0.7	465B/1
MRF18090BS	M	1930–1990	90 CW	1–Tone	26	13.5/1930,1990	45	0.7	465C/1
1.9 GHz, Class AB (2–CH N–CDMA)									
MRF19030	M	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465E/1
MRF19030R3[18i]	M	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465E/1
MRF19030S	M	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465F/1
MRF19030SR3[18i]	M	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465F/1
MRF19045★	M	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	0.65	465E/1
MRF19045R3[18i]★	M	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	0.65	465E/1
MRF19045S★	M	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	0.65	465F/1
MRF19045SR3[18i]★	M	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	0.65	465F/1
MRF19060	M	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465/1
MRF19060R3[18i]	M	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465/1
MRF19060S	M	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465A/1
MRF19060SR3[18i]	M	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465A/1
MRF19090	M	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465B/1
MRF19090S	M	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465C/1
MRF19090SR3[18i]	M	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465C/1
MRF19085	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465/1
MRF19085R3[18i]	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465/1
MRF19085S	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19085SR3[18i]	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19085LS★	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19085LSR3[18i]★	M	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19120[3]	M	1930–1990	120 PEP	2–Tone	26	11.7/1990	34	0.45	375D/1
MRF19120S[3]	M	1930–1990	120 PEP	2–Tone	26	11.7/1990	34	0.45	375E/1

[3]Internal Impedance Matched Push-Pull Transistors

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

★New Product

Table 4. PCS and 3G – To 2.1 GHz (continued)

Product	Frequency Band[37]		P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
1.9 GHz, Class AB (2–CH N–CDMA) (continued)									
MRF19125	M	1930–1990	24 AVG	N–CDMA	26	13.5/1990	22	0.53	465B/1
MRF19125S	M	1930–1990	24 AVG	N–CDMA	26	13.5/1990	22	0.53	465C/1
MRF19125SR3[18i]	M	1930–1990	24 AVG	N–CDMA	26	13.5/1990	22	0.53	465C/1
MRF5S19150[46c]	M	1930–1990	34 AVG	W–CDMA	28	13.6/1990	26	—	465B/1
MRF5S19150S[46c]	M	1930–1990	34 AVG	W–CDMA	28	13.6/1990	26	—	465C/1
MRF19180[46b]	M	1930–1990	40 AVG	N–CDMA	26	11.4/1990	22	0.46	375D/1
MRF19180S[46b]	M	1930–1990	40 AVG	N–CDMA	26	11.4/1990	22	0.46	375E/1
2.0 GHz, Class A, AB									
MRF281SR1[18a]	U	1930–2000	4 PEP	2–Tone	26	12.5/2000	33	5.74	458B/1
MRF281ZR1[18a]	U	1930–2000	4 PEP	2–Tone	26	12.5/2000	33	5.74	458C/1
MRF282SR1[18a]	U	1930–2000	10 PEP	2–Tone	26	11.5/2000	28(min)	4.2	458B/1
MRF282ZR1[18a]	U	1930–2000	10 PEP	2–Tone	26	11.5/2000	28(min)	4.2	458C/1
MRF284	U	1930–2000	30 PEP	2–Tone	26	10.5/2000	35	2.0	360B/1
MRF284SR1[18a]	U	1930–2000	30 PEP	2–Tone	26	10.5/2000	35	2.0	360C/1
MRF286[46a]	M	1930–2000	60 PEP	2–Tone	26	10.5/2000	32	0.73	465/1
MRF286S[46a]	M	1930–2000	60 PEP	2–Tone	26	10.5/2000	32	0.73	465A/1
2.1 GHz, Class AB (2–CH W–CDMA, UMTS)									
MRF21010	U	2110–2170	10 PEP	2–Tone	28	13.5/2170	35	5.5	360B/1
MRF21010S★	U	2110–2170	10 PEP	2–Tone	28	13.5/2170	35	5.5	360C/1
MRF21030	M	2110–2170	30 PEP	2–Tone	28	13/2170	33	2.1	465E/1
MRF21030R3[18i]	M	2110–2170	30 PEP	2–Tone	28	13/2170	33	2.1	465E/1
MRF21030S	M	2110–2170	30 PEP	2–Tone	28	13/2170	33	2.1	465F/1
MRF21030SR3[18i]	M	2110–2170	30 PEP	2–Tone	28	13/2170	33	2.1	465F/1
MRF21045	M	2110–2170	10 AVG	W–CDMA	28	15/2170	23.5	1.65	465E/1
MRF21045R3[18i]	M	2110–2170	10 AVG	W–CDMA	28	15/2170	23.5	1.65	465E/1
MRF21045S	M	2110–2170	10 AVG	W–CDMA	28	15/2170	23.5	1.65	465F/1
MRF21045SR3[18i]	M	2110–2170	10 AVG	W–CDMA	28	15/2170	23.5	1.65	465F/1
MRF21060	M	2110–2170	60 PEP	2–Tone	28	12.5/2170	34	1.02	465/1
MRF21060R3[18i]	M	2110–2170	60 PEP	2–Tone	28	12.5/2170	34	1.02	465/1
MRF21060S	M	2110–2170	60 PEP	2–Tone	28	12.5/2170	34	1.02	465/1
MRF21060SR3[18i]	M	2110–2170	60 PEP	2–Tone	28	12.5/2170	34	1.02	465A/1
MRF21085	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465/1
MRF21085LS★	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465A/1
MRF21085LSR3[18i]★	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465A/1
MRF21085S	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465A/1
MRF21085SR3[18i]	M	2110–2170	19 AVG	W–CDMA	28	13.6/2170	23	0.78	465A/1
MRF21090	M	2110–2170	90 PEP	2–Tone	28	11.7/2170	33	0.65	465B/1
MRF21090S	M	2110–2170	90 PEP	2–Tone	28	11.7/2170	33	0.65	465C/1
MRF21120[3]	M	2110–2170	120 PEP	2–Tone	28	11.4/2170	34.5	0.45	375D/1
MRF21120S[3]	M	2110–2170	120 PEP	2–Tone	28	11.2/2170	34.5	0.45	375E/1
MRF21125	M	2110–2170	20 AVG	W–CDMA	28	13/2170	18	0.53	465B/1
MRF21125S	M	2110–2170	20 AVG	W–CDMA	28	13/2170	18	0.53	465C/1
MRF21125SR3[18i]	M	2110–2170	20 AVG	W–CDMA	28	13/2170	18	0.53	465C/1
MRF21180[3]★	M	2110–2170	38 AVG	W–CDMA	28	12.1/2170	22	0.46	375D/1
MRF21180S[3]★	M	2110–2170	38 AVG	W–CDMA	28	12.1/2170	22	0.46	375E/1

[3]Internal Impedance Matched Push-Pull Transistors

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

★New Product

Table 4. PCS and 3G – To 2.1 GHz (continued)

Product	Frequency Band[37]	P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
2.1 GHz, Class AB (2–CH W–CDMA, UMTS) (continued)								
MRF5S21090[46c]	M	2110–2170	19 AVG	W–CDMA	28	14.5/2170	26	—	465/1
MRF5S21090S[46c]	M	2110–2170	19 AVG	W–CDMA	28	14.5/2170	26	—	465A/1
MRF5S21090L[46c]	M	2110–2170	19 AVG	W–CDMA	28	14.5/2170	26	—	465/1
MRF5S21090LS[46c]	M	2110–2170	19 AVG	W–CDMA	28	14.5/2170	26	—	465A/1
MRF5S21100[46c]	M	2110–2170	23 AVG	W–CDMA	28	13.5/2170	26	—	465/1
MRF5S21100S[46c]	M	2110–2170	23 AVG	W–CDMA	28	13.5/2170	26	—	465A/1
MRF5S21100L[46c]	M	2110–2170	23 AVG	W–CDMA	28	13.5/2170	26	—	465/1
MRF5S21100LS[46c]	M	2110–2170	23 AVG	W–CDMA	28	13.5/2170	26	—	465A/1
MRF5S21150[46c]	M	2110–2170	35 AVG	W–CDMA	28	13/2170	26	—	465B/1
MRF5S21150S[46c]	M	2110–2170	35 AVG	W–CDMA	28	13/2170	26	—	465C/1
MRF5P21180[46c]	M	2110–2170	38 AVG	W–CDMA	28	13.5/2170	25	—	375D/1
MRF5P21180S[46c]	M	2110–2170	38 AVG	W–CDMA	28	13.5/2170	25	—	375E/1
MRF5P21240[46c]	M	2110–2170	55 AVG	W–CDMA	28	13/2170	25	—	375D/1
MRF5P21240S[46c]	M	2110–2170	55 AVG	W–CDMA	28	13/2170	25	—	375E/1

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

RF Power GaAs Transistors

Motorola power GaAs transistors are made using an InGaAs PHEMT epitaxial structure for superior RF efficiency and linearity. The FETs listed in this section are designed for operation in base station infrastructure RF power amplifiers and are grouped according to frequency range and type of application. Parts are listed first by order of operating voltage, then by increasing output power.

Table 1. 3.5 GHz – Linear Transistors

Product	Frequency Band[37]	P_{out} Watts	Test Signal	V_{DD} Volts	Gain (Typ)/Freq. dB/GHz	η Eff. (Typ) %	θ_{JC} °C/W	Pkg/ Style
3.5 GHz, Class AB (WLL, BWA, W–CDMA)								
MRFG35010★	U	3.5 G	1 AVG	W–CDMA	12	10/3.5	26	5.8	360D/1
MRFG35030[9]	M	3.5 G	4 AVG	W–CDMA	12	10/3.5	26	—	—

[9]In development.

[37]M = Matched Frequency Band; U = Unmatched Frequency Band.

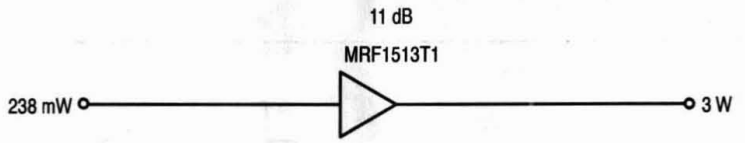
★New Product

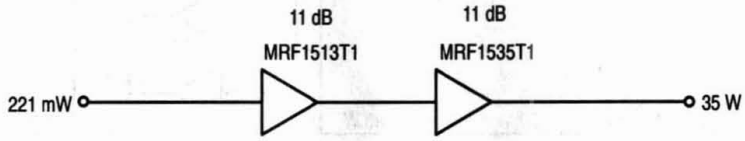
RF Low Power Transistors

Product	Gain – Bandwidth		NFmin @ f		Gain @ f		Maximum Ratings		Packaging
	f_τ Typ GHz	I_C mA	Typ dB	GHz	Typ dB	GHz	V(BR) CEO Volts	I_C mA	
MBC13900[46b]	15	20	1.0	1.0	17	1.0	7.0	20	318M/ SOT–343
			1.3	2.0	14	2.0			

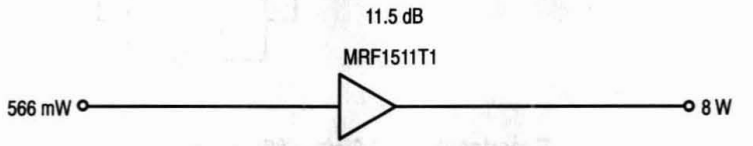
[46]To be introduced: a) 1Q02; b) 2Q02; c) 3Q02

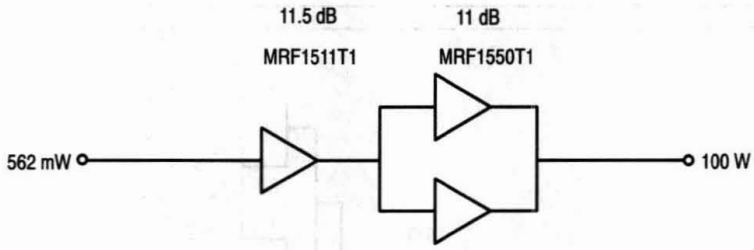
RF High Power Amplifier LDMOS Line–ups



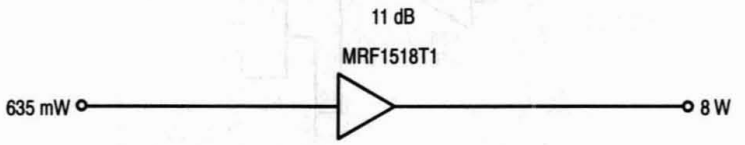


Mobile – UHF

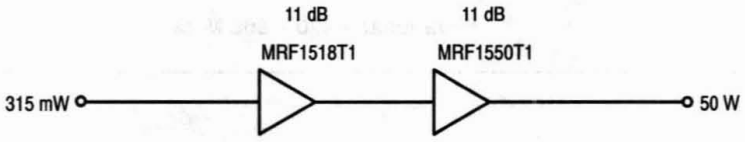




Mobile – VHF

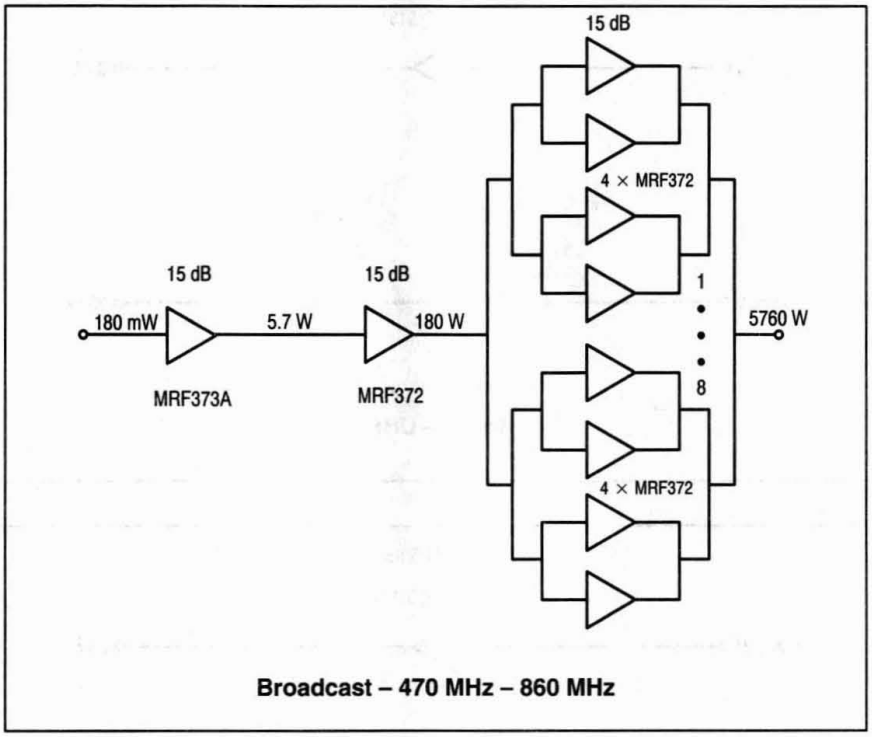


Mobile – UHF

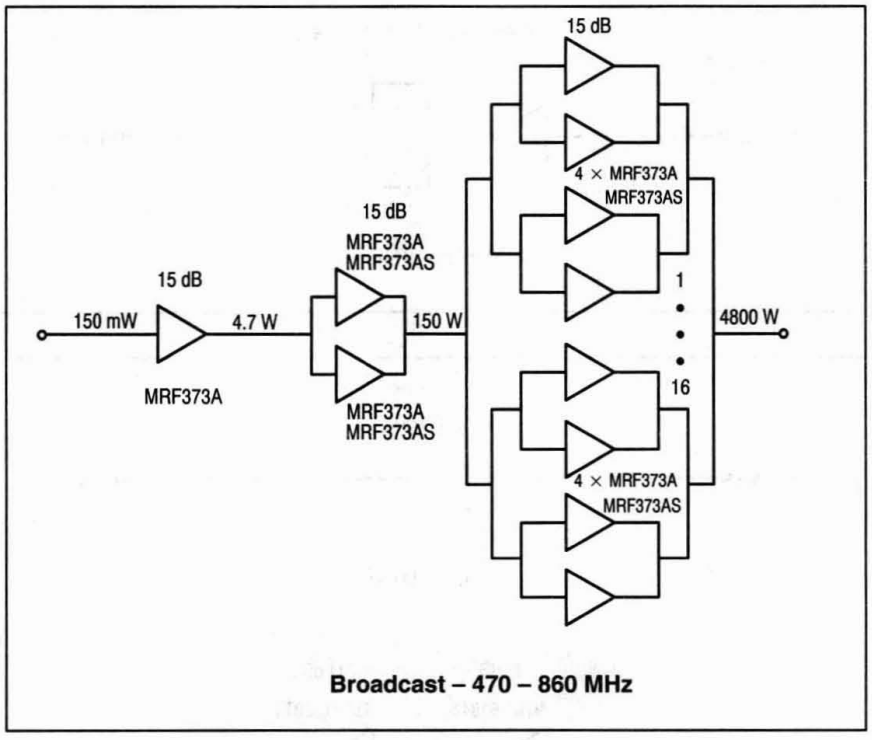


Mobile – VHF

RF High Power Amplifier LDMOS Line–ups (continued)

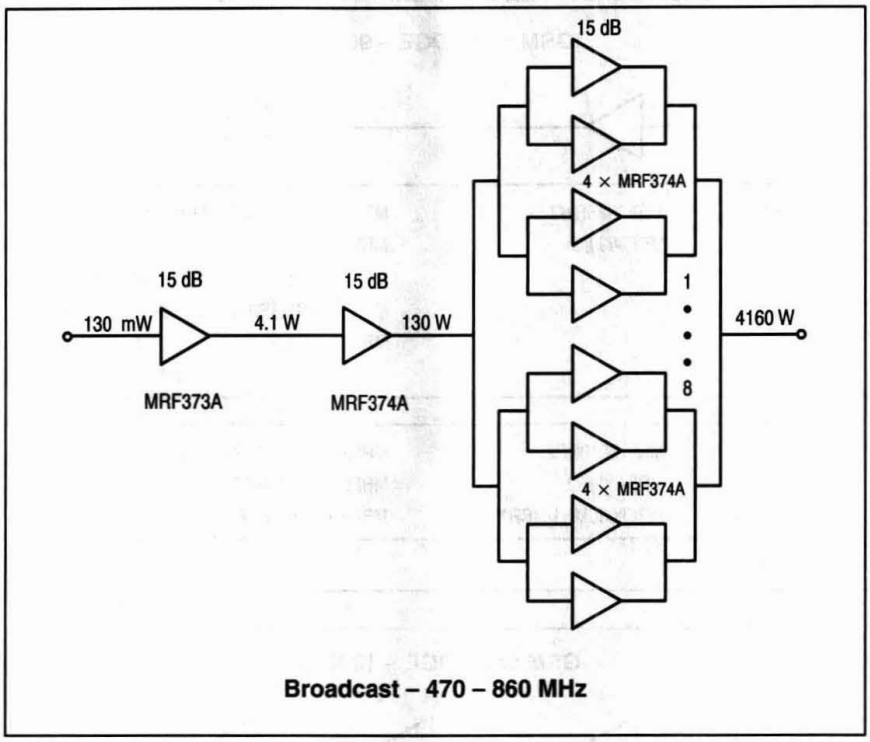


Broadcast – 470 MHz – 860 MHz



Broadcast – 470 – 860 MHz

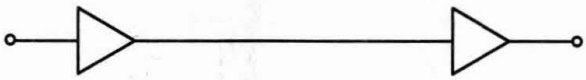
RF High Power Amplifier LDMOS Line–ups (continued)



Broadcast – 470 – 860 MHz

RF High Power Amplifier LDMOS Line–ups (continued)

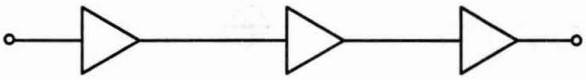
GSM and EDGE – 900 MHz



Ceramic	MRF282SR1/ZR1	MRF9045/S	MRF9100/S
	MRF9030/S	MRF9060/S	MRF9120/S
		MRF6522–70	MRF9130L/LS
		MRF9080/S/LSR3	MRF9135L/LS
		MRF9085/S/LS	MRF9180/S
			MRF9210

Plastic	MHVIC910HR2	MRF9030MR1/MBR1
	MRF9002R2	MRF9045MR1/MBR1
	MRF9030MR1/MBR1	MRF9060MR1/MBR1

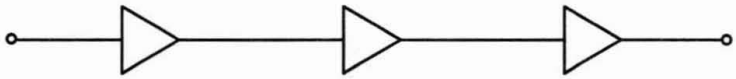
GSM and EDGE – 1800 MHz



Ceramic	MRF281SR1/ZR1	MRF18030A/S	MRF18060A/S
	MRF282SR1/ZR1	MRF284/SR1	MRF18085A/S
			MRF18090A/S

Hybrid	MHW1810–1
	MHW1810–2

GSM and EDGE – 1900 MHz



Ceramic	MRF281SR1/ZR1	MRF18030B/S	MRF18060B/S
	MRF282SR1/ZR1	MRF284/SR1	MRF18085B/S
			MRF18090B/S

Hybrid	MHW1910–1

RF High Power Amplifier LDMOS Line–ups (continued)

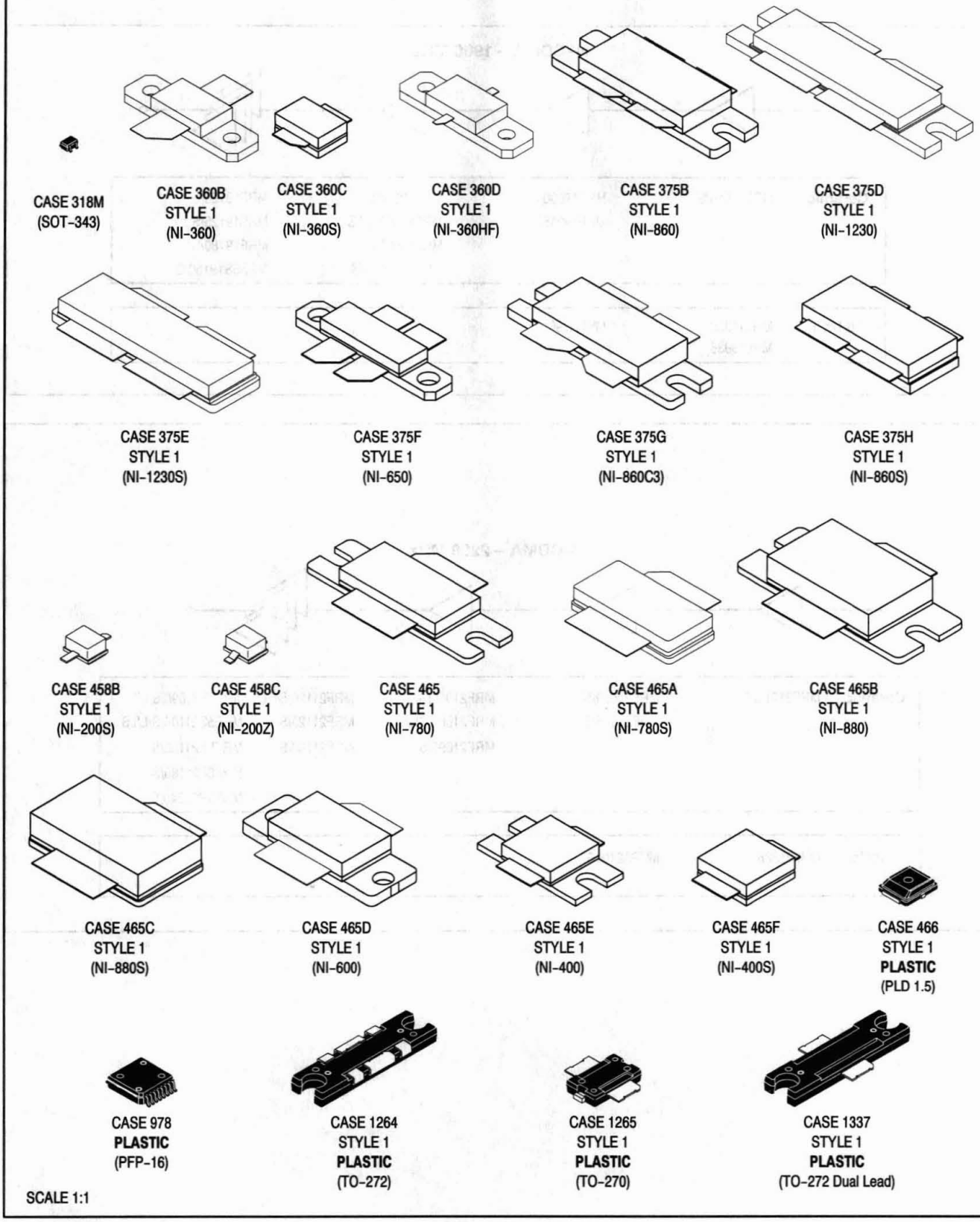
N–CDMA – 1900 MHz

Ceramic	MRF21010/S	MRF19030/S MRF19045/S	MRF19060/S MRF19085/S/LS MRF19090/S MRF5S19090/S	MRF19120/S MRF19125/S MRF19180/S MRF5S19150/S
Hybrid	MHL19338 MHL19936	MHPA19010		

W–CDMA – 2200 MHz

Ceramic	MRF21010/S	MRF21030/S MRF21045/S	MRF21060/S MRF21085/S/LS MRF21090/S	MRF21120/S MRF21125/S MRF21180/S	MRF5S21090/S/L/LS MRF5S21100/S/L/LS MRF5S21150/S MRF5P21180/S MRF5P21240/S
Hybrid	MHL21336	MHPA21010			

RF Transistor Packages



Section Two

Motorola RF Transistors – Data Sheets

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MRF281ZR1	5.2–4
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MRF284	5.2–15
MRF284SR1	5.2–15
MRF372	5.2–25
MRF373A	5.2–36
MRF373AS	5.2–36
MRF374A	5.2–41
MRF1511T1	5.2–51
MRF1513T1	5.2–61
MRF1517T1	5.2–73
MRF1518T1	5.2–85
MRF1535T1	5.2–97
MRF1550T1	5.2–107
MRF6522–70	5.2–116
MRF6522–70R3	5.2–116
MRF9002R2	5.2–123
MRF9030	5.2–130
MRF9030S	5.2–130
MRF9030SR1	5.2–130
MRF9030MR1	5.2–137
MRF9045	5.2–143
MRF9045S	5.2–143
MRF9045SR1	5.2–143
MRF9045MR1	5.2–150
MRF9045MBR1	5.2–150
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MRF9060S	5.2–158
MRF9060SR1	5.2–158
MRF9060MBR1	5.2–166
MRF9080	5.2–173
MRF9080R3	5.2–173
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MRF9080SR3	5.2–173
MRF9080LSR3	5.2–173
MRF9085	5.2–181
MRF9085R3	5.2–181
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MRF9085SR3	5.2–181
MRF9085LS	5.2–181
MRF9085LSR3	5.2–181
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MRF18060AS	5.2–213
MRF18060ASR3	5.2–213
MRF18060B	5.2–219
MRF18060BR3	5.2–219
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MRF19085S	5.2–255
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MRF19085LS	5.2–255
MRF19085LSR3	5.2–255
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MRF21085	5.2–309
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MRF21180S	5.2–336

MOTOROLA
intelligence everywhere

digital dna

MBC13900

Product Preview

The RF Building Block Series

NPN Silicon Low Noise Transistor

The MBC13900 is a high performance transistor fabricated using Motorola's 15 GHz f_τ bipolar IC process. It is housed in the 4–lead SC–70 (SOT–343) surface mount plastic package resulting in a parasitic effect reduction and RF performance enhancements. The high performance at low power makes the MBC13900 suitable for front–end applications in portable wireless systems such as pagers, cellular and cordless phones.

- Low Noise Figure, NF_{min} = 1.0 dB (Typ) @1.0 GHz, 3.0 V and 3.0 mA
- Maximum Stable Gain, 22 dB @ 1.0 GHz, 3.0 V and 3.0 mA
- Output Third Order Intercept, OIP_3 = 23 dBm @ 1.0 GHz, 3.0 V and 22 mA
- Ultra small SOT–343 Surface Mount Package
- Available Only in Tape and Reel Packaging

RF NPN SILICON TRANSISTOR

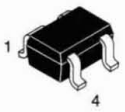
f_τ = 15 GHz

NF_{min} = 1.2 dB

I_{CMAX} = 20 mA

V_{CEO} = 5.0 V

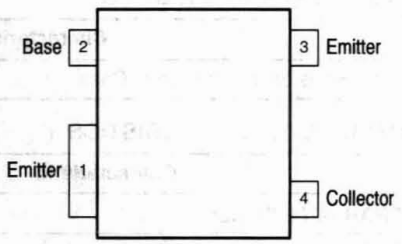
SEMICONDUCTOR TECHNICAL DATA



(Scale 4:1)

PLASTIC PACKAGE
CASE 318M
(SOT–343, Tape & Reel Only)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package
MBC13900	SOT–343

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

MRF281SR1
MRF281ZR1

Designed for digital and analog cellular PCN and PCS base station applications with frequencies from 1000 to 2500 MHz. Characterized for operation Class A and Class AB at 26 volts in commercial and industrial applications.

- Specified Two–Tone Performance @ 1930 and 2000 MHz, 26 Volts
  Output Power — 4 Watts PEP
  Power Gain — 11 dB
  Efficiency — 30%
  Intermodulation Distortion — –29 dBc
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 4 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Available in Tape and Reel. R1 Suffix = 500 Units per 12 mm, 7 inch Reel.

2000 MHz, 4 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

CASE 458B–03, STYLE 1
(NI–200S)
(MRF281SR1)

CASE 458C–03, STYLE 1
(NI–200Z)
(MRF281ZR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.115	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.74	°C/W

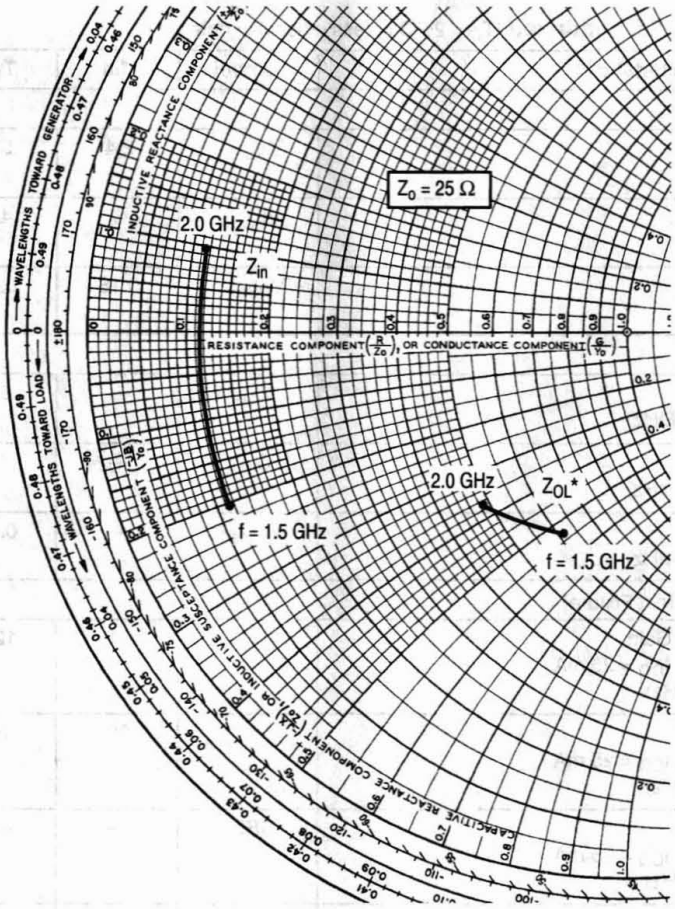
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	74	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 20 μAdc)	$V_{GS(th)}$	2.4	3.2	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 25 mAdc)	$V_{GS(q)}$	3	4.1	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.1 A)	$V_{DS(on)}$	0.18	0.24	0.30	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	5.5	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	3.3	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.17	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 4 W PEP, I_{DQ} = 25 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	G_{ps}	11	12.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 4 W PEP, I_{DQ} = 25 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	η	30	33	—	%
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 4 W PEP, I_{DQ} = 25 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IRL	—	–16	–10	dB
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 4 W PEP, I_{DQ} = 25 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IMD	—	–31	–29	dBc
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 4 W PEP, I_{DQ} = 25 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	11	12.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 4 W, I_{DQ} = 25 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	30	—	—	%
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 4 W PEP, I_{DQ} = 25 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IRL	—	–16	–10	dB
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 4 W PEP, I_{DQ} = 25 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IMD	—	–31	—	dBc
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 4 W CW, I_{DQ} = 25 mA, f1 = 2000.0 MHz)	G_{ps}	10.5	12	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 4 W CW, I_{DQ} = 25 mA, f1 = 2000.0 MHz)	η	40	44	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 4 W CW, I_{DQ} = 25 mA, f1 = 2000.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power			



V_{DD} = 26 V, I_{DQ} = 25 mA, P_{out} = 4 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1500	3.15 – j5.3	15.5 – j13.6
1600	3.1 – j3.8	14.7 – j12.5
1700	3.1 – j2.3	14.0 – j11.7
1800	3.1 – j0.7	13.4 – j11.0
1900	3.1 + j0.9	12.8 – j10.1
2000	3.1 + j2.4	12.2 – j9.2

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at given output power, voltage, IMD, bias current and frequency.

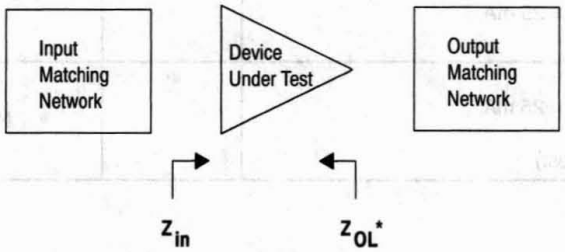


Figure 1. Series Equivalent Input and Output Impedance

Table 1. Common Source S–Parameters at V_{DS} = 26 Vdc, I_D = 250 mAdc

f GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	dB	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
0.1	.982	-28	18.9	160	.008	73	.851	-13
0.2	.947	-52	17.0	143	.015	58	.811	-25
0.3	.912	-73	15.0	129	.019	45	.770	-33
0.4	.886	-90	12.9	117	.022	36	.741	-42
0.5	.859	-103	11.1	108	.022	28	.719	-47
0.6	.854	-114	9.69	100	.023	23	.718	-51
0.7	.841	-123	8.54	93	.022	18	.709	-56
0.8	.837	-131	7.57	87	.021	15	.714	-59
0.9	.838	-138	6.69	81	.019	12	.719	-62
1.0	.841	-143	6.01	76	.018	11	.728	-64
1.1	.840	-149	5.41	72	.015	12	.742	-66
1.2	.849	-153	4.91	68	.013	13	.745	-68
1.3	.848	-158	4.51	64	.012	18	.758	-69
1.4	.856	-162	4.12	60	.010	26	.769	-70
1.5	.858	-167	3.78	57	.009	36	.786	-70
1.6	.871	-170	3.50	54	.008	54	.797	-72
1.7	.868	-173	3.22	51	.009	69	.808	-71
1.8	.870	-176	3.00	49	.009	82	.823	-72
1.9	.872	-180	2.80	46	.011	95	.828	-72
2.0	.877	178	2.63	44	.013	104	.845	-72
2.1	.876	174	2.47	41	.015	109	.843	-72
2.2	.880	171	2.36	39	.018	111	.859	-71
2.3	.882	168	2.21	36	.021	114	.858	-72
2.4	.886	165	2.12	34	.024	114	.872	-70
2.5	.896	162	1.97	32	.027	115	.863	-70
2.6	.897	158	1.89	29	.029	117	.873	-69

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

MRF282SR1
MRF282ZR1

Designed for Class A and Class AB PCN and PCS base station applications with frequencies up to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications.

- Specified Two–Tone Performance @ 2000 MHz, 26 Volts
  Output Power — 10 Watts PEP
  Power Gain — 10.5 dB
  Efficiency — 28%
  Intermodulation Distortion — –31 dBc
- Specified Single–Tone Performance @ 2000 MHz, 26 Volts
  Output Power — 10 Watts CW
  Power Gain — 9.5 dB
  Efficiency — 35%
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 10 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R1 Suffix = 500 Units per 12 mm, 7 inch Reel.

2000 MHz, 10 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

CASE 458B–03, STYLE 1
(NI–200S)
(MRF282SR1)

CASE 458C–03, STYLE 1
(NI–200Z)
(MRF282ZR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.34	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	°C/W

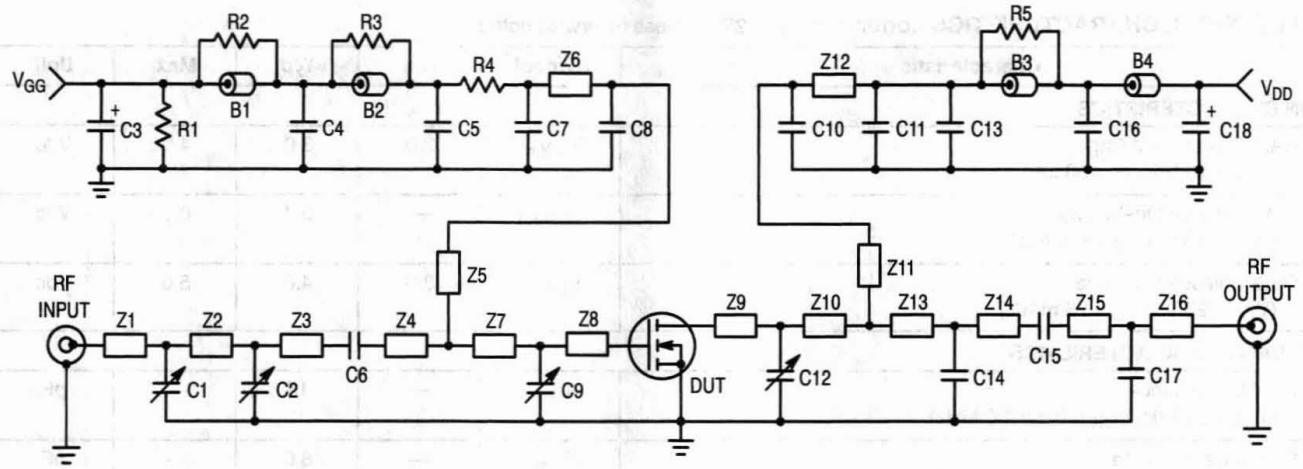
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 50 μAdc)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc)	$V_{DS(on)}$	—	0.4	0.6	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 75 mAdc)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	15	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	8.0	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.45	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	G_{ps}	10.5	11.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	η	28	—	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IRL	—	–14	–9	dB
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	10.5	11.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	28	—	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IRL	—	–14	–9	dB
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f = 2000.0 MHz)	G_{ps}	9.5	11.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f = 2000.0 MHz)	η	35	40	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz, Load VSWR = 10:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power			



Z1	0.491″ x 0.080″ Microstrip	Z11	0.636″ x 0.055″ Microstrip
Z2	0.253″ x 0.080″ Microstrip	Z12	0.303″ x 0.055″ Microstrip
Z3	0.632″ x 0.080″ Microstrip	Z13	0.463″ x 0.080″ Microstrip
Z4	0.567″ x 0.080″ Microstrip	Z14	0.105″ x 0.080″ Microstrip
Z5	1.139″ x 0.055″ Microstrip	Z15	0.452″ ± 0.085″ x 0.080″ Microstrip
Z6	0.236″ x 0.055″ Microstrip	Z16	0.910″ ± 0.085″ x 0.080″ Microstrip
Z7	0.180″ x 0.325″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z8	0.301″ x 0.325″ Microstrip		
Z9	0.439″ x 0.325″ Microstrip		
Z10	0.055″ x 0.325″ Microstrip		

Figure 1. 1.93 – 2.0 GHz Broadband Test Circuit Schematic

Table 1. 1.93 – 2.0 GHz Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B4	Surface Mount Ferrite Beads, 0.120″ x 0.333″ x 0.100″, Fair Rite #2743019446
B2, B3	Surface Mount Ferrite Beads, 0.120″ x 0.170″ x 0.100″, Fair Rite #2743029446
C1, C2, C9	0.8–8.0 pF Variable Capacitors, Johanson Gigatrim #27291SL
C3	10 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet #T495X106K035AS4394
C4, C5, C13, C16	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C6	200 pF Chip Capacitor, B Case, ATC #100B201JCA500X
C7	18 pF Chip Capacitor, B Case, ATC #100B180KP500X
C8	39 pF Chip Capacitor, B Case, ATC #100B390JCA500X
C10	27 pF Chip Capacitor, B Case, ATC #100B270JCA500X
C11	1.2 pF Chip Capacitor, B Case, ATC #100B1R2CCA500X
C12	0.6–4.5 pF Variable Capacitor, Johanson Gigatrim #27271SL
C14	0.5 pF Chip Capacitor, B Case, ATC #100B0R5BCA500X
C15	15 pF Chip Capacitor, B Case, ATC #100B150JCA500X
C17	0.1 pF Chip Capacitor, B Case, ATC #100B0R1BCA500X
C18	22 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet #T491X226K035AS4394
R1	560 kΩ, 1/4 W Chip Resistor, 0.08″ x 0.13″
R2, R5	12 Ω, 1/4 W Chip Resistors, 0.08″ x 0.13″, Garrett Instruments #RM73B2B120JT
R3, R4	91 Ω, 1/4 W Chip Resistors, 0.08″ x 0.13″, Garrett Instruments #RM73B2B910JT
WS1, WS2	Beryllium Copper Wear Blocks 0.010″ x 0.235″ x 0.135″ NOM
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type “N” Jack Connectors, Omni–Spectra # 3052–1648–10
	4–40 Ph Head Screws, 0.125″ Long
	4–40 Ph Head Screws, 0.188″ Long
	4–40 Ph Head Screws, 0.312″ Long
	4–40 Ph Rec. Hd. Screws, 0.438″ Long
RF Circuit Board	3″ x 5″ Copper Clad PCB, Glass Teflon®

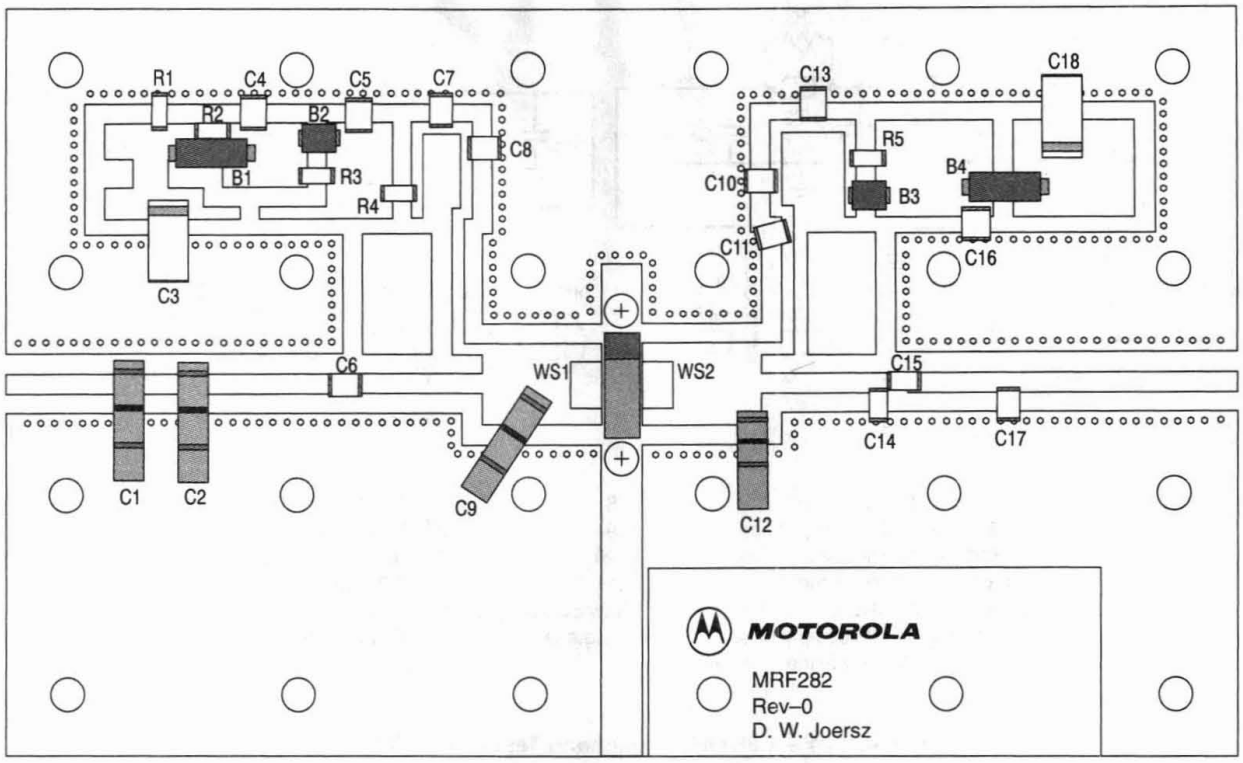
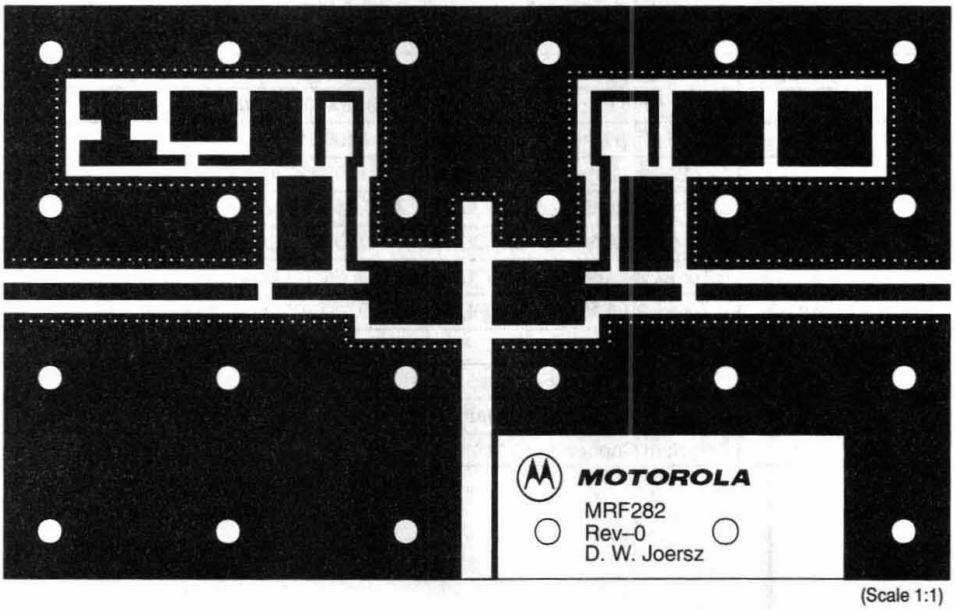
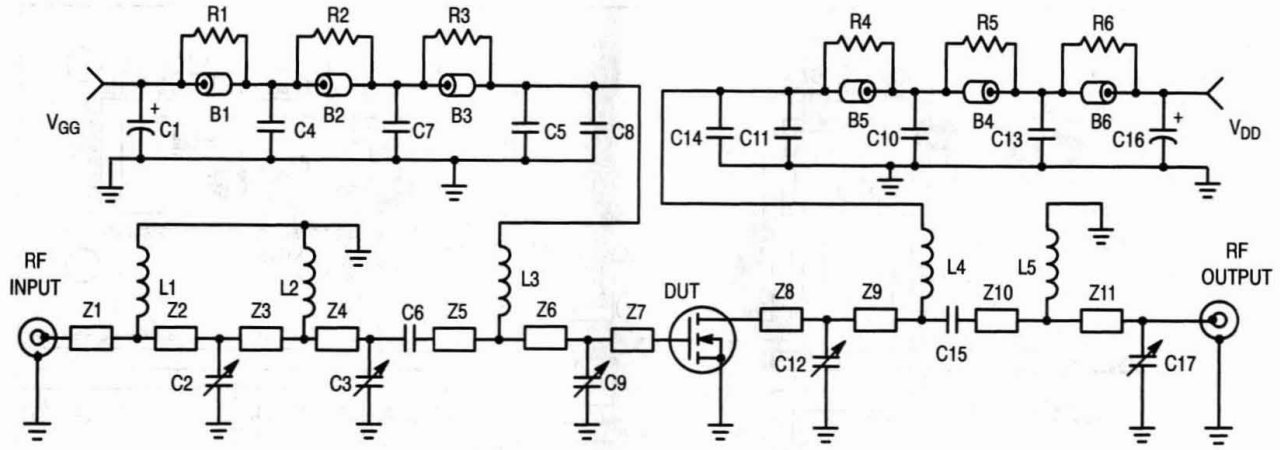


Figure 2. 1.93–2.0 GHz Broadband Test Circuit Component Layout



(Scale 1:1)

Figure 3. MRF282 Test Circuit Photomaster
(Reduced 18% in printed data book, DL110/D)

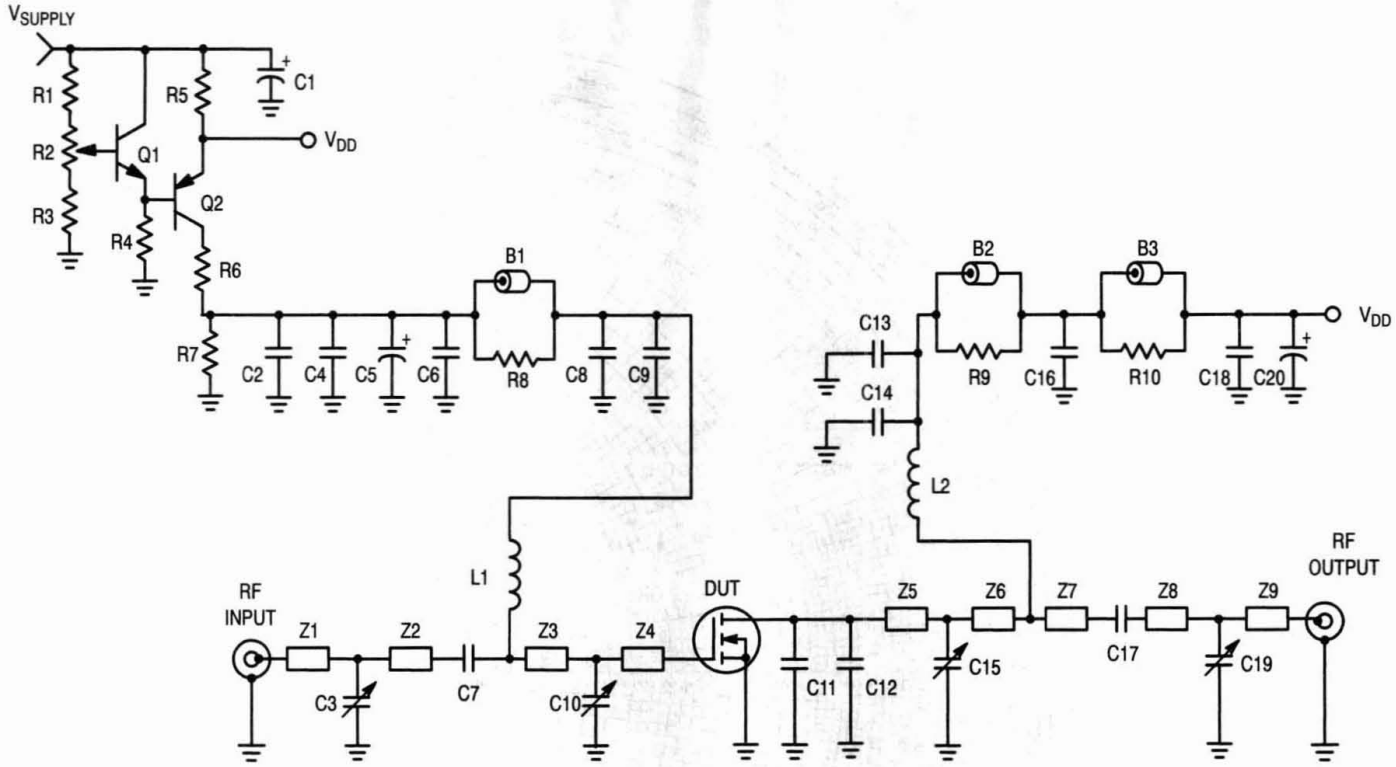


Z1	0.122″ x 0.08″ Microstrip	Z8	0.414″ x 0.330″ Microstrip
Z2	0.650″ x 0.08″ Microstrip	Z9	0.392″ x 0.08″ Microstrip
Z3	0.160″ x 0.08″ Microstrip	Z10	0.070″ x 0.08″ Microstrip
Z4	0.030″ x 0.08″ Microstrip	Z11	1.110″ x 0.08″ Microstrip
Z5	0.045″ x 0.08″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z6	0.291″ x 0.08″ Microstrip		
Z7	0.483″ x 0.330″ Microstrip		

Figure 4. 1.81 – 1.88 GHz Broadband Test Circuit Schematic

Table 2. 1.81 – 1.88 GHz Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B2, B3, B4, B5, B6	Surface Mount Ferrite Beads, 0.120″ x 0.170″ x 0.100″, Fair Rite #2743029446
C1, C16	470 μF, 63 V Electrolytic Capacitors, Mallory #SME63UB471M12X25L
C2, C9, C12, C17	0.6–4.5 pF Variable Capacitors, Johanson Gigatrim #27271SL
C3	0.8–8.0 pF Variable Capacitor, Johanson Gigatrim #27291SL
C4, C13	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C5, C14	100 pF Chip Capacitors, B Case, ATC #100B101JCA500X
C6, C8, C11, C15	12 pF Chip Capacitors, B Case, ATC #100B120JCA500X
C7, C10	1000 pF Chip Capacitors, B Case, ATC #100B102JCA50X
L1	3 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.053″ Long, 6.0 nH
L2	5 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.091″ Long, 15 nH
L3, L4	9 Turns, 26 AWG, 0.080″ OD, 0.046″ ID, 0.170″ Long, 30.8 nH
L5	4 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.078″ Long, 10 nH
R1, R2, R3	12 Ω, 1/8 W Fixed Film Chip Resistors, Garrett Instruments #RM73B2B120JT
R4, R5, R6	0.08″ x 0.13″ Resistors, Garrett Instruments #RM73B2B120JT
W1, W2	Beryllium Copper 0.010″ x 0.110″ x 0.210″

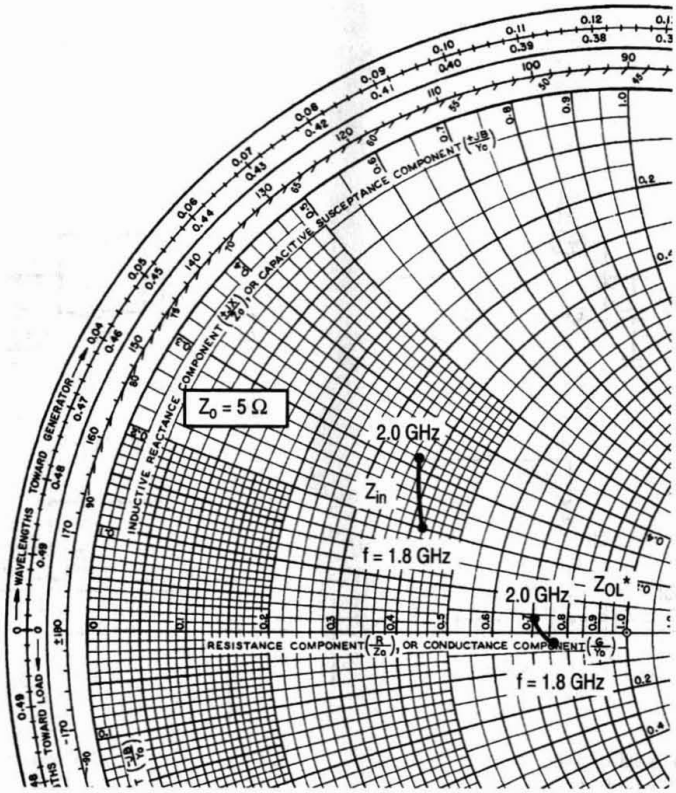


Z1	0.624″ x 0.08″ Microstrip	Z7	0.408″ x 0.08″ Microstrip
Z2	0.725″ x 0.08″ Microstrip	Z8	0.990″ x 0.08″ Microstrip
Z3	0.455″ x 0.08″ Microstrip	Z9	0.295″ x 0.08″ Microstrip
Z4	0.530″ x 0.330″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z5	0.280″ x 0.330″ Microstrip		
Z6	0.212″ x 0.330″ Microstrip		

Figure 5. Class A Broadband Test Circuit Schematic

Table 3. Class A Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B2, B3	Ferrite Beads, Ferroxcube #56–590–65–3B
C1, C20	470 μF, 63 V Electrolytic Capacitors, Mallory #SME63V471M12X25L
C2	0.01 μF Chip Capacitor, B Case, ATC #100B103JCA50X
C3, C10, C15	0.6–4.5 pF Variable Capacitors, Johanson #27271SL
C4, C16	0.02 μF Chip Capacitors, B Case, ATC #100B203JCA50X
C5	100 μF, 50 V Electrolytic Capacitor, Mallory #SME50VB101M12X256
C6, C7, C9, C14, C17	12 pF Chip Capacitors, B Case, ATC #100B120JCA500X
C8, C13	51 pF Chip Capacitors, B Case, ATC #100B510JCA500X
C11, C12	0.3 pF Chip Capacitors, B Case, ATC #100B0R3CCA500X
C18	0.1 μF Chip Capacitor, Kemet #CDR33BX104AKWS
C19	0.4–2.5 pF Variable Capacitor, Johanson #27285
L1	8 Turns, 0.042″ ID, 24 AWG, Enamel
L2	9 Turns, 0.046″ ID, 26 AWG, Enamel
Q1	NPN, 15 W, Bipolar Transistor, MJD310
Q2	PNP, 15 W, Bipolar Transistor, MJD320
R1	200 Ω, 1/4 W Axial Resistor
R2	1.0 kΩ, 1/2 W Potentiometer, Bourns
R3	13 kΩ, 1/4 W Axial Resistor
R4, R6, R7	390 Ω, 1/8 W Chip Resistors, Garrett Instruments #RM73B2B391JT
R5	1.0 Ω, 10 W 1% Resistor, Dale #RE65G1R00
R8, R9, R10	12 Ω, 1/8 W Chip Resistors, Garrett Instruments #RM73B2B120JT
Input/Output	Type N Flange Mount RF55–22 Connectors, Omni–Spectra



V_{DD} = 26 V, I_{DQ} = 75 mA, P_{out} = 10 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1800	2.1 + j1.0	3.8 – j0.15
1860	2.05 + j1.15	3.77 – j0.13
1900	2.0 + j1.2	3.75 – j0.1
1960	1.9 + j1.4	3.65 + j0.1
2000	1.85 + j1.6	3.55 + j0.2

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at given output power, voltage, IMD, bias current and frequency.

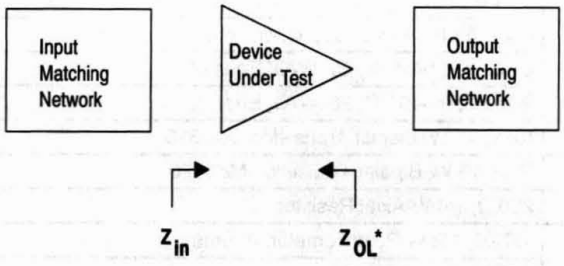


Figure 6. Series Equivalent Input and Output Impedence

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

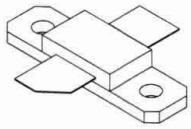
N–Channel Enhancement–Mode Lateral MOSFETs

MRF284
MRF284SR1

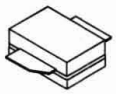
2000 MHz, 30 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1000 to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications. To be used in Class A and Class AB for PCN–PCS/cellular radio and wireless local loop.

- Specified Two–Tone Performance @ 2000 MHz, 26 Volts
  Output Power = 30 Watts (PEP)
  Power Gain = 9 dB
  Efficiency = 30%
  Intermodulation Distortion = –29 dBc
- Typical Single–Tone Performance at 2000 MHz, 26 Volts
  Output Power = 30 Watts (CW)
  Power Gain = 9.5 dB
  Efficiency = 45%
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 30 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.



CASE 360B–05, STYLE 1
(NI–360)
(MRF284)



CASE 360C–05, STYLE 1
(NI–360S)
(MRF284SR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	87.5 0.5	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

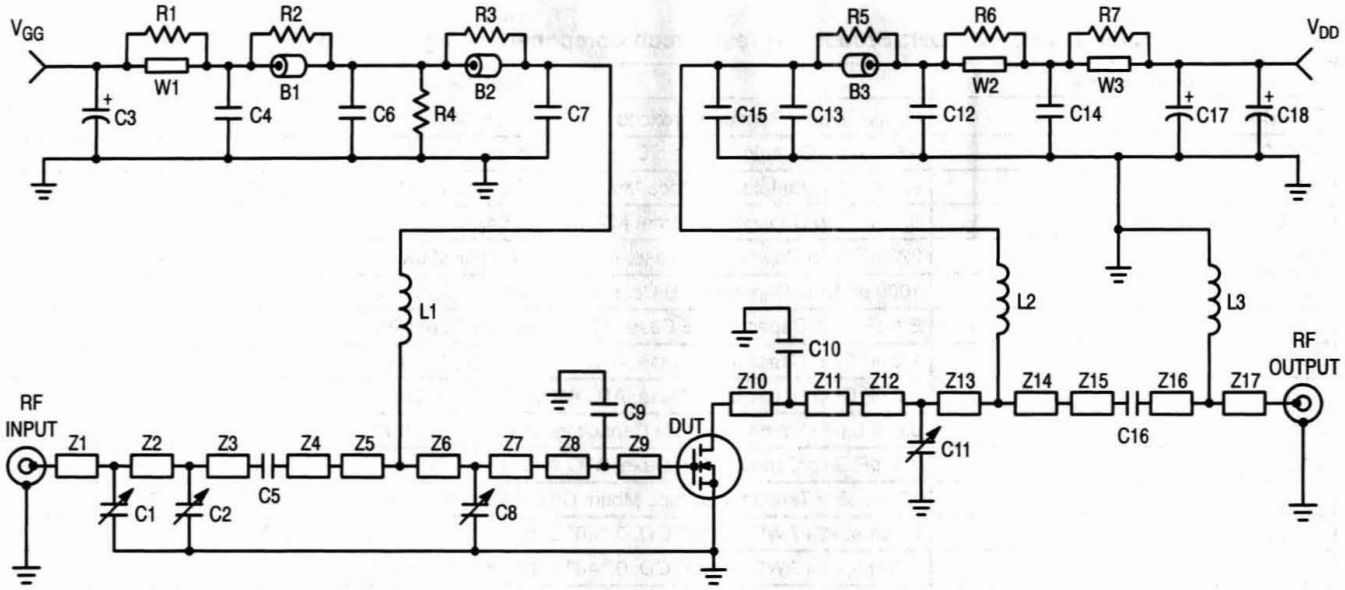
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	10	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 200 mAdc)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	—	0.3	0.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.0 Adc)	g_{fs}	—	1.5	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	43	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	23	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	1.4	—	pF
FUNCTIONAL TESTS (in Motorola Test Fixture)					
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	G_{ps}	9	10.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	η	30	35	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IMD	—	–32	–29	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IRL	—	–15	–9	dB
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	9	10.4	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	—	35	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IMD	—	–34	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IRL	—	–15	–9	dB
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz)	G_{ps}	8.5	9.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz)	η	35	45	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz, VSWR = 10:1, at All Phase Angles)	Ψ	No Degradation In Output Power			



Z1	0.530″ x 0.080″ Microstrip	Z11	0.155″ x 0.515″ Microstrip
Z2	0.255″ x 0.080″ Microstrip	Z12	0.120″ x 0.325″ Microstrip
Z3	0.600″ x 0.080″ Microstrip	Z13	0.150″ x 0.325″ Microstrip
Z4	0.525″ x 0.080″ Microstrip	Z14	0.010″ x 0.325″ Microstrip
Z5	0.015″ x 0.325″ Microstrip	Z15	0.505″ x 0.080″ Microstrip
Z6	0.085″ x 0.325″ Microstrip	Z16	0.865″ x 0.080″ Microstrip
Z7	0.165″ x 0.325″ Microstrip	Z17	0.525″ x 0.080″ Microstrip
Z8	0.110″ x 0.515″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z9	0.095″ x 0.515″ Microstrip		
Z10	0.050″ x 0.515″ Microstrip		

Figure 1. 1.93–2.0 GHz Broadband Test Circuit Schematic

Table 1. 1.93 – 2.0 GHz Broadband Test Circuit Component Designations and Values

Designators	Description
B1 – B3	Ferrite Beads, Round, Ferroxcube #56–590–65–3B
C1, C2, C8	0.8–8.0 pF Gigatrim Variable Capacitors, Johanson #27291SL
C3, C17	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T491X226K035AS4394
C4, C14	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C5	220 pF Chip Capacitor, B Case, ATC #100B221KP500X
C6, C12	1000 pF Chip Capacitors, B Case, ATC #100B102JCA50X
C7, C13	5.1 pF Chip Capacitors, B Case, ATC #100B5R1CCA500X
C9	1.2 pF Chip Capacitor, B Case, ATC #100B1R2CCA500X
C10	2.7 pF Chip Capacitor, B Case, ATC #100B2R7CCA500X
C11	0.6–4.5 pF Gigatrim Variable Capacitors, Johanson #27271SL
C15, C16	200 pF Chip Capacitors, B Case, ATC #100B201KP500X
C18	10 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet #T495X106K035AS4394
L1, L2	4 Turns, #24 AWG, 0.120″ OD, 0.140″ Long, (12.5 nH), Coilcraft #A04T–5
L3	2 Turns, #24 AWG, 0.120″ OD, 0.140″ Long, (5.0 nH), Coilcraft #A02T–5
R1, R2, R3, R5, R6, R7	12 Ω, 1/4 W Chip Resistors, 0.08″ x 0.13″, Garrett Instruments #RM73B2B120JT
R4	560 kΩ, 1/4 W Chip Resistor, 0.08″ x 0.13″
W1, W2, W3	Solid Copper Buss Wire, 16 AWG
WS1, WS2	Berrylium Copper Wear Blocks 0.005″ x 0.250″ x 0.250″
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type “N” Jack Connectors, Omni–Spectra #3052–1648–10
	4–40 Ph Head Screws, 0.125″ Long
	4–40 Ph Head Screws, 0.188″ Long
	4–40 Ph Head Screws, 0.312″ Long
	4–40 Ph Rec. Hd. Screws, 0.438″ Long
RF Circuit Board	3″ x 5″ Copper Clad PCB, Glass Teflon®

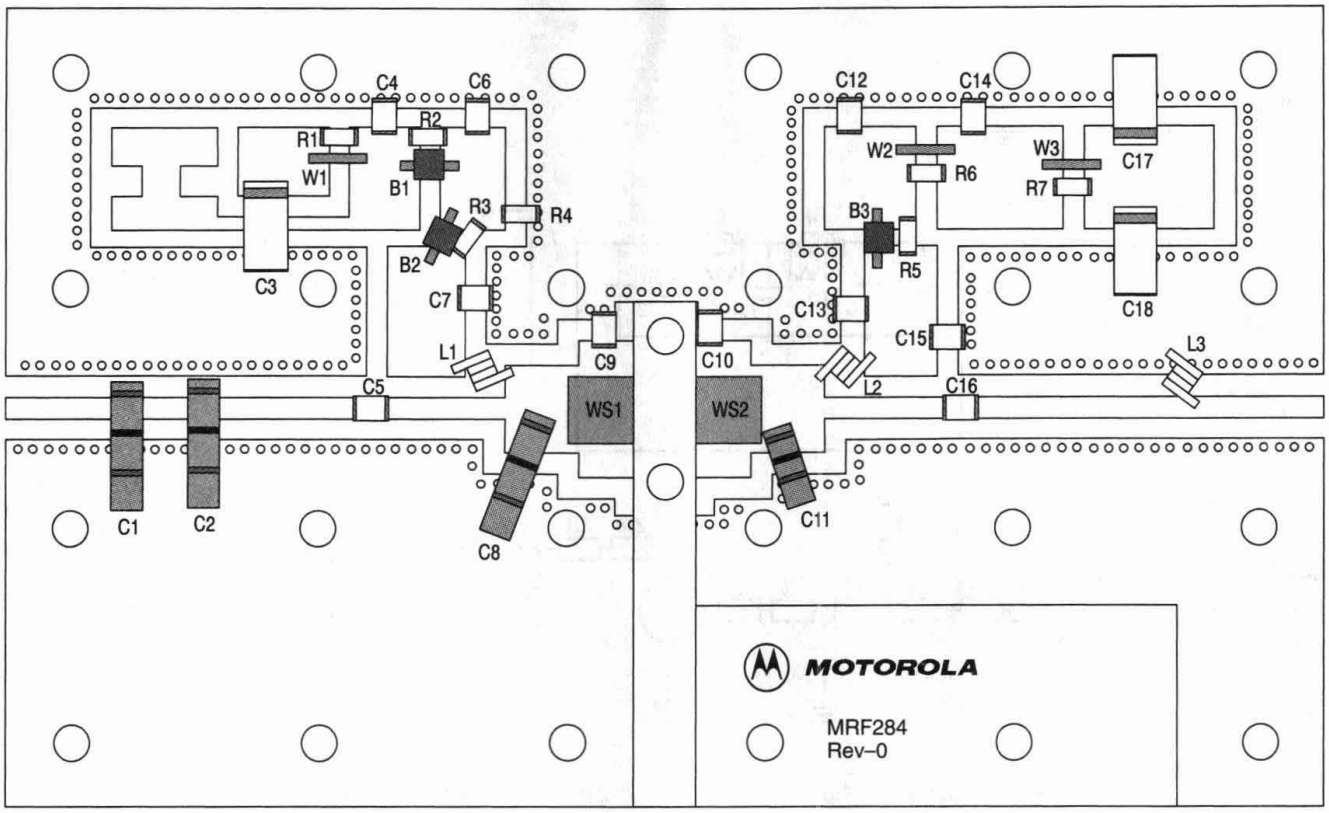
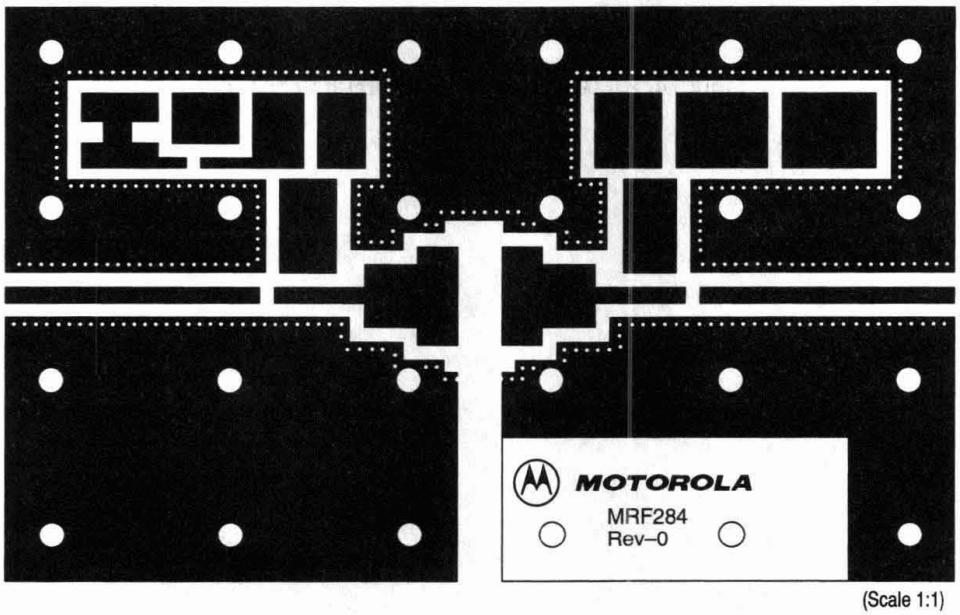
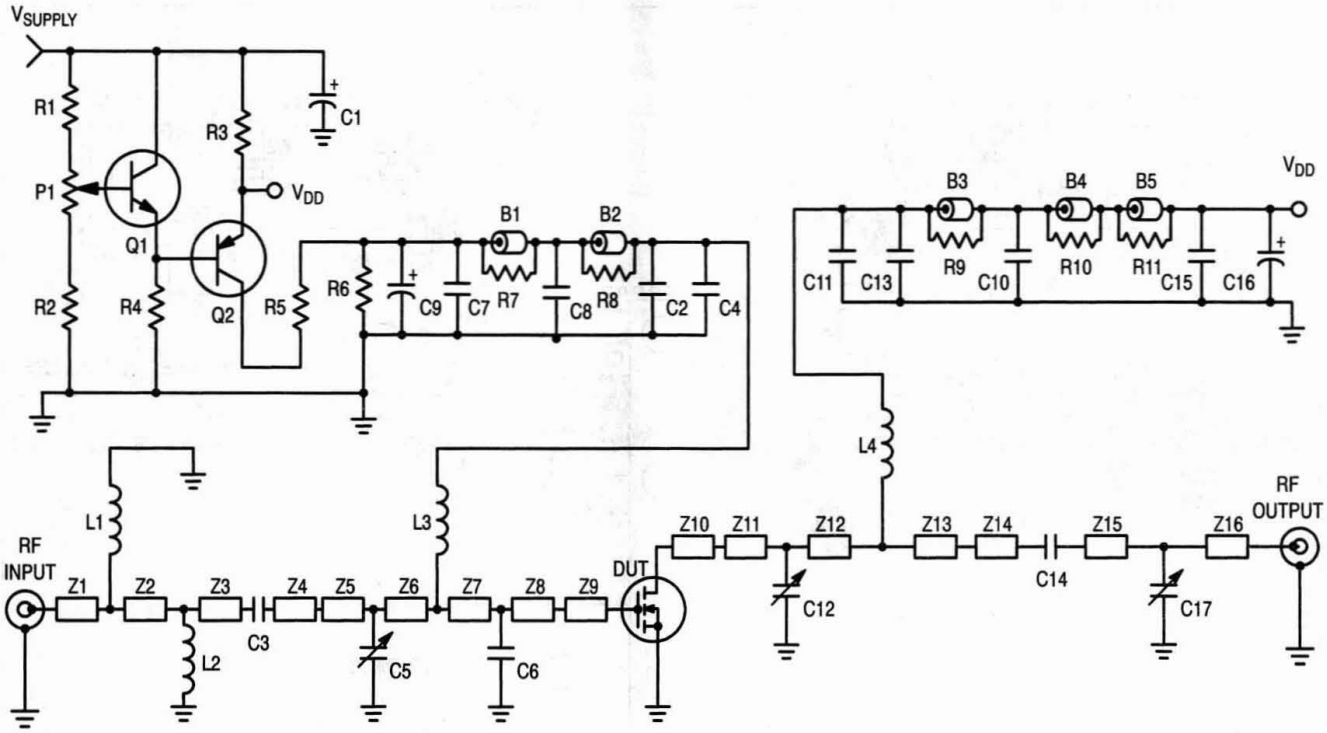


Figure 2. 1.93–2.0 GHz Broadband Test Circuit Component Layout



(Scale 1:1)

Figure 3. MRF284 Test Circuit Photomaster
(Reduced 18% in printed data book, DL110/D)



Z1	0.363″ x 0.080″ Microstrip
Z2	0.080″ x 0.080″ Microstrip
Z3	0.916″ x 0.080″ Microstrip
Z4	0.517″ x 0.080″ Microstrip
Z5	0.050″ x 0.325″ Microstrip
Z6	0.050″ x 0.325″ Microstrip
Z7	0.071″ x 0.325″ Microstrip
Z8	0.125″ x 0.325″ Microstrip
Z9	0.210″ x 0.515″ Microstrip
Z10	0.210″ x 0.515″ Microstrip
Z11	0.235″ x 0.325″ Microstrip
Z12	0.02″ x 0.325″ Microstrip
Z13	0.02″ x 0.325″ Microstrip
Z14	0.510″ x 0.080″ Microstrip
Z15	0.990″ x 0.080″ Microstrip
Z16	0.390″ x 0.080″ Microstrip
Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55

Figure 4. 2.0 GHz Class A Test Circuit Schematic

Table 2. 2.0 GHz Class A Test Circuit Component Designations and Values

Designators	Description
B1 – B5	Ferrite Beads, Round, Ferroxcube # 56–590–65–3B
C1, C9, C16	100 μF, 50 V Electrolytic Capacitors, Mallory #SME50VB101M12X25L
C2, C13	51 pF Chip Capacitors, B Case, ATC #100B510JCA500x
C3, C14	10 pF Chip Capacitors, B Case, ATC #100B100JCA500X
C4, C11	12 pF Chip Capacitors, B Case, ATC #100B120JCA500X
C5	0.8 – 8.0 pF Variable Capacitor, Johansen Gigatrim #27291SL
C6	4.7 pF Chip Capacitor, B Case, ATC #100B4R7CCA500X
C7, C15	91 pF Chip Capacitors, B Case, ATC #100B910KP500X
C8	1000 pF Chip Capacitor, B Case, ATC #100B102JCA50X
C10	0.1 μF Chip Capacitor, Kemet #CDR33BX104AKWS
C12, C17	0.6 – 4.5 pF Variable Capacitors, Johansen Gigatrim #27271SL
L1	4 Turns, #27 AWG, 0.087″ OD, 0.050″ ID, 0.069″ Long, 10 nH
L2	5 Turns, #24 AWG, 0.083″ OD, 0.040″ ID, 0.128″ Long, 12.5 nH
L3, L4	9 Turns, #26 AWG, 0.080″ OD, 0.046″ ID, 0.170″ Long, 30.8 nH
P1	1000 Ω Potentiometer, 1/2 W, 10 Turns, Bourns
Q1	Transistor, NPN, Motorola P/N: MJD31, Case 369A–10
Q2	Transistor, PNP, Motorola P/N: MJD32, Case 369A–10
R1	360 Ω, Fixed Film Chip Resistor, 0.08″ x 0.13″, Garrett Instruments #RM73B2B361JT
R2	2 x 12 kΩ, Fixed Film Chip Resistor, 0.08″ x 0.13″, Garrett Instruments #RM73B2B122JT
R3	1 Ω, Wirewound, 5 W, 3% Resistor, Dale # RE60G1R00
R4	4 x 6.8 kΩ, Fixed Film Chip Resistor, 0.08″ x 0.13″, Garrett Instruments #RM73B2B682JT
R5	2 x 1500 Ω, Fixed Film Chip Resistor, 0.08″ x 0.13″, Garrett Instruments #RM73B2B152JT
R6	270 Ω, Fixed Film Chip Resistor, 0.08″ x 0.13″, Garrett Instruments #RM73B2B271JT
R7 – R11	12 Ω, Fixed Film Chip Resistors, 0.08″ x 0.13″, Garrett Instruments #RM73B2B120JT

TYPICAL CHARACTERISTICS

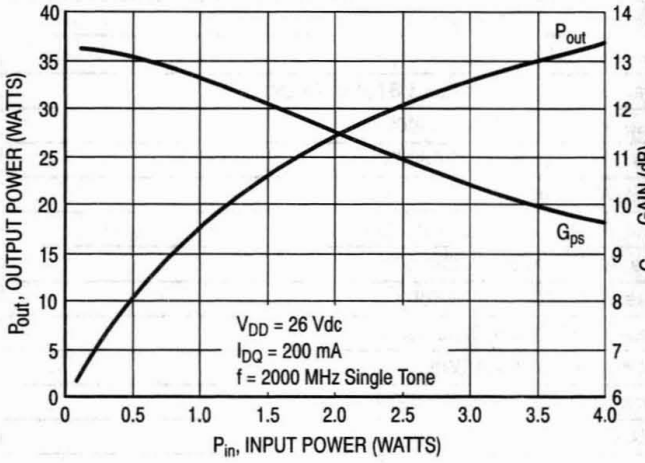


Figure 5. Output Power & Power Gain versus Input Power

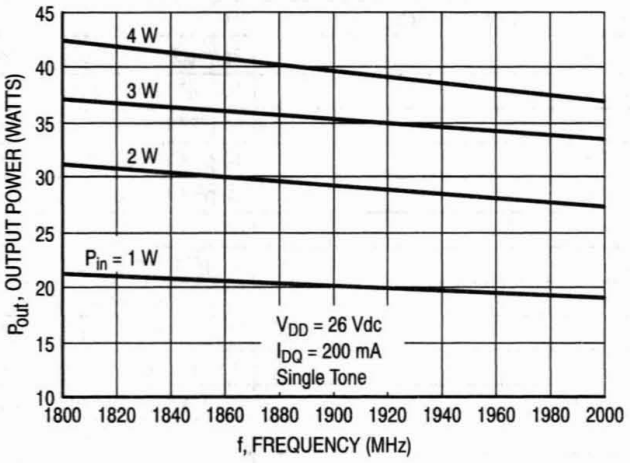


Figure 6. Output Power versus Frequency

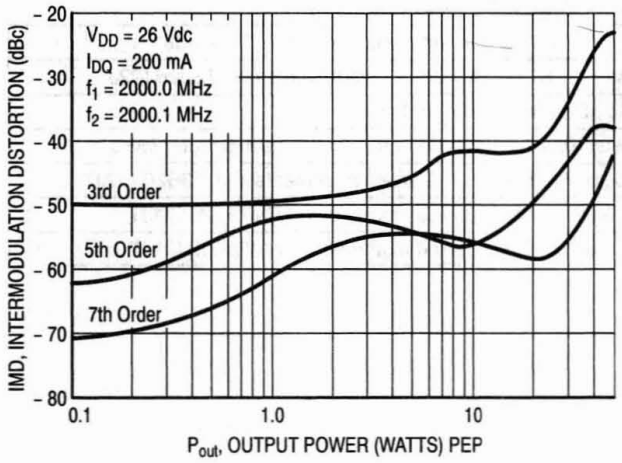


Figure 7. Intermodulation Distortion Products versus Output Power

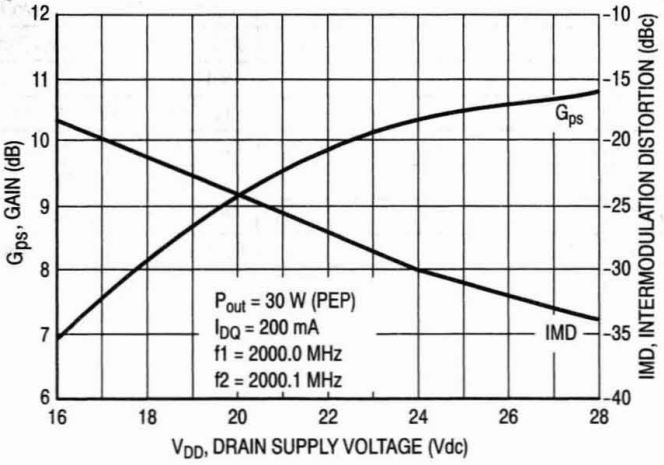


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage

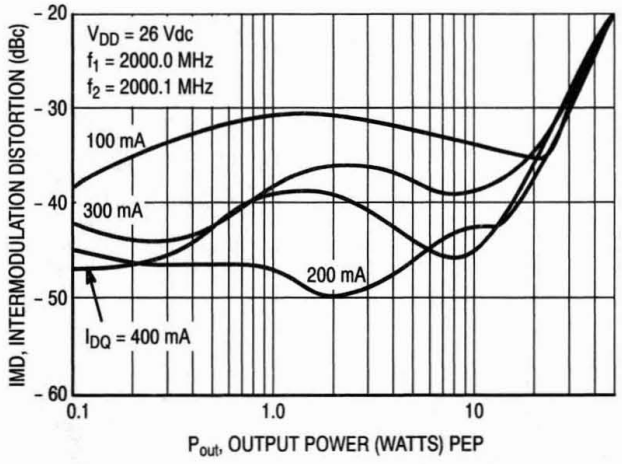


Figure 9. Intermodulation Distortion versus Output Power

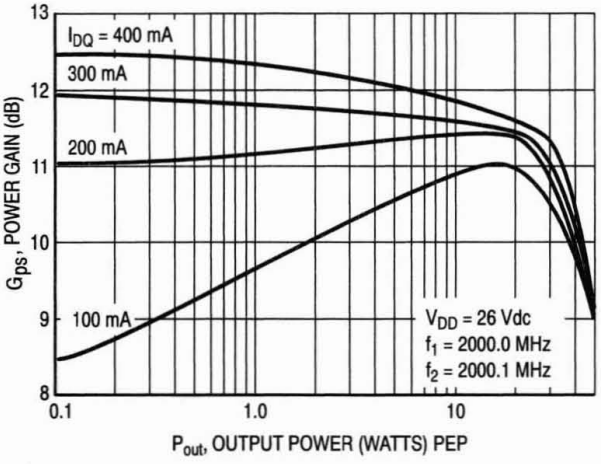


Figure 10. Power Gain versus Output Power

TYPICAL CHARACTERISTICS

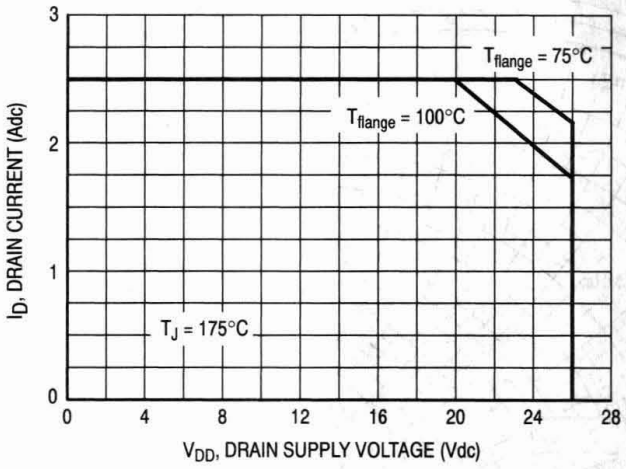


Figure 11. DC Safe Operating Area

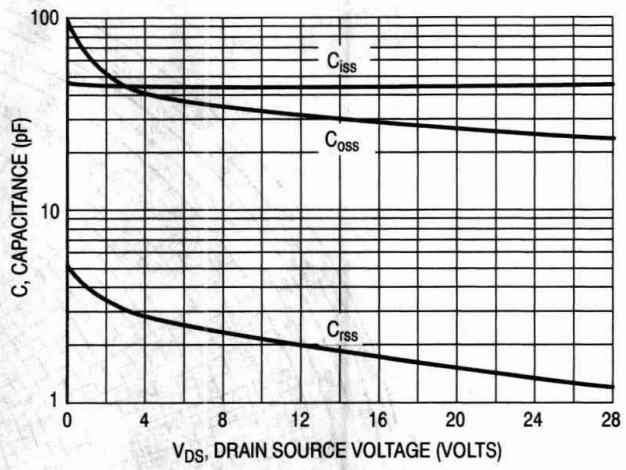


Figure 12. Capacitance versus Drain Source Voltage

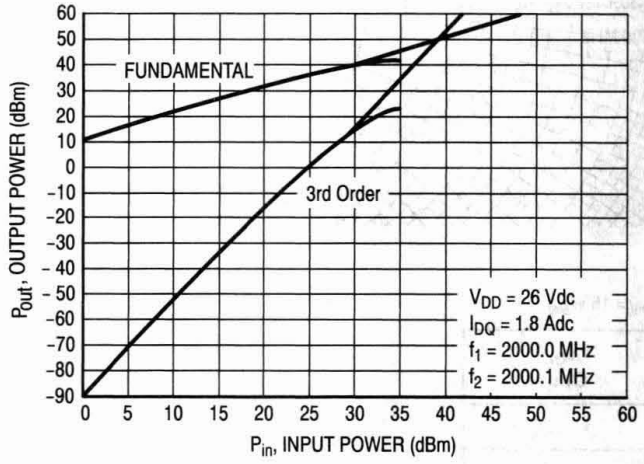


Figure 13. Class A Third Order Intercept Point

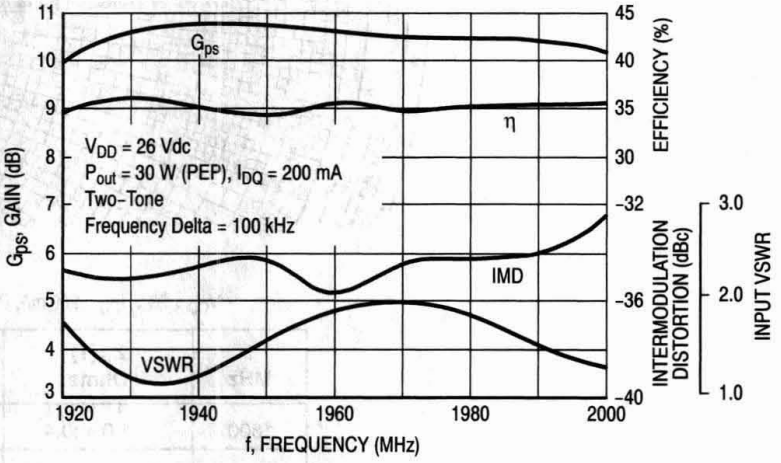
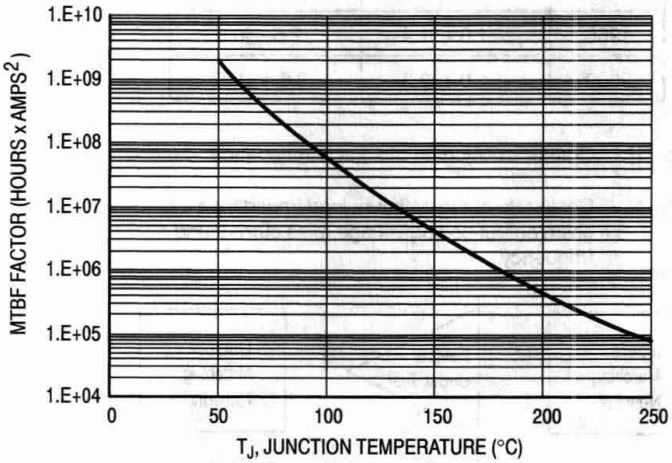
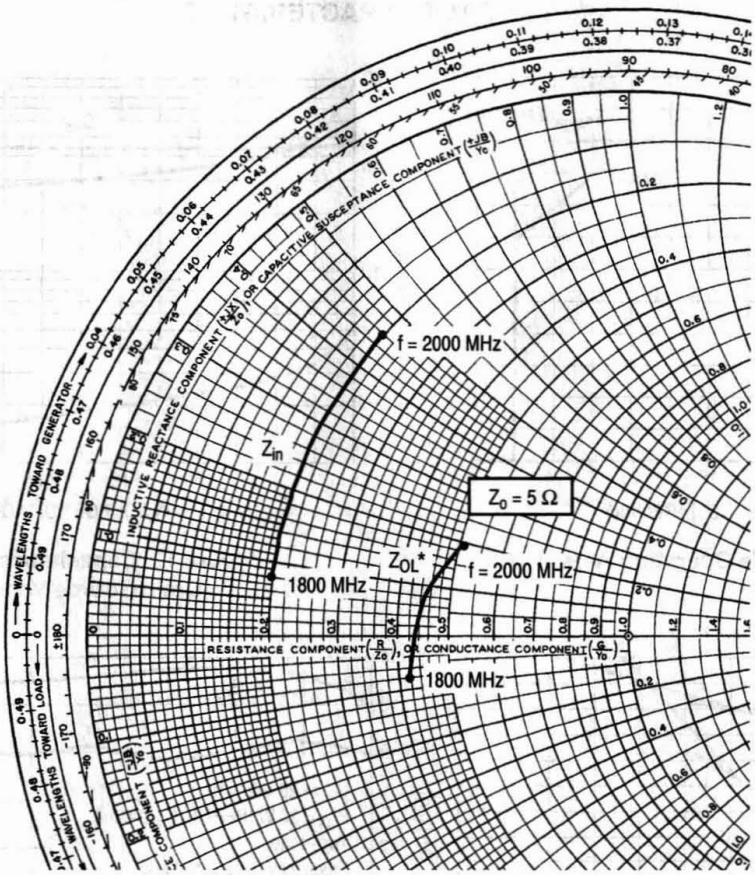


Figure 14. 1.92–2.0 GHz Broadband Circuit Performance



This graph displays calculated MTBF in hours x ampere^2 drain current. Life tests at elevated temperature have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 15. MTBF Factor versus Junction Temperature



V_{CC} = 26 V, I_{CQ} = 200 mA, P_{out} = 15 W_{avg}

f MHz	$Z_{in}(1)$ Ohms	Z_{OL}^* Ohms
1800	1.0 + j0.4	2.1 – j0.4
1860	1.0 + j0.8	2.2 + j0.2
1900	1.0 + j1.1	2.3 + j0.5
1960	1.0 + j1.4	2.5 + j0.9
2000	1.0 + j2.3	2.6 + j0.92

$Z_{in}(1)$ = Complex conjugate of source impedance.

Z_{OL}^* = Conjugate of the optimum load impedance at given output power, voltage, bias current and frequency.

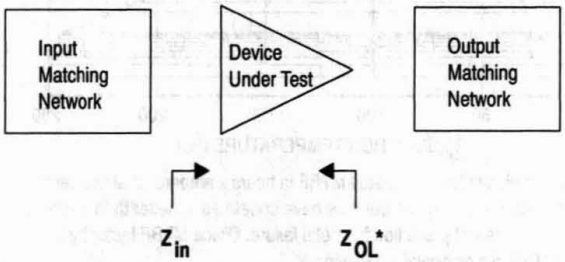


Figure 16. Series Equivalent Input and Output Impedence

The RF MOSFET Line

RF Power Field-Effect Transistor

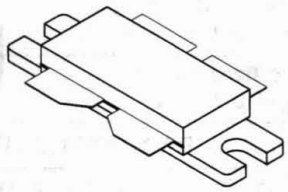
N–Channel Enhancement–Mode Lateral MOSFET

MRF372

470 – 860 MHz, 180 W, 32 V
LATERAL N–CHANNEL
RF POWER MOSFET

Designed for broadband commercial and industrial applications with frequencies from 470 to 860 MHz. The high gain and broadband performance of this device make it ideal for large–signal, common source amplifier applications in 32 volt transmitter equipment.

- Typical Narrowband Two–Tone Performance @ f1 = 857 MHz, f2 = 863 MHz, 32 Volts
  Output Power — 180 Watts PEP
  Power Gain — 17 dB
  Efficiency — 36%
  IMD — –35 dBc
- Typical Broadband Two–Tone Performance @ f1 = 857 MHz, f2 = 863 MHz, 32 Volts
  Output Power — 180 Watts PEP
  Power Gain — 14.5 dB
  Efficiency — 37%
  IMD — –31 dBc
- Internally Matched, Controlled Q, for Ease of Use
- Integrated ESD Protection
- 100% Tested for Load Mismatch Stress at All Phase Angles with 3:1 VSWR @ 32 Vdc, f1 = 857 MHz, f2 = 863 MHz, 180 Watts PEP
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 375G–04, STYLE 1
(NI–860C)

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	68	Vdc
Gate–Source Voltage	V_{GS}	+15, – 0.5	Vdc
Drain Current – Continuous	I_D	17	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.0	W W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	°C/W

(1) Each side of device measured separately.

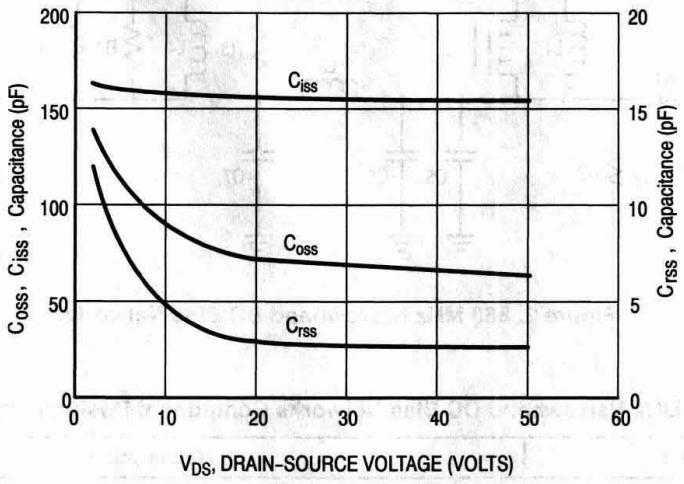
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D =10 μA)	$V_{(BR)DSS}$	68	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 32 V, I_D = 100 mA)	$V_{GS(Q)}$	2.5	3.5	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	—	0.28	0.45	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	—	2.6	—	S
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (Includes Input Matching Capacitance) (V_{DS} = 32 V, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	—	260	—	pF
Output Capacitance (V_{DS} = 32 V, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	—	69	—	pF
Reverse Transfer Capacitance (V_{DS} = 32 V, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	—	2.5	—	pF
FUNCTIONAL CHARACTERISTICS, TWO–TONE TESTING, NARROWBAND FIXTURE (2)					
Common Source Power Gain (V_{DD} = 32 V, P_{out} = 180 W PEP, I_{DQ} = 2 x 400 mA, f1 = 857 MHz, f2 = 863 MHz)	G_{ps}	16	17	—	dB
Drain Efficiency (V_{DD} = 32 V, P_{out} = 180 W PEP, I_{DQ} = 2 x 400 mA, f1 = 857 MHz, f2 = 863 MHz)	η	33	36	—	%
Intermodulation Distortion (V_{DD} = 32 Vdc, P_{out} = 180 W PEP, I_{DQ} = 2 x 400 mA, f1 = 857 MHz, f2 = 863 MHz)	IMD	—	–35	–31	dBc
Output Mismatch Stress (V_{DD} = 32 Vdc, P_{out} = 180 W PEP, I_{DQ} = 2 x 400 mA, f1 = 857 MHz, f2 = 863 MHz, V_{SWR} = 3:1 at all phase angles of test)	ψ	No Degradation in Output Power			
TYPICAL CHARACTERISTICS, TWO–TONE OPERATION, BROADBAND FIXTURE (2)					
Common Source Power Gain (V_{DD} = 32 Vdc, P_{out} = 180 W PEP, I_{DQ} = 2 x 500 mA, f1 = 857 MHz, f2 = 863 MHz)	G_{ps}	—	14.5	—	dB
Drain Efficiency (V_{DD} = 32 Vdc, P_{out} = 180 W PEP, I_{DQ} = 2 x 500 mA, f1 = 857 MHz, f2 = 863 MHz)	η	—	37	—	%
Intermodulation Distortion (V_{DD} = 32 Vdc, P_{out} = 180 W PEP, I_{DQ} = 2 x 500 mA, f1 = 857 MHz, f2 = 863 MHz)	IMD	—	–31	—	dBc

(1) Each side of device measured separately.
(2) Measured in push–pull configuration.

TYPICAL CHARACTERISTICS



Note: C_{iss} does not include input matching capacitance.

Figure 1. Capacitance versus Voltage

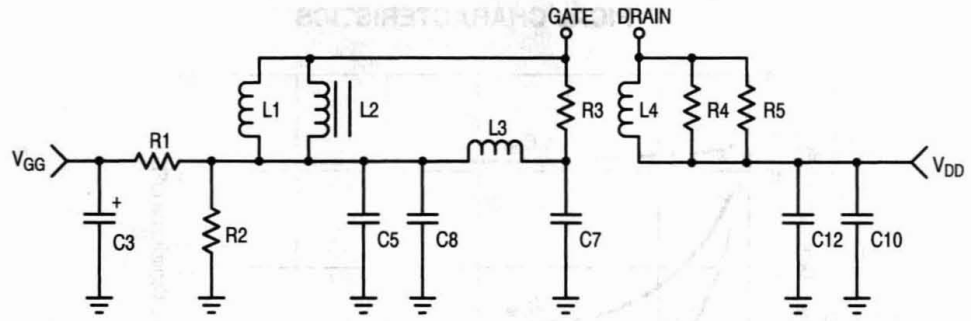
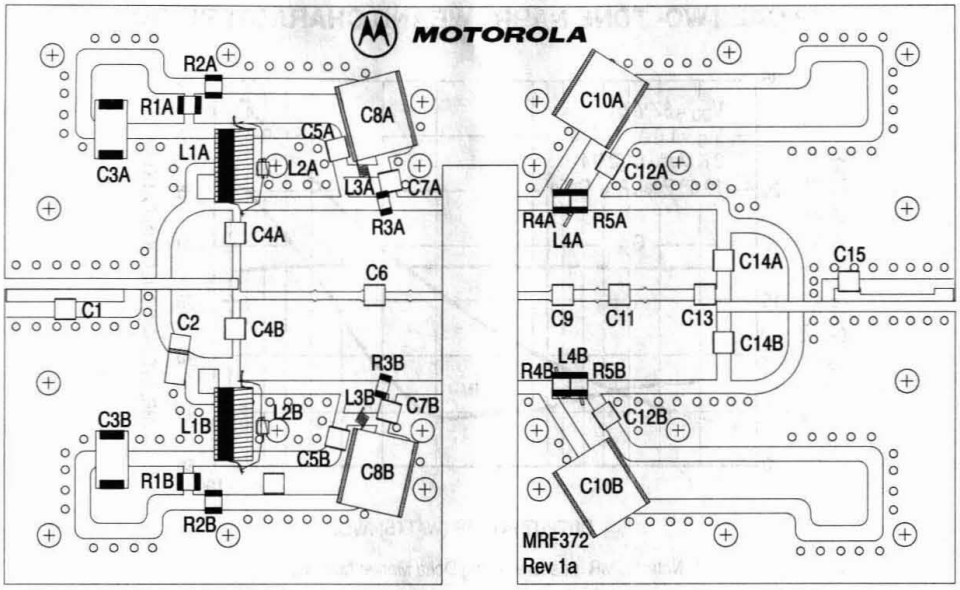


Figure 2. 860 MHz Narrowband DC Bias Networks

Table 1. 860 MHz Narrowband DC Bias Networks Component Designations and Values

Designation	Description
C1	2.2 pF Chip Capacitor, B Case, ATC
C2	0.5 — 5.0 pF Variable Capacitor, B Case, Johansen Gigatrim
C3A, B	22 μF, 22 V Tantalum Chip Capacitors, Kemet #T491D226K22AS
C4A, B, C14A, B	47.0 pF Chip Capacitors, B Case, ATC
C5A, B	100 pF Chip Capacitors, B Case, ATC
C6	10.0 pF Chip Capacitor, B Case, ATC
C7A, B	2.7 pF Chip Capacitors, A Case, ATC
C8A, B	1.0 μF, 100 V Chip Capacitors, Vitramon #VJ3640Y105KXBAT
C9	10.0 pF Chip Capacitor, B Case, ATC
C10A, B	2.2 μF, 100 V Chip Capacitors, Vitramon #VJ3640Y225KXBAT
C11	5.1 pF Chip Capacitor, B Case, ATC
C12A, B	0.01 μF, 100 V Chip Capacitors, Kemet #VJ1210Y103KXBAT
C13	3.9 pF Chip Capacitor, B Case, ATC
C15	1.2 pF Chip Capacitor, B Case, ATC
L1A, B	130 nH, Coilcraft #132–11SM
L2A, B	#24 AWG, 3 Turns Loose, Fair Rite #2643706001
L3A, B	3.85 nH, Coilcraft #0906–4
L4A, B	5.0 nH, Coilcraft #A02T
R1A, B, R2A, B R4A, B, R5A, B	180 Ω, 1/4 W Chip Resistors, Vishay Dale (1210)
R3A, B	12 Ω, 1/8 W Chip Resistors, Vishay Dale (1206)
PCB	MRF372 Printed Circuit Board Rev 1a, Rogers RO4350, Height 30 mils, ε_r = 3.48
Balun A, B	Vertical 860 MHz Broadband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, ε_r = 10.2



Vertical Balun Mounting Detail

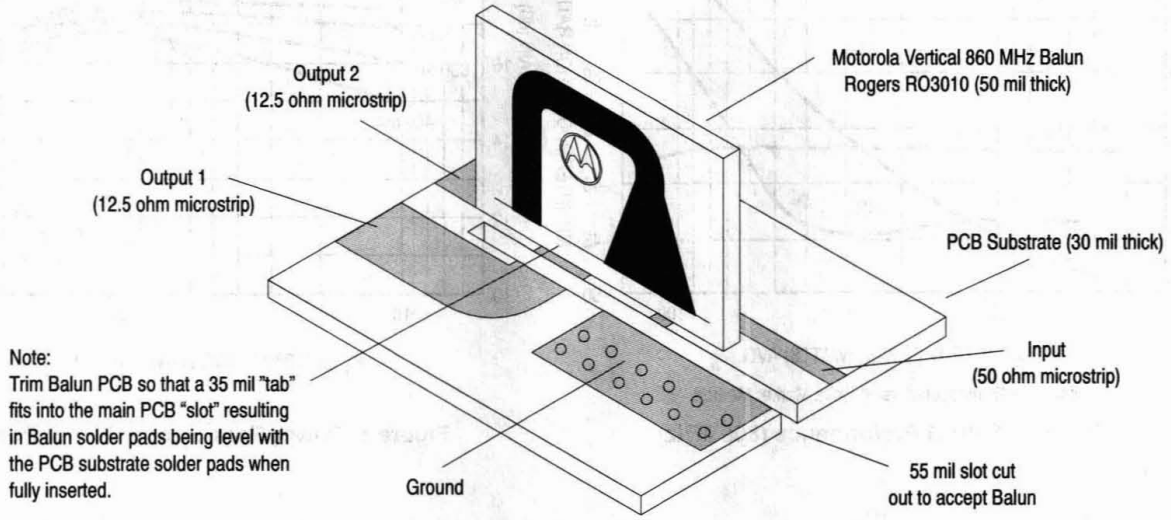
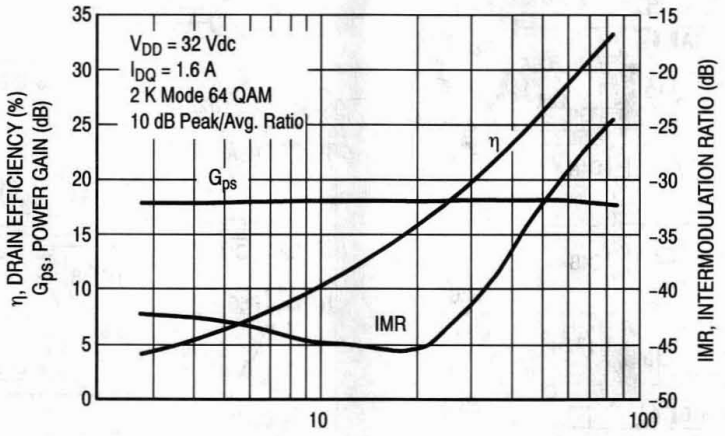


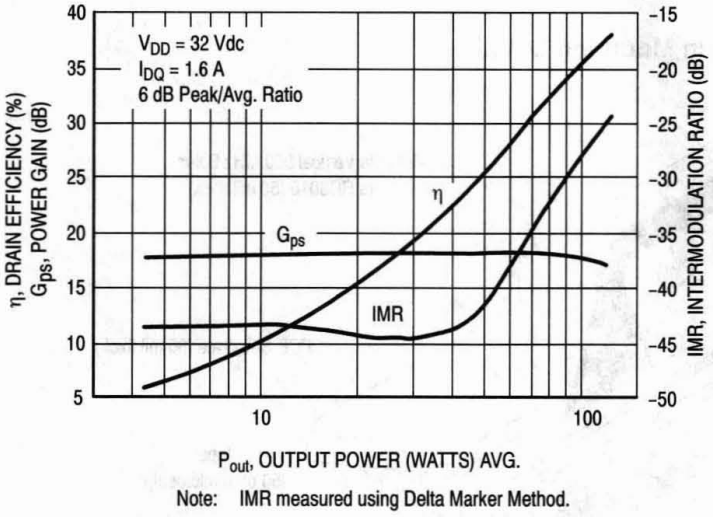
Figure 3. 860 MHz Narrowband Component Layout

TYPICAL TWO–TONE NARROWBAND CHARACTERISTICS



Note: IMR measured using Delta Marker Method.

Figure 4. COFDM Performance (860 MHz)



Note: IMR measured using Delta Marker Method.

Figure 5. 8–VSB Performance (860 MHz)

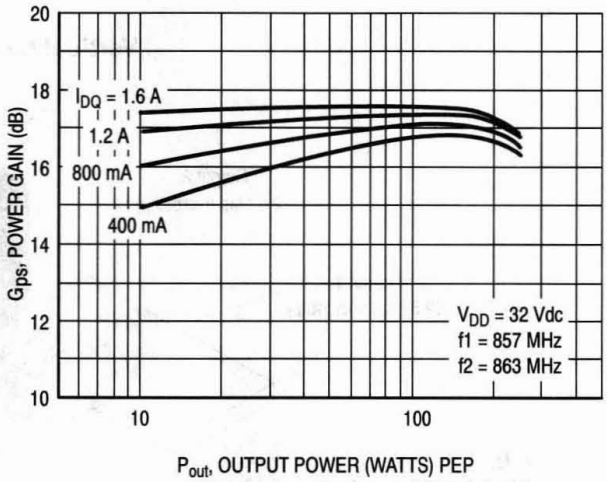


Figure 6. Power Gain versus Output Power

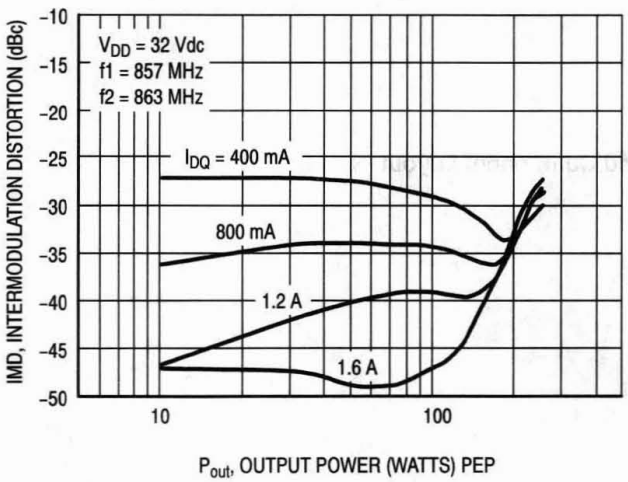


Figure 7. Intermodulation Distortion versus Output Power

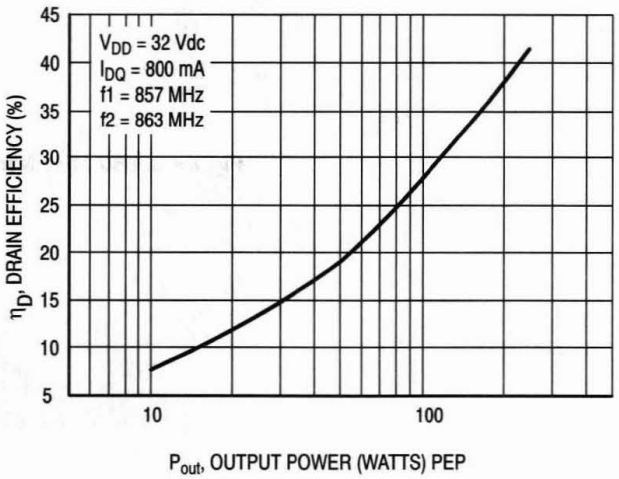
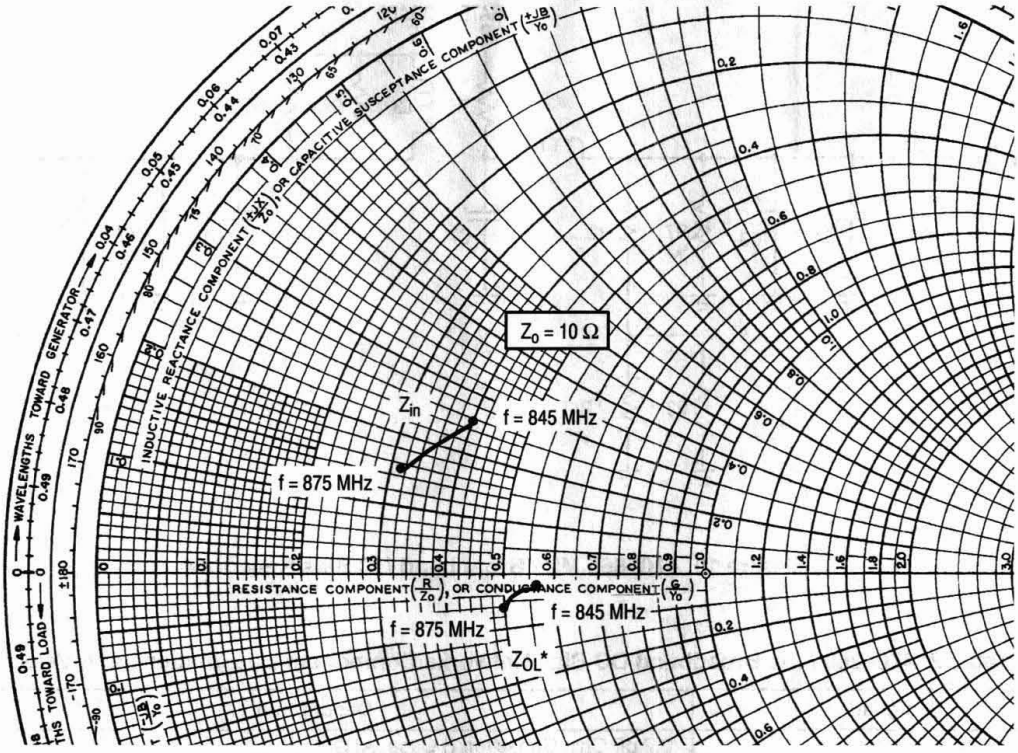


Figure 8. Drain Efficiency versus Output Power



V_{DD} = 32 V, I_{DQ} = 800 mA, P_{out} = 180 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
845	3.99 + j2.50	5.63 – j0.38
860	3.56 + j1.98	5.28 – j0.43
875	3.18 + j1.46	4.94 – j0.56
Harmonics		
f GHz	Z_{in} Ω	Z_{OL}* Ω
1.69	2.85 – j14.30	1.23 – j9.37
1.72	3.27 – j14.32	1.54 – j9.60
1.75	3.35 – j14.36	1.73 – j9.62

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{in} and Z_{OL}* were chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

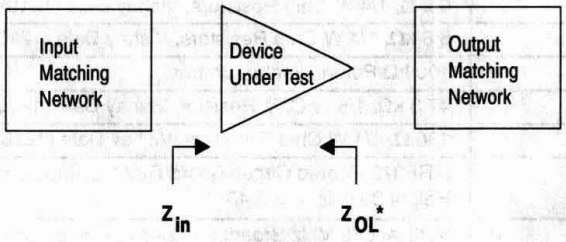


Figure 9. Narrowband Series Equivalent Input and Output Impedance

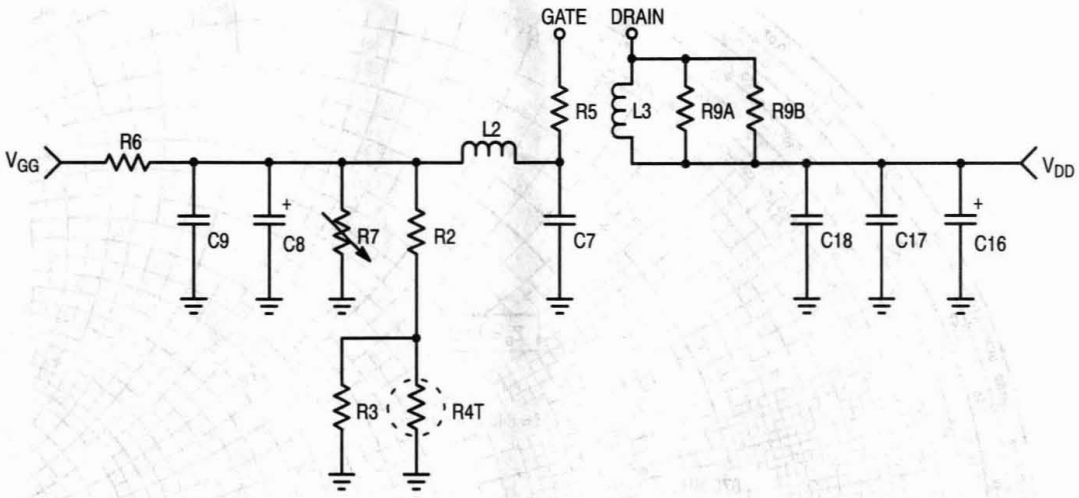
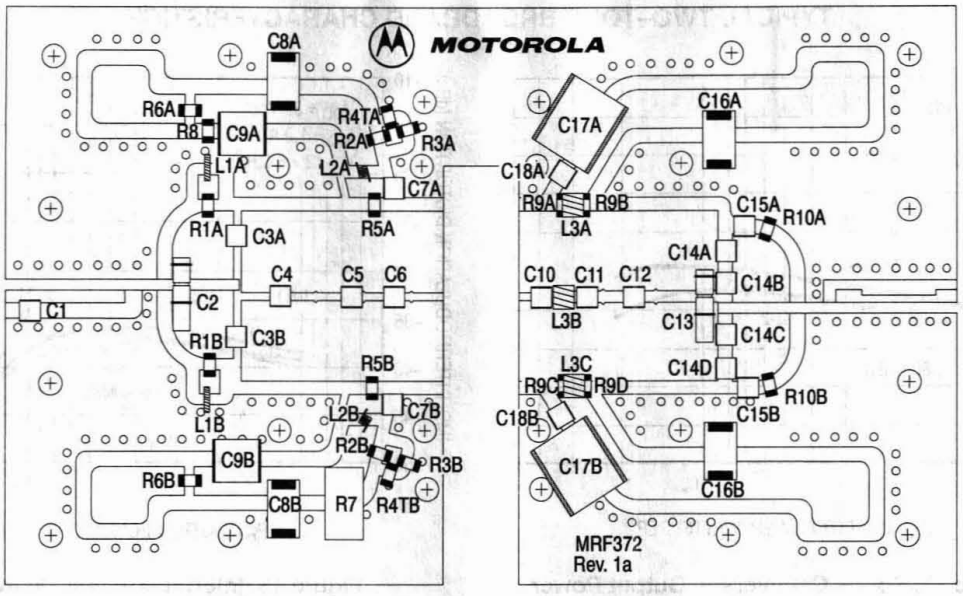


Figure 10. 470–860 MHz Broadband DC Bias Networks

Table 2. 470–860 MHz Broadband DC Bias Networks Component Designations and Values

Designation	Description
C1	0.7 pF Chip Capacitor, B Case, ATC
C2, C13	0.8 — 8.0 pF Variable Capacitors, Johansen Gigatrim
C3A, B, C14A, B, C, D	100 pF Chip Capacitors, B Case, ATC
C4	4.7 pF,Chip Capacitor, B Case, ATC
C5	7.5 pF Chip Capacitor, B Case, ATC
C6	10.0 pF Chip Capacitor, B Case, ATC
C7A, B	6.2 pF Chip Capacitors, A Case, ATC
C8A, B	22 μF, 22 V Tantalum Chip Capacitors, Kemet #T491D226K22AS
C9A, B	0.1 μF, 100 V Chip Capacitors, Vitramon #VJ3640Y104KXBAT
C10	13 pF Chip Capacitor, B Case, ATC
C11	6.8 pF Chip Capacitor, B Case, ATC
C12	3.9 pF Chip Capacitor, B Case, ATC
C15A, B	3.3 pF Chip Capacitors, B Case, ATC
C16A, B	10 μF, 35 V Tantalum Chip Capacitors, Kemet #T491D106K35AS
C17A, B	3.3 μF, 100 V Chip Capacitors, Vitramon #VJ3640Y335KXBAT
C18A, B	0.01 μF Chip Capacitors, B Case, ATC
L1A, B	12.55 nH, Coilcraft #1606–10
L2A, B	5.45 nH, Coilcraft #0906–5
L3A, B, C	12.5 nH, Coilcraft #A04T
R1A, B	10 Ω, 1/4 W Chip Resistors, Vishay Dale (1210)
R2A, B	2.2 kΩ, 1/4 W Chip Resistors, Vishay Dale (1210)
R3A, B, R10A, B	390 Ω, 1/8 W Chip Resistors, Vishay Dale (1206)
R4TA, B	520 Ω, Thermistor, Vishay #NTHS—1206J14520R5%
R5A, B	6.2 Ω, 1/4 W Chip Resistors, Vishay Dale (1210)
R6A, B	6.8 kΩ, 1/4 W Chip Resistors, Vishay Dale (1210)
R7	100 kΩ Potentiometer, Bourns
R8	47.3 kΩ, 1/8 W Chip Resistor, Vishay Dale (1206)
R9A, B, C, D	180 Ω, 1/4 W Chip Resistors, Vishay Dale (1210)
PCB	MRF372 Printed Circuit Board Rev 1a, Rogers RO4350, Height 30 mils, ε_r = 3.48
Balun A, B	Vertical 660 MHz Broadband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, ε_r = 10.2



Vertical Balun Mounting Detail

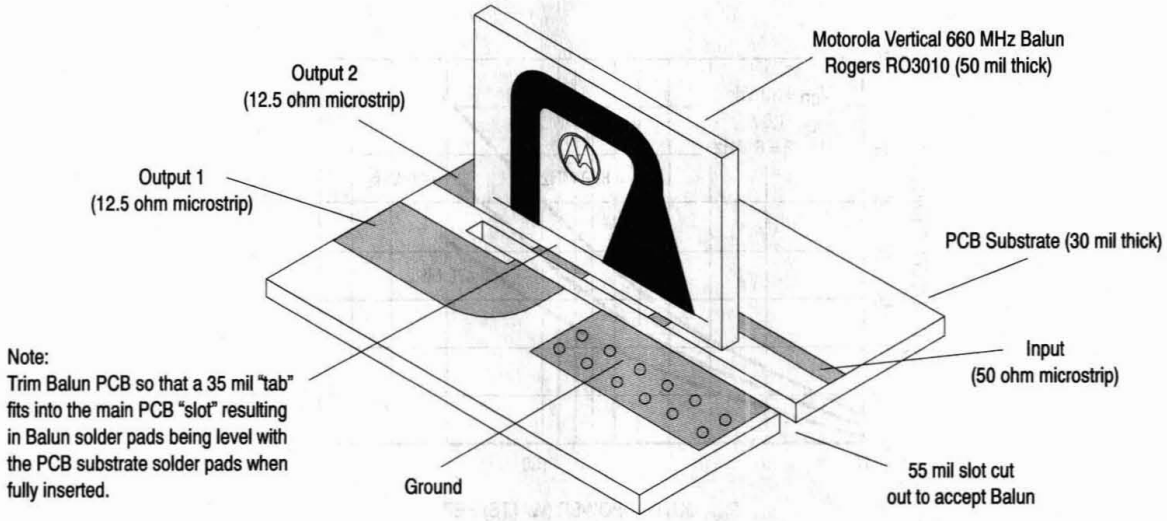


Figure 11. 470–860 MHz Broadband Component Layout

TYPICAL TWO–TONE BROADBAND CHARACTERISTICS

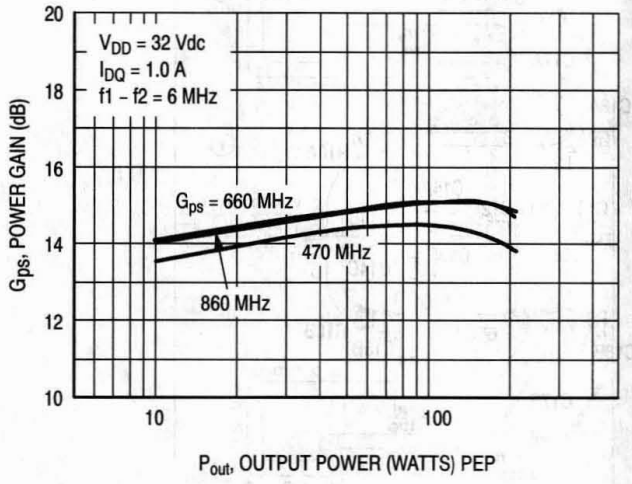


Figure 12. Power Gain versus Output Power

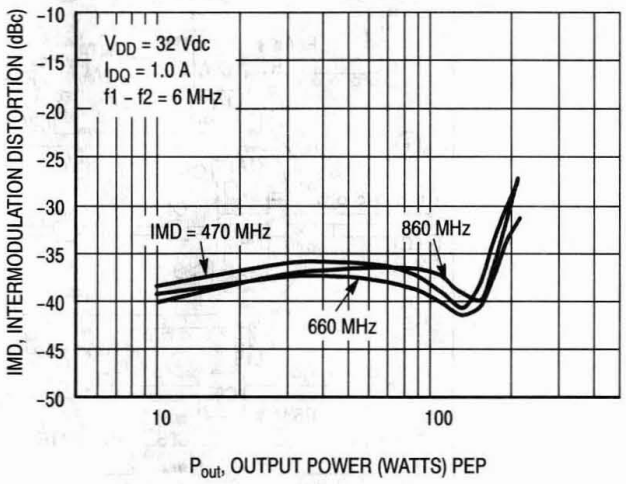


Figure 13. Intermodulation Distortion versus Output Power

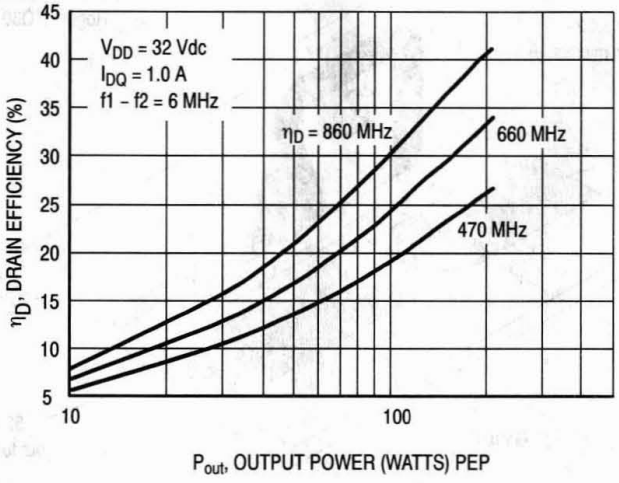
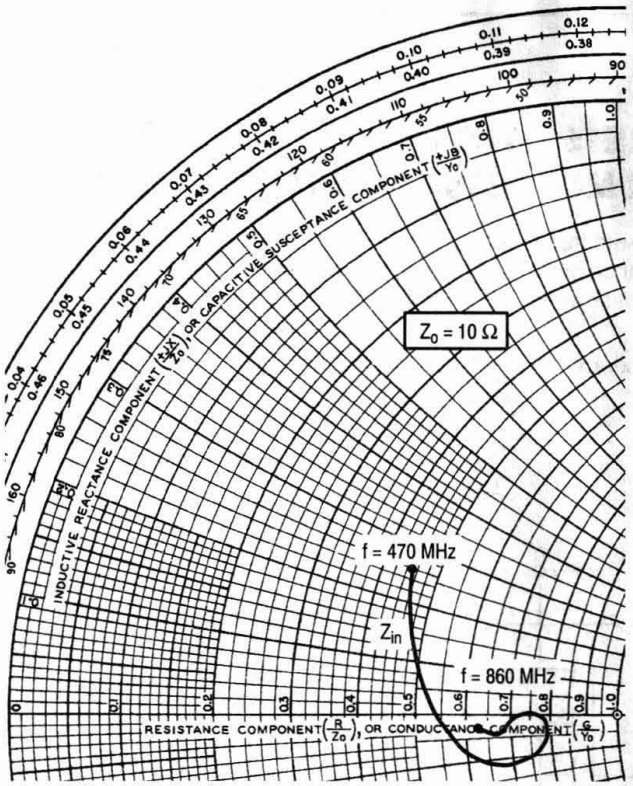
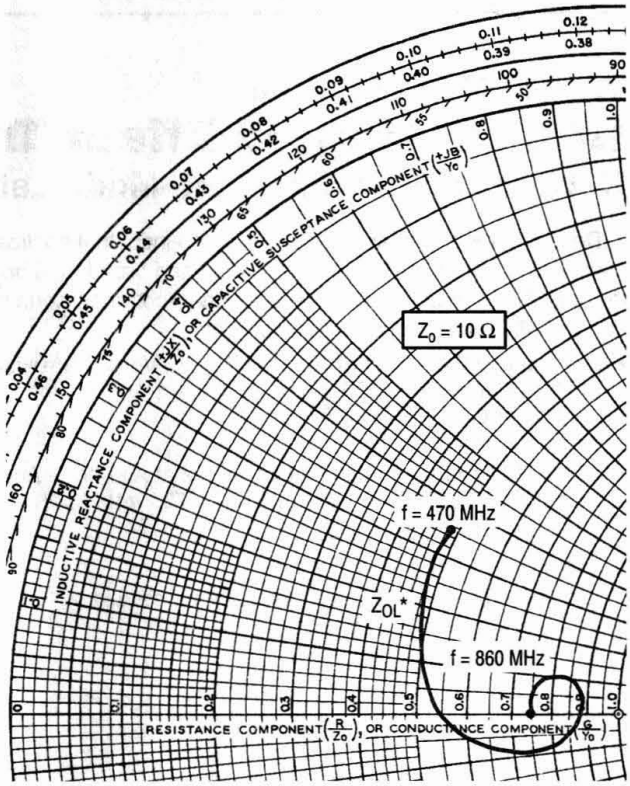


Figure 14. Drain Efficiency versus Output Power





V_{DD} = 32 V, I_{DQ} = 1.0 mA, P_{out} = 180 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
470	4.46 + j2.57	4.88 + j3.50
560	6.40 – j1.06	5.45 + j0.07
660	7.84 – j0.14	8.13 – j0.73
760	6.67 – j0.46	8.27 + j1.00
860	6.25 – j0.31	7.52 – j0.02

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{in} and Z_{OL}* were chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

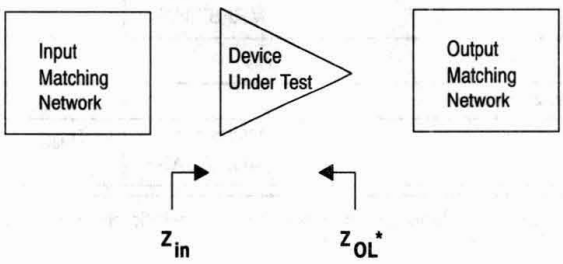


Figure 15. Broadband Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

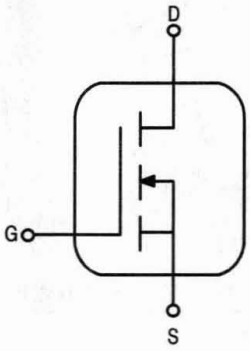
N–Channel Enhancement–Mode Lateral MOSFETs

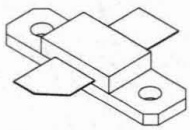
MRF373A
MRF373AS

470 – 860 MHz, 75 W, 32 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

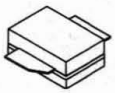
Designed for broadband commercial and industrial applications with frequencies from 470 to 860 MHz. The high gain and broadband performance of these devices make them ideal for large–signal, common source amplifier applications in 28/32 volt transmitter equipment.

- Typical CW Performance at 860 MHz, 32 Volts, Narrowband Fixture
  Output Power — 75 Watts
  Power Gain — 18.2 dB
  Efficiency — 60%
- 100% Tested for Load Mismatch Stress at All Phase Angles with 10:1 VSWR @ 32 Vdc, 860 MHz, 75 Watts (CW)
- Integrated ESD Protection
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters





CASE 360B–05, STYLE 1
(NI–360)
(MRF373A)



CASE 360C–05, STYLE 1
(NI–360S)
(MRF373AS)

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain–Source Voltage		V_{DSS}	70	Vdc
Gate–Source Voltage		V_{GS}	+15, – 0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	MRF373A MRF373AS	P_D	197 1.12 278 1.59	Watts W/°C Watts W/°C
Storage Temperature Range		T_{stg}	– 65 to +150	°C
Operating Junction Temperature		T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions		Class
Human Body Model		1 (Minimum)
Machine Model	MRF373A MRF373AS	M2 (Minimum) M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case	MRF373A MRF373AS	$R_{\theta JC}$	0.89 0.63	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 1 μA)	$V_{(BR)DSS}$	70	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 32 V, I_D = 100 mA)	$V_{GS(Q)}$	2.5	3.3	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	—	0.41	0.45	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 32 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	98.5	—	pF
Output Capacitance (V_{DS} = 32 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	49	—	pF
Reverse Transfer Capacitance (V_{DS} = 32 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2	—	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 32 V, P_{out} = 75 W CW, I_{DQ} = 200 mA, f = 860 MHz)	G_{ps}	16.5	18.2	—	dB
Drain Efficiency (V_{DD} = 32 V, P_{out} = 75 W CW, I_{DQ} = 200 mA, f = 860 MHz)	η	56	60	—	%
Load Mismatch (V_{DD} = 32 V, P_{out} = 75 W CW, I_{DQ} = 200 mA, f = 860 MHz, Load VSWR at 10:1 at All Phase Angles)	ψ	No Degradation in Output Power			

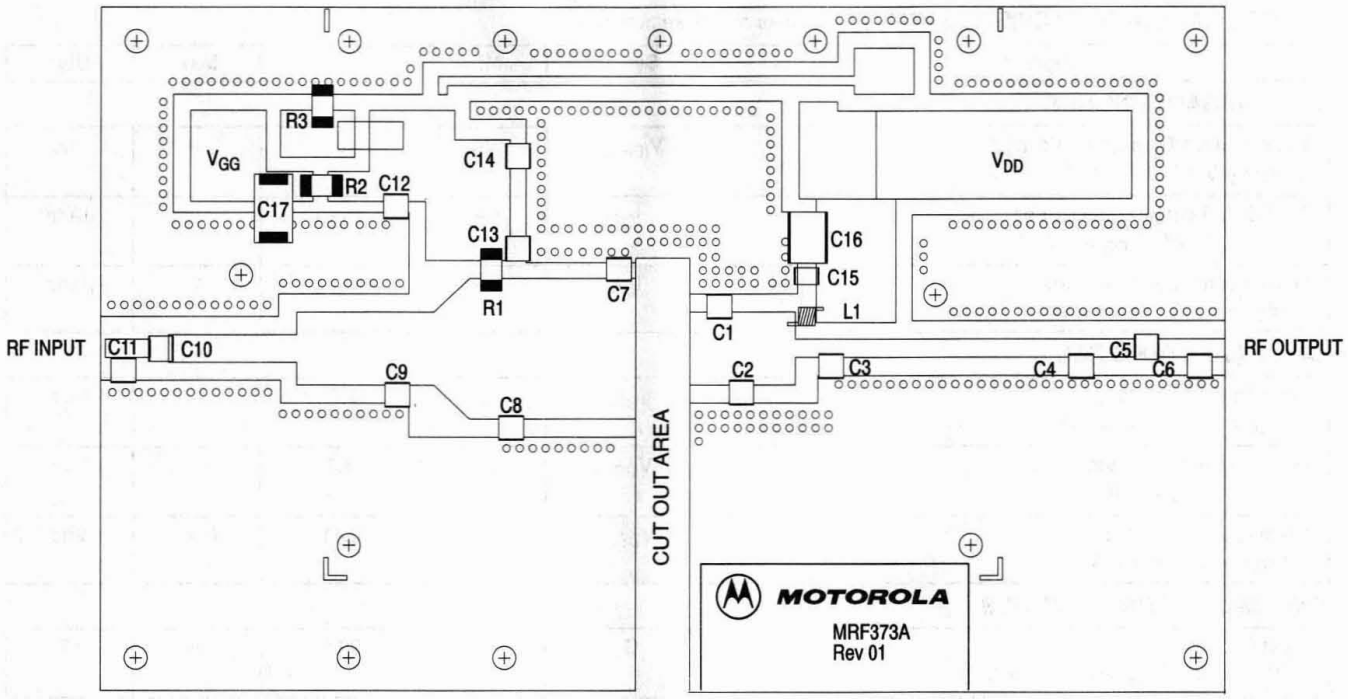


Figure 1. MRF373A/AS Narrowband Test Circuit Component Layout

Table 1. MRF373A/AS Narrowband Test Circuit Component Layout Designations and Values

Designation	Description
C1, C2	18 pF Chip Capacitors, B Case, ATC
C3	12 pF Chip Capacitor, B Case, ATC
C4	1.8 pF Chip Capacitor, B Case, ATC
C5, C10	51 pF Chip Capacitors, B Case, ATC
C6	0.3 pF Chip Capacitor, B Case, ATC (Used only on the MRF373AS)
C7	15 pF Chip Capacitor, B Case, ATC
C8	10 pF Chip Capacitor, B Case, ATC
C9	2.7 pF Chip Capacitor, B Case, ATC
C11	0.5 pF Chip Capacitor, B Case, ATC
C12	1000 pF Chip Capacitor, B Case, ATC
C13	39 pF Chip Capacitor, B Case, ATC
C14, C15	470 pF Chip Capacitors, B Case, ATC
C16	2.2 μF, 100 V Chip Capacitor, Vishay #VJ3640Y225KXBAT
C17	10 μF, 35 V Tantalum Capacitor, Kemet #T491D106K35AS
L1A	12 nH, Coilcraft #A04T
R1, R2	390 Ω, 1/2 Ω Chip Resistors, Vishay Dale (2010)
R3	1 kΩ, 1/2 Ω Chip Resistor, Vishay Dale (2010)
PCB	MRF373 Printed Circuit Board Rev 01, CuClad 250 (GX–0300–55), Height 30 mils, ε_r = 2.55

TYPICAL CHARACTERISTICS

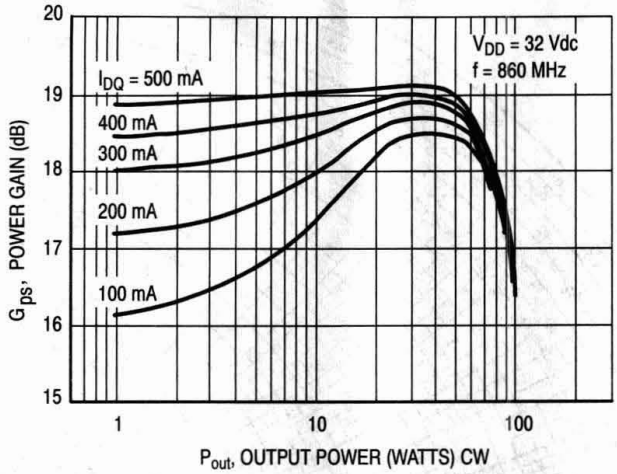


Figure 2. Power Gain versus Output Power

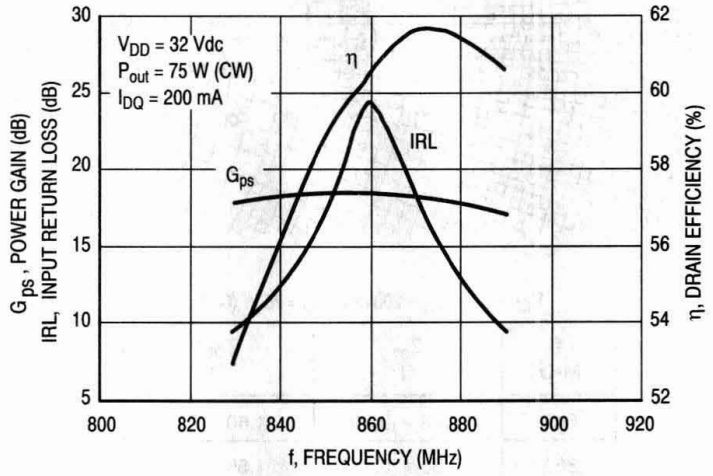


Figure 3. Performance in Narrowband Circuit

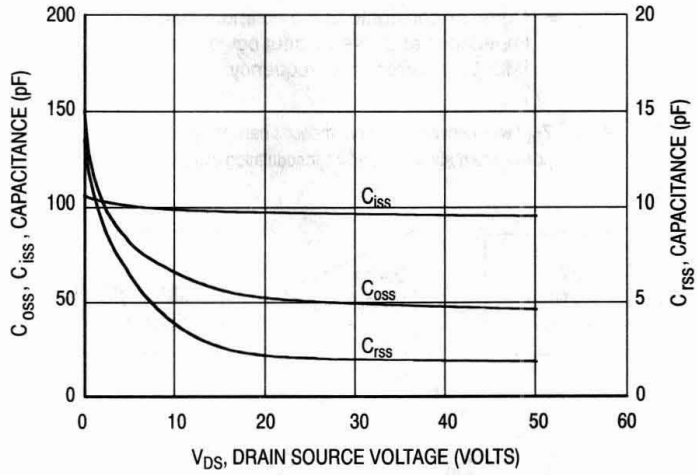
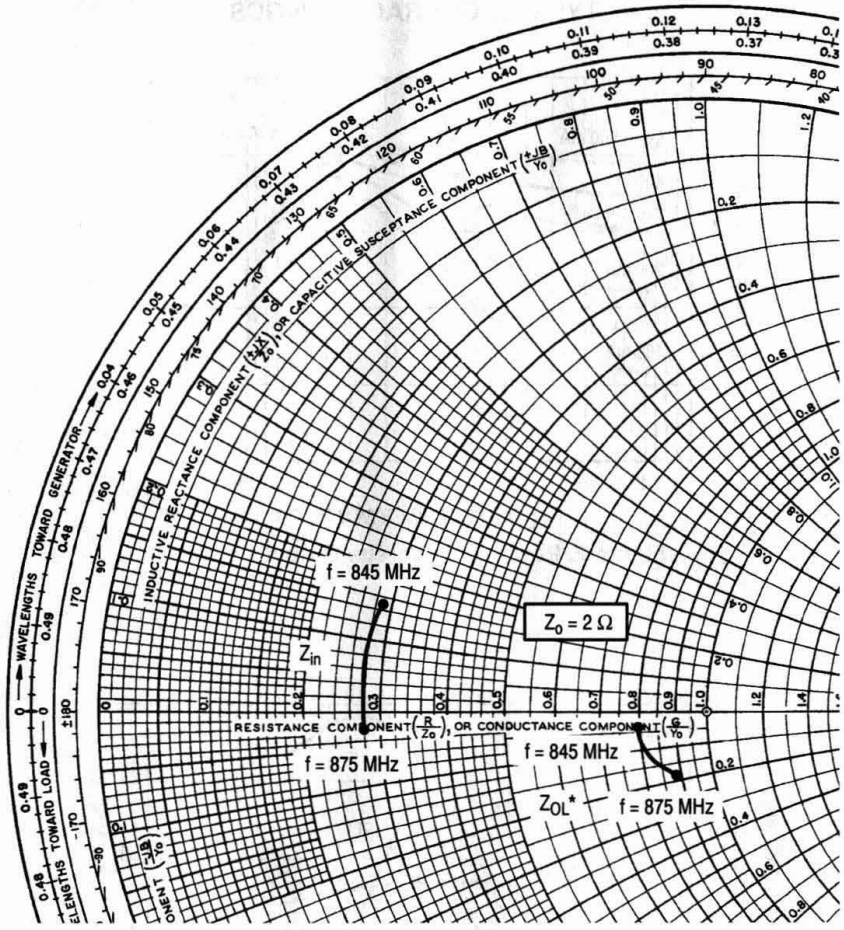


Figure 4. Capacitance versus Voltage



V_{DD} = 32 V, I_{DQ} = 200 mA, P_{out} = 75 W (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
845	0.58 + j0.29	1.60 – j0.07
860	0.56 + j0.11	1.65 – j0.22
875	0.56 – j0.06	1.79 – j0.38

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

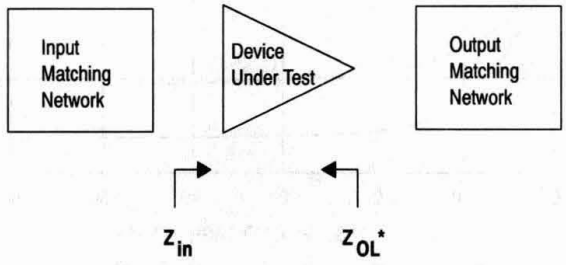


Figure 5. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field-Effect Transistor

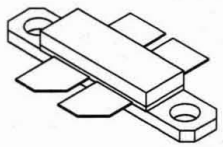
N–Channel Enhancement–Mode Lateral MOSFET

MRF374A

Designed for broadband commercial and industrial applications with frequencies from 470 to 860 MHz. The high gain and broadband performance of this device make it ideal for large–signal, common source amplifier applications in 28/32 volt transmitter equipment.

- Typical Two–Tone Performance @ 860 MHz, 32 Volts, Narrowband Fixture
  Output Power — 130 Watts PEP
  Power Gain — 17.3 dB
  Efficiency — 41%
  IMD — –32.5 dBc
- 100% Tested for Load Mismatch Stress at All Phase Angles with 10:1 VSWR @ 32 Vdc, 860 MHz, 130 Watts, f1 = 857 MHz, f2 = 863 MHz
- Integrated ESD Protection
- Excellent Thermal Stability
- Characterized with Differential Large–Signal Impedance Parameters

470 – 860 MHz, 130 W, 32 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET



CASE 375F–04, STYLE 1
(NI–650)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	70	Vdc
Gate–Source Voltage	V_{GS}	+15, – 0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	302 1.72	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

THERMAL CHARACTERISTICS

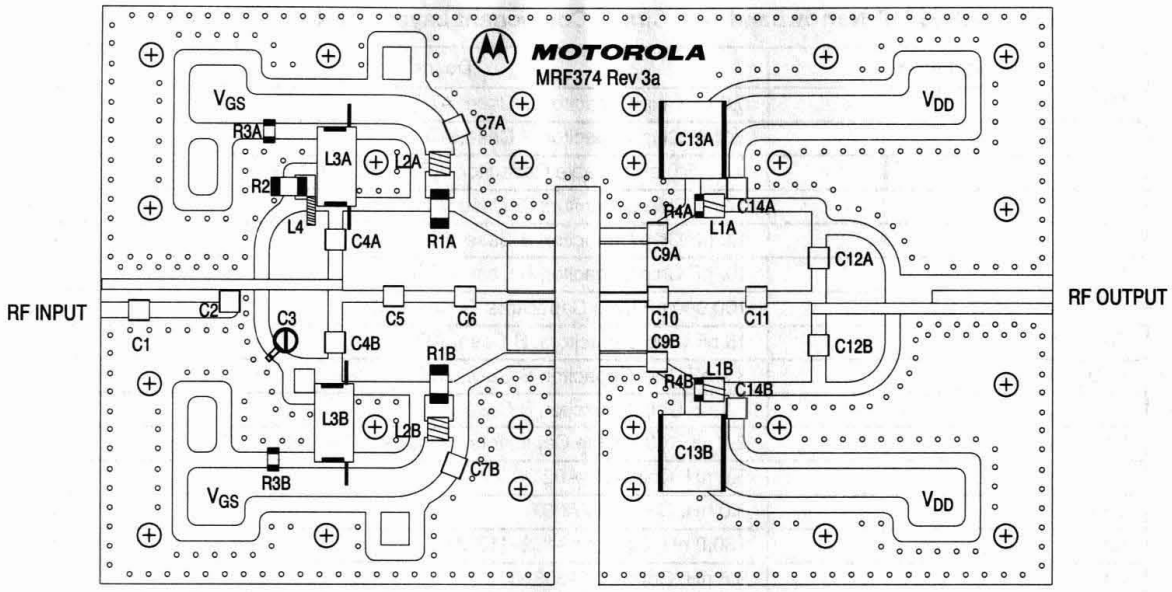
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.58	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D =10 μA)	$V_{(BR)DSS}$	70	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 32 V, I_D = 100 mA)	$V_{GS(Q)}$	2.5	3.3	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	—	0.41	0.45	Vdc
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 32 V, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	—	97.3	—	pF
Output Capacitance (V_{DS} = 32 V, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	—	49	—	pF
Reverse Transfer Capacitance (V_{DS} = 32 V, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	—	1.91	—	pF
FUNCTIONAL CHARACTERISTICS, TWO–TONE NARROWBAND TESTING (2) (MRF374A)					
Common Source Power Gain (V_{DD} = 32 Vdc, P_{out} = 130 W PEP, I_{DQ} = 2 x 200 mA, f1 = 857 MHz, f2 = 863 MHz)	G_{ps}	16	17.3	—	dB
Drain Efficiency (V_{DD} = 32 Vdc, P_{out} = 130 W PEP, I_{DQ} = 2 x 200 mA, f1 = 857 MHz, f2 = 863 MHz)	η	36	41.2	—	%
Intermodulation Distortion (V_{DD} = 32 Vdc, P_{out} = 130 W PEP, I_{DQ} = 2 x 200 mA, f1 = 857 MHz, f2 = 863 MHz)	IMD	—	–32.5	–28	dB
Load Mismatch (V_{DD} = 32 Vdc, P_{out} = 130 W Two–Tone, I_{DQ} = 2 x 200 mA, f1 = 857 MHz, f2 = 863 MHz, VSWR 10:1 at All Phase Angles of Test)		No Degradation in Output Power			
TYPICAL TWO–TONE BROADBAND (IN MRF374 BROADBAND CIRCUIT)					
Common Source Power Gain (V_{DD} = 32 Vdc, P_{out} = 100 W PEP, I_{DQ} = 750 mA, f1 = 857 MHz, f2 = 863 MHz)	G_{ps}	—	15.8	—	dB
Drain Efficiency (V_{DD} = 32 Vdc, P_{out} = 100 W PEP, I_{DQ} = 750 mA, f1 = 857 MHz, f2 = 863 MHz)	η	—	35	—	%
Intermodulation Distortion (V_{DD} = 32 Vdc, P_{out} = 100 W PEP, I_{DQ} = 750 mA, f1 = 857 MHz, f2 = 863 MHz)	IMD	—	34.5	—	dB

(1) Each side of device measured separately.
(2) Measured in push–pull configuration.



Vertical Balun Mounting Detail

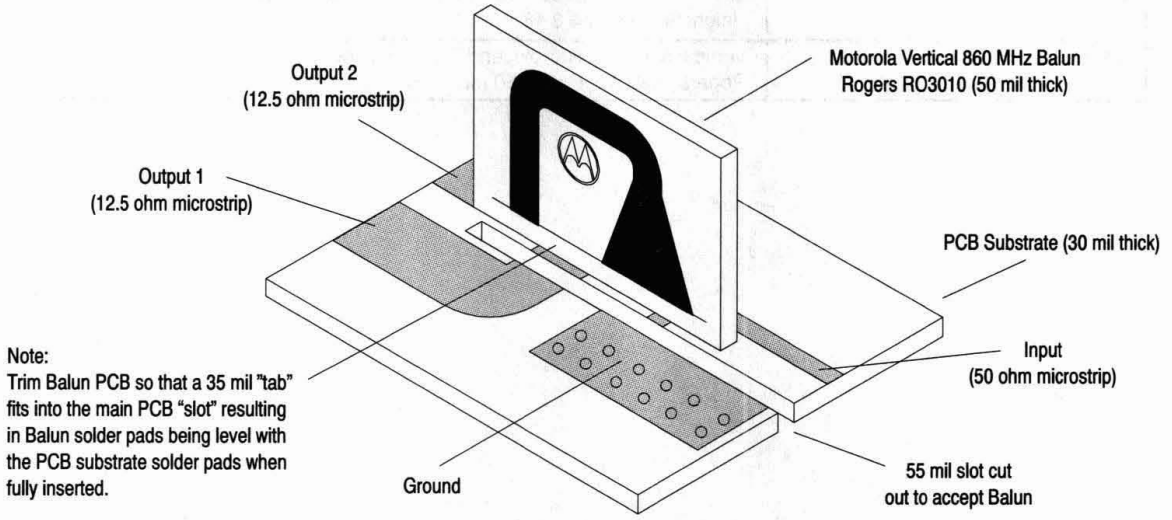
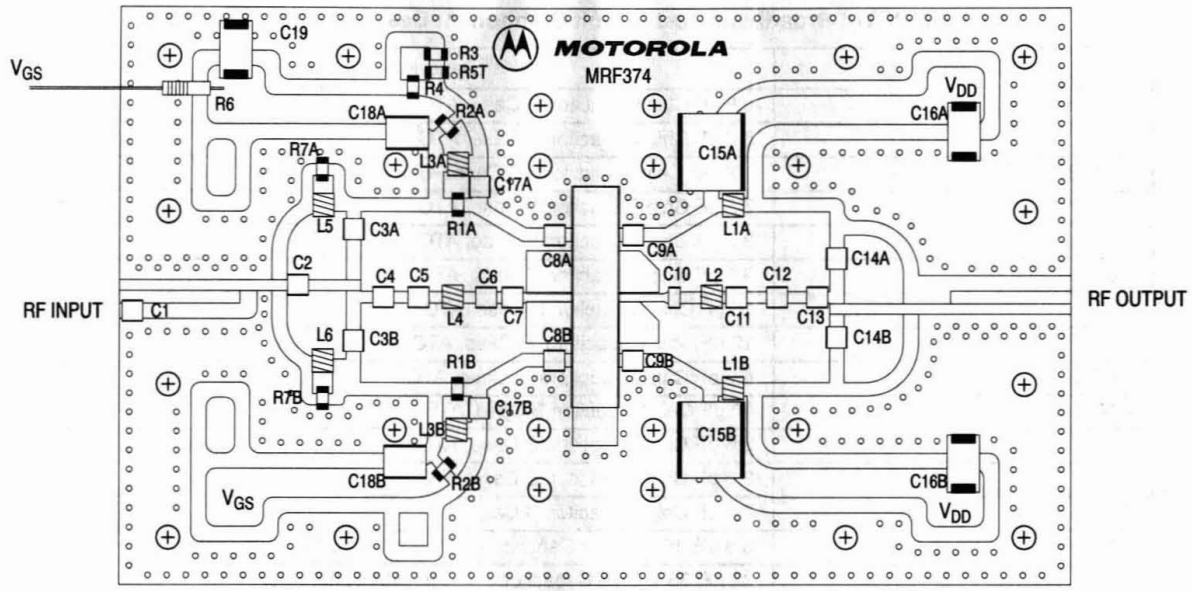


Figure 1. MRF374A Narrowband Test Circuit Component Layout

Table 1. MRF374A Narrowband Test Circuit Component Layout Designations and Values

Designation	Description
C1	0.8 pF Chip Capacitor, B Case, ATC
C2	2.2 pF Chip Capacitor, B Case, ATC
C3	0.5 – 5.0 pF Variable Capacitor, Johanson Gigatrim
C4A, B, C12A, B	47 pF Chip Capacitors, B Case, ATC
C5	1.0 pF Chip Capacitor, B Case, ATC
C6	10 pF Chip Capacitor, B Case, ATC
C7A, B, C14A, B	100,000 pF Chip Capacitors, B Case, ATC
C9A, B	15 pF Chip Capacitors, B Case, ATC
C10	3.9 pF Chip Capacitor, B Case, ATC
C11	5.1 pF Chip Capacitor, B Case, ATC
C13A, B	2.2 μF, 100 V Chip Capacitors, Vishay #VJ3640Y225KXBAT
L1A, B	5.0 nH, Coilcraft #A02T
L2A, B	8.0 nH, Coilcraft #A03T
L3A, B	130.0 nH, Coilcraft #132–11SMJ
L4	8.8 nH, Coilcraft #1606–8
R1A, B	51 Ω, 1/4 W Chip Resistors, Vishay Dale (1210)
R2	10 Ω, 1/2 W Chip Resistor, Vishay Dale (2010)
R3A, B	3.3 kΩ, 1/8 W Chip Resistors, Vishay Dale (1206)
R4A, B	180 Ω, 1/4 W Chip Resistors, Vishay Dale (1210)
PCB	MRF374 Printed Circuit Board Rev 03, Rogers RO4350, Height 30 mils, ε_r = 3.48
Balun B1A, B	Vertical 860 MHz Narrowband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, ε_r = 10.2



Vertical Balun Mounting Detail

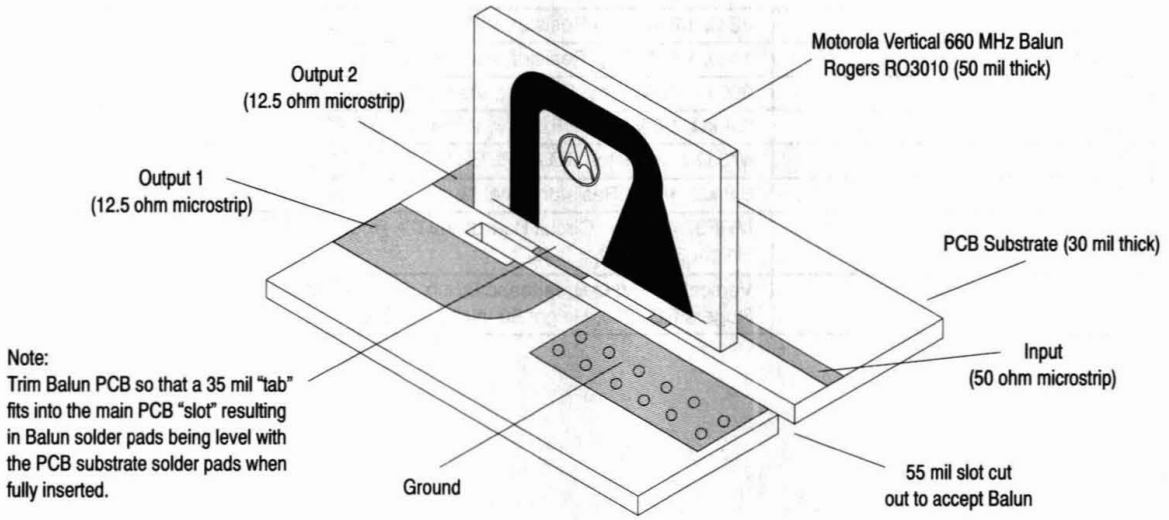


Figure 2. MRF374 Broadband Test Circuit Component Layout

Table 2. MRF374 Broadband Test Circuit Component Designations and Values

Designation	Description
C1	0.8 pF Chip Capacitor, B Case, ATC
C2	8.2 pF Chip Capacitor, B Case, ATC
C3A, B, C14A, B	100 pF Chip Capacitors, B Case, ATC
C4	7.5 pF Chip Capacitor, B Case, ATC
C5	3.0 pF Chip Capacitor, B Case, ATC
C6	9.1 pF Chip Capacitor, B Case, ATC
C7	15 pF Chip Capacitor, B Case, ATC
C8A, B	12 pF Chip Capacitors, B Case, ATC
C9A, B	4.7 pF Chip Capacitors, B Case, ATC
C10	10 pF Chip Capacitor, B Case, ATC
C11	3.6 pF Chip Capacitor, B Case, ATC
C12	3.0 pF Chip Capacitor, B Case, ATC
C13	2.7 pF Chip Capacitor, B Case, ATC
C15A, B	3.3 μF, 100 V Chip Capacitors, Vitramon #VJ3640Y335KXBAT
C16A, B	22 μF, 35 V Chip Capacitors, Kemet #491D226K035AS
C17A, B	3.9 pF Chip Capacitors, B Case, ATC
C18A, B	2.2 μF, 50 V Chip Capacitors, Vitramon #VJ2225Y225KXAAT
C19	10 μF, 35 V Chip Capacitor, Kemet #T491D106K035AS
L1A, B, L3A, B, L4, L5	8.0 nH, Coilcraft #A03T
L2, L6	12.5 nH, Coilcraft #A04T
R1A, B	22 Ω, 1/8 W Chip Resistor, Vishay Dale (1206)
R2A, B, R7A, B	10 Ω, 1/8 W Chip Resistor, Vishay Dale (1206)
R3	390 Ω, 1/8 W Chip Resistor, Vishay Dale (1206)
R4	2.4 kΩ, 1/8 W Chip Resistor, Vishay Dale (1206)
R5T	470 Ω Thermistor, KOA SPEER MOT #0680149M01
R6	6.8 kΩ, 1/2 W Resistor (Axial Lead), Vishay Dale (2010)
PCB	MRF374 Printed Circuit Board Rev 03, Rogers RO4350, Height 30 mils, $\varepsilon_r = 3.48$
Balun B1, B2	Vertical 660 MHz Broadband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, $\varepsilon_r = 10.2$

MRF374A TYPICAL CHARACTERISTICS

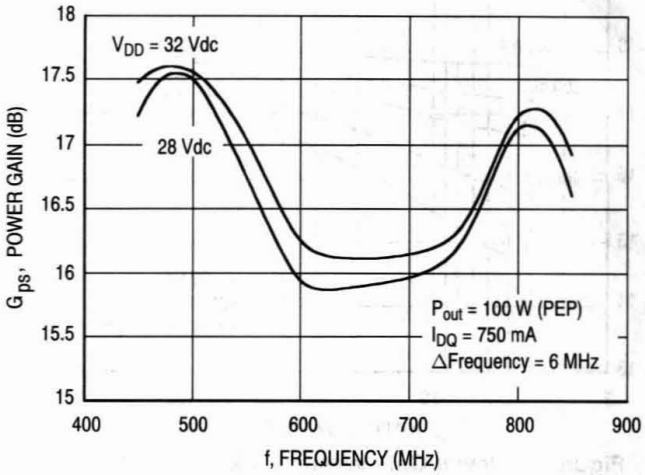


Figure 3. Gain versus Frequency in Broadband Circuit

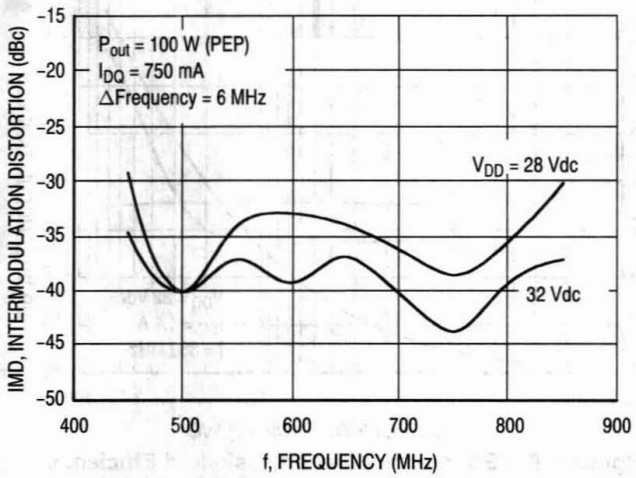


Figure 4. Intermodulation Distortion versus Frequency in Broadband Circuit

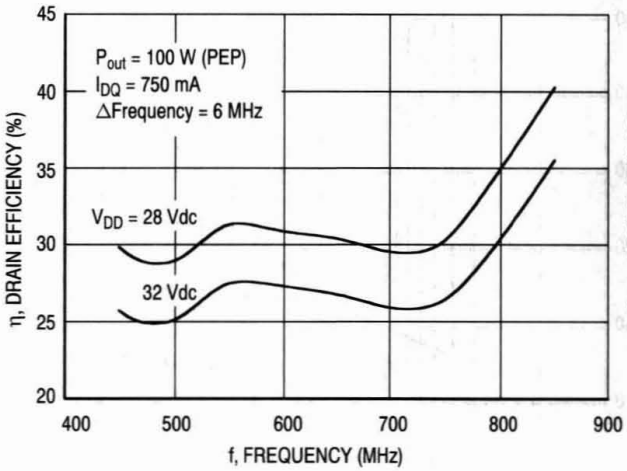


Figure 5. Drain Efficiency versus Frequency in Broadband Circuit

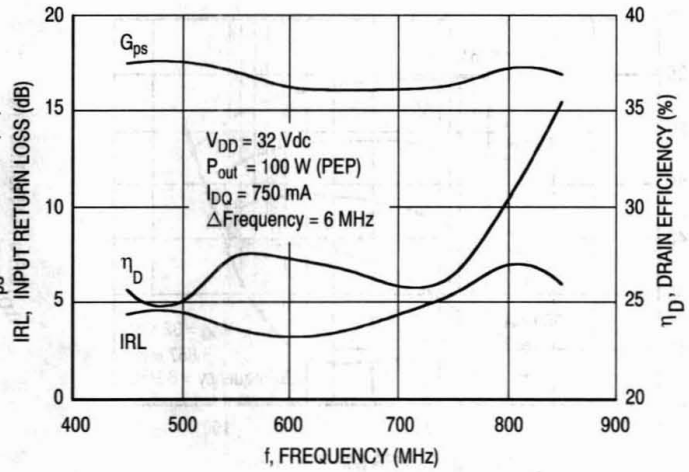


Figure 6. Performance in Broadband Circuit

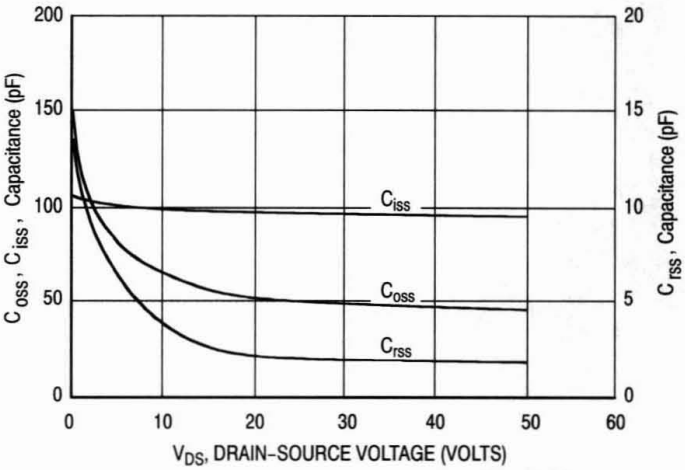


Figure 7. Capacitance versus Voltage

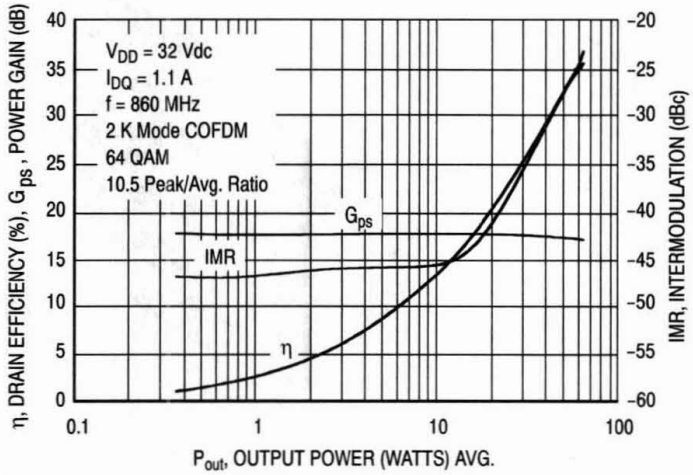


Figure 8. COFDM Intermodulation, Gain and Efficiency versus Output Power in Broadband Circuit

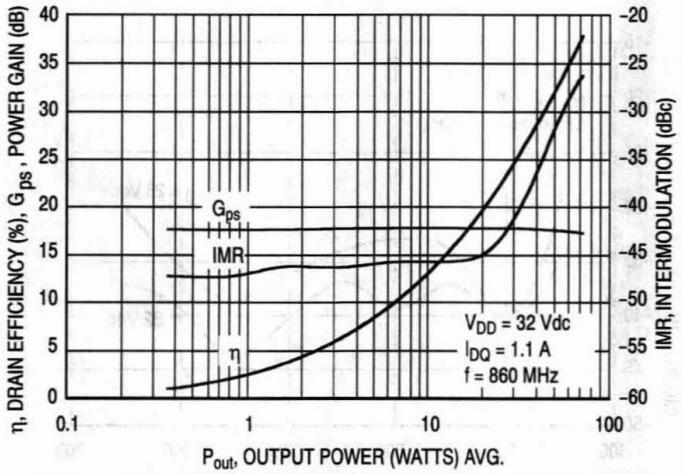


Figure 9. 8–VSB Intermodulation, Gain and Efficiency versus Output Power in Broadband Circuit

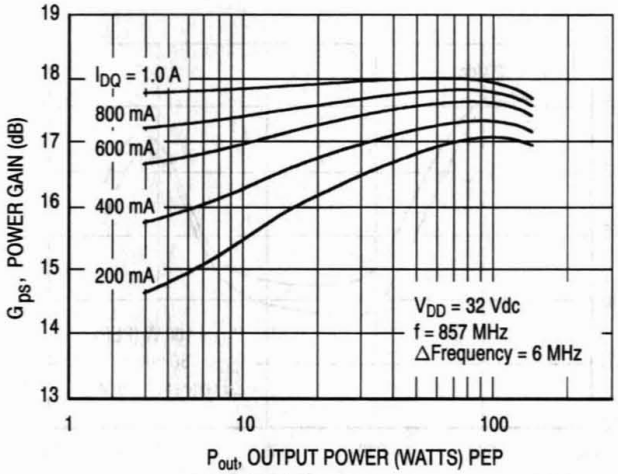


Figure 10. Power Gain versus Peak Output Power in Narrowband Circuit

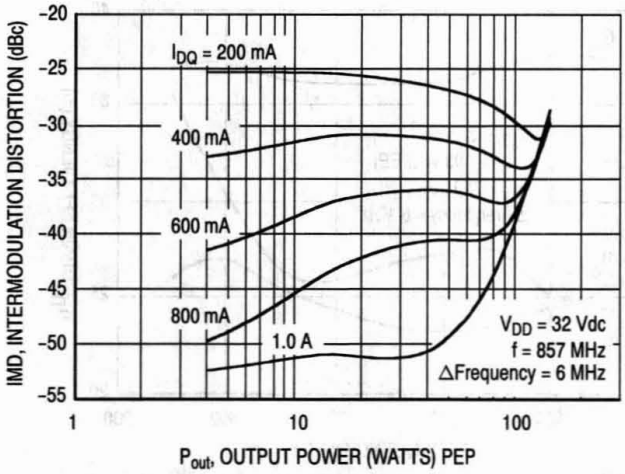


Figure 11. Intermodulation Distortion versus Peak Output Power in Narrowband Circuit

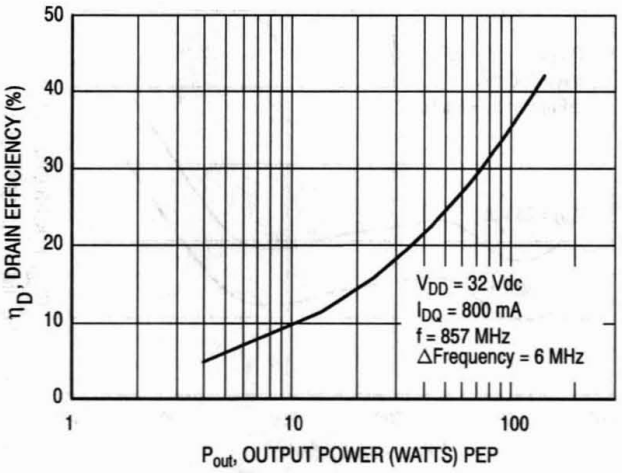


Figure 12. Drain Efficiency versus Peak Output Power in Narrowband Circuit

MRF374A TYPICAL CHARACTERISTICS

V_{DD} = 28 Vdc

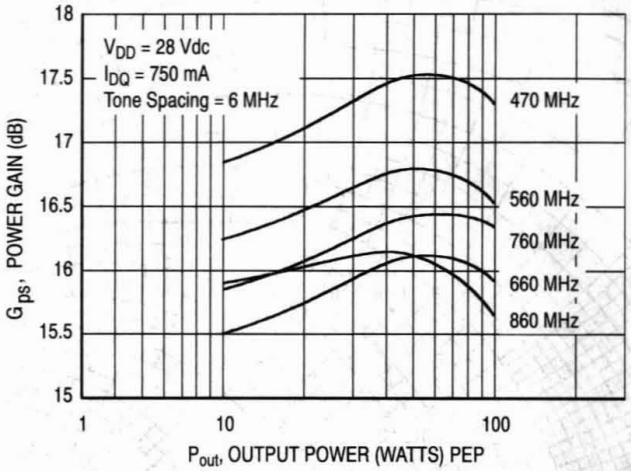


Figure 13. Power Gain versus Peak Output Power in Broadband Circuit

V_{DD} = 32 Vdc

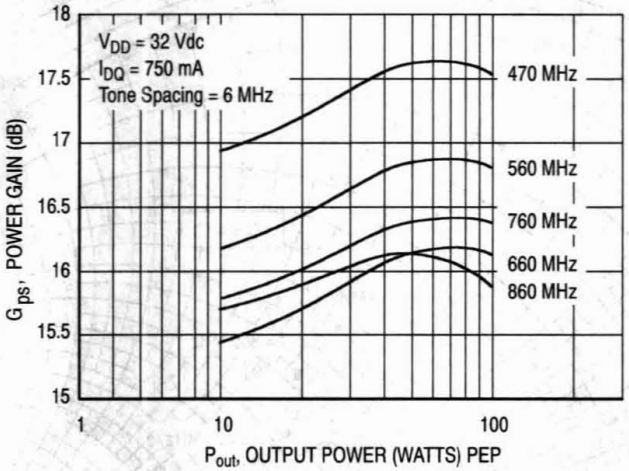


Figure 14. Power Gain versus Peak Output Power in Broadband Circuit

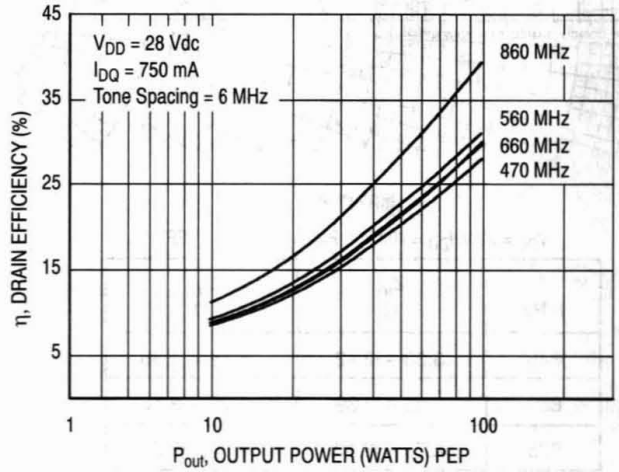


Figure 15. Drain Efficiency versus Peak Output Power in Broadband Circuit

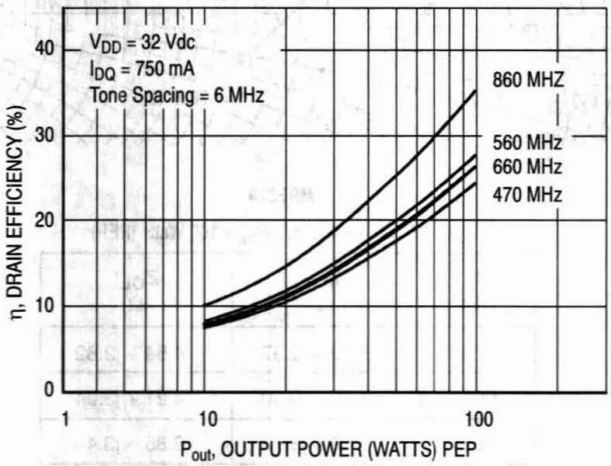


Figure 16. Drain Efficiency versus Peak Output Power in Broadband Circuit

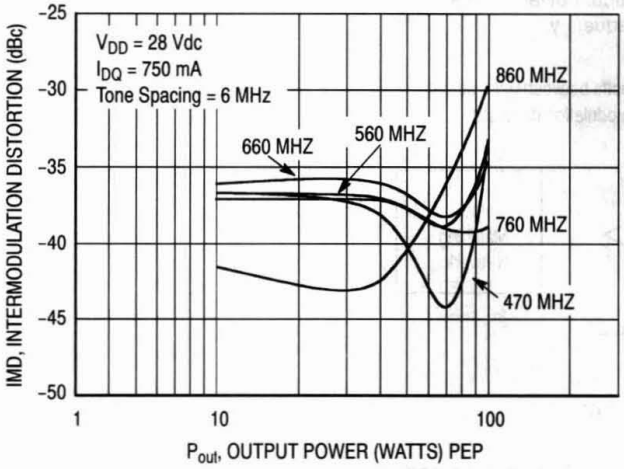


Figure 17. Intermodulation Distortion versus Peak Output Power in Broadband Circuit

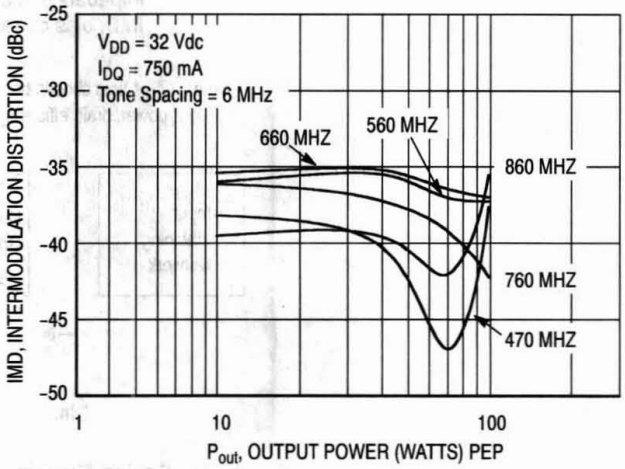
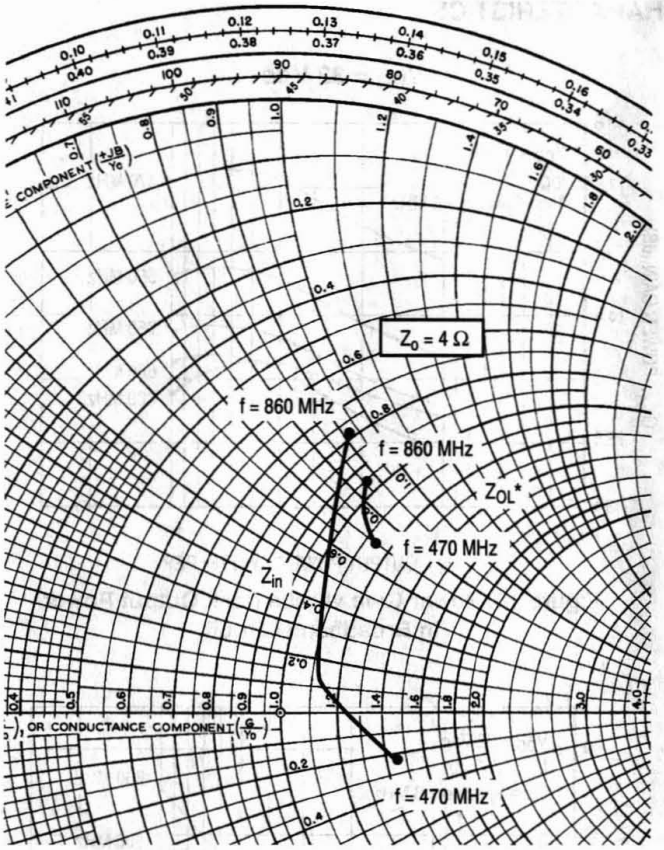


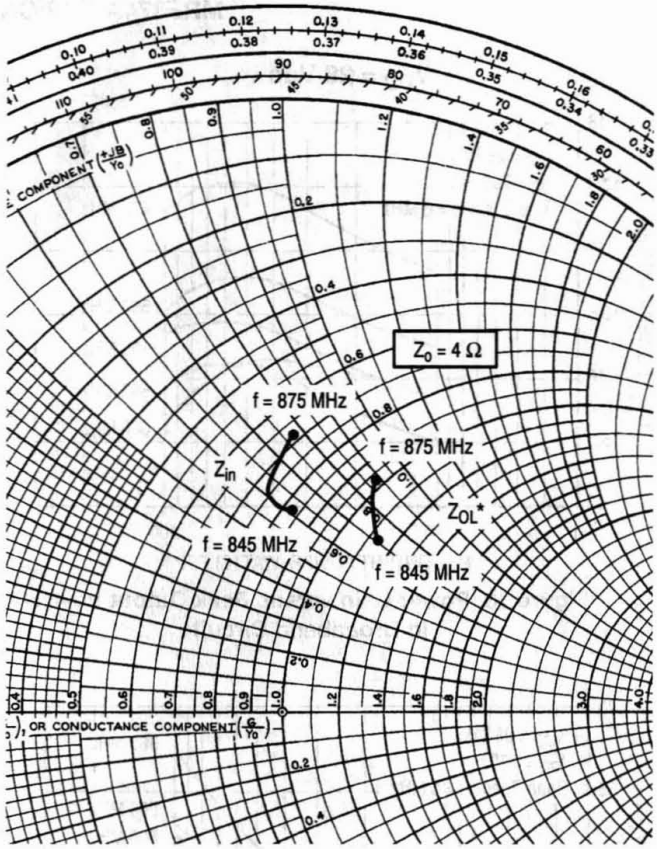
Figure 18. Intermodulation Distortion versus Peak Output Power in Broadband Circuit



MRF374

V_{DD} = 28 V, I_{DQ} = 400 mA, P_{out} = 100 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
470	5.79 – j0.97	4.54 + j2.82
660	4.52 + j0.50	4.21 + j3.04
860	3.16 + j3.73	3.86 + j3.44



MRF374A

V_{DD} = 32 V, I_{DQ} = 400 mA, P_{out} = 130 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
845	3.33 + j2.42	4.56 + j2.86
860	3.03 + j2.39	4.22 + j3.16
875	2.73 + j3.10	3.87 + j3.52

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

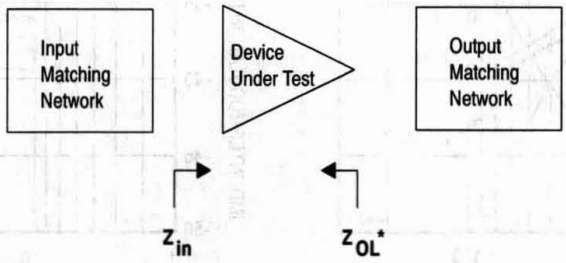


Figure 19. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistor

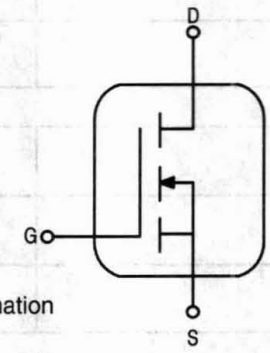
N–Channel Enhancement–Mode Lateral MOSFET

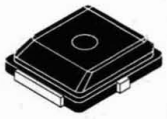
MRF1511T1

175 MHz, 8 W, 7.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

The MRF1511T1 is designed for broadband commercial and industrial applications at frequencies to 175 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 7.5 volt portable FM equipment.

- Specified Performance @ 175 MHz, 7.5 Volts
  Output Power — 8 Watts
  Power Gain — 11.5 dB
  Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 9.5 Vdc, 175 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- RF Power Plastic Surface Mount Package
- Available in Tape and Reel.
  T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.





CASE 466–02, STYLE 1
(PLD–1.5)

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	40	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	62.5 0.5	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

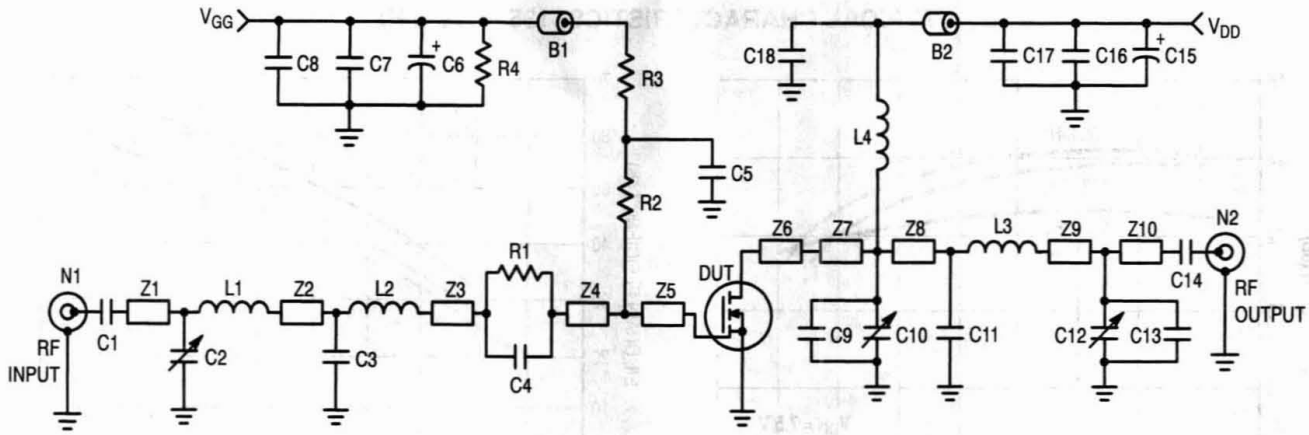
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current (V_{DS} = 35 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 7.5 Vdc, I_D = 170 μA)	$V_{GS(th)}$	1.0	1.6	2.1	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.4	—	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	100	—	pF
Output Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	53	—	pF
Reverse Transfer Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 7.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 175 MHz)	G_{ps}	10	11.5	—	dB
Drain Efficiency (V_{DD} = 7.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 175 MHz)	η	50	55	—	%



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R1	15 Ω, 0805 Chip Resistor
C1, C5, C18	120 pF, 100 mil Chip Capacitor	R2	1.0 kΩ, 1/8 W Resistor
C2, C10, C12	0 to 20 pF, Trimmer Capacitor	R3	1.0 kΩ, 0805 Chip Resistor
C3	33 pF, 100 mil Chip Capacitor	R4	33 kΩ, 1/8 W Resistor
C4	68 pF, 100 mil Chip Capacitor	Z1	0.200″ x 0.080″ Microstrip
C6, C15	10 μF, 50 V Electrolytic Capacitor	Z2	0.755″ x 0.080″ Microstrip
C7, C16	1,200 pF, 100 mil Chip Capacitor	Z3	0.300″ x 0.080″ Microstrip
C8, C17	0.1 μF, 100 mil Chip Capacitor	Z4	0.065″ x 0.080″ Microstrip
C9	150 pF, 100 mil Chip Capacitor	Z5, Z6	0.260″ x 0.223″ Microstrip
C11	43 pF, 100 mil Chip Capacitor	Z7	0.095″ x 0.080″ Microstrip
C13	24 pF, 100 mil Chip Capacitor	Z8	0.418″ x 0.080″ Microstrip
C14	300 pF, 100 mil Chip Capacitor	Z9	1.057″ x 0.080″ Microstrip
L1, L3	12.5 nH, A04T, Coilcraft	Z10	0.120″ x 0.080″ Microstrip
L2	26 nH, 4 Turn, Coilcraft	Board	Glass Teflon®, 31 mils, 2 oz. Copper
L4	55.5 nH, 5 Turn, Coilcraft		
N1, N2	Type N Flange Mount		

Figure 1. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

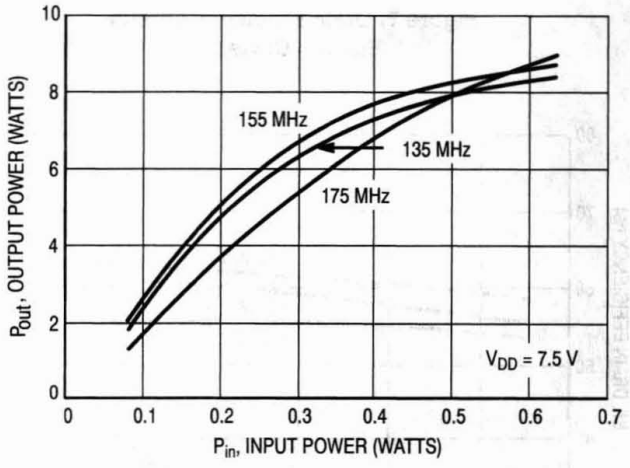


Figure 2. Output Power versus Input Power

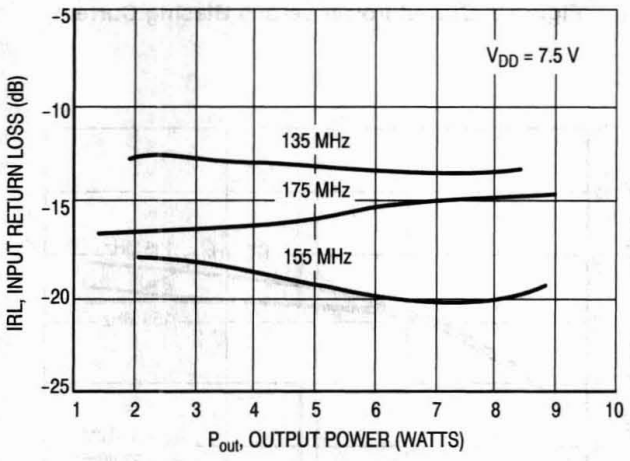


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 – 175 MHz

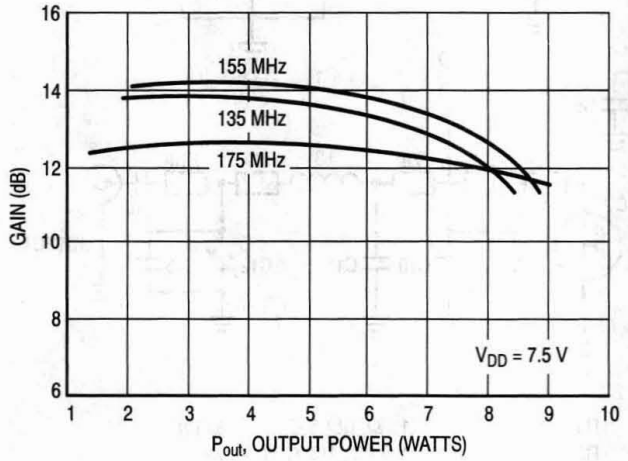


Figure 4. Gain versus Output Power

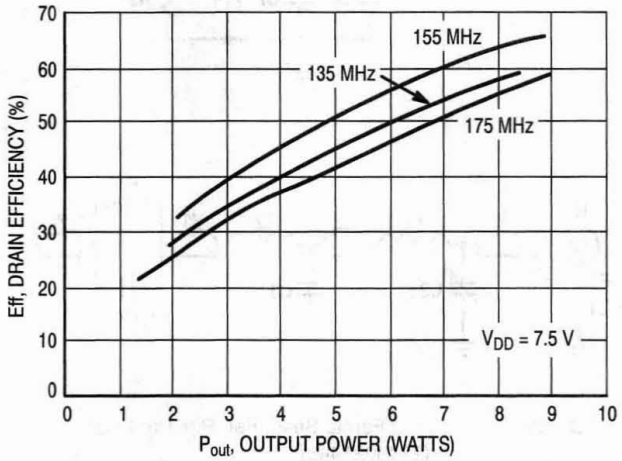


Figure 5. Drain Efficiency versus Output Power

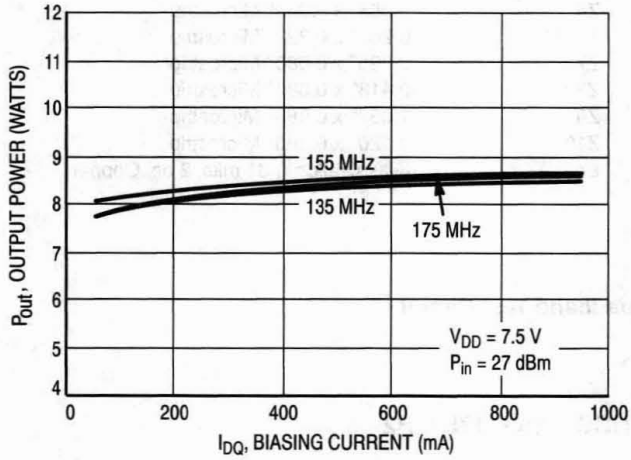


Figure 6. Output Power versus Biasing Current

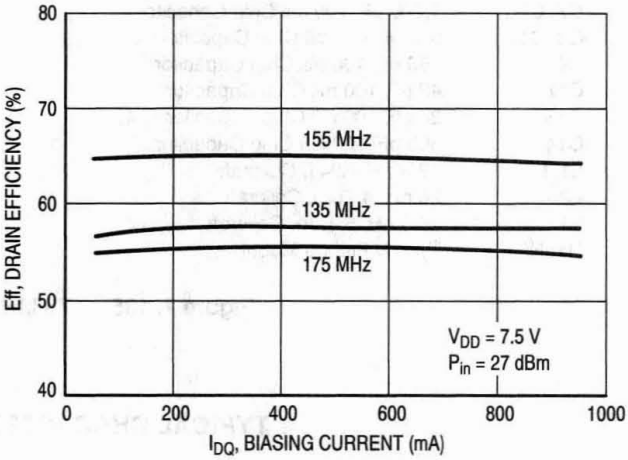


Figure 7. Drain Efficiency versus Biasing Current

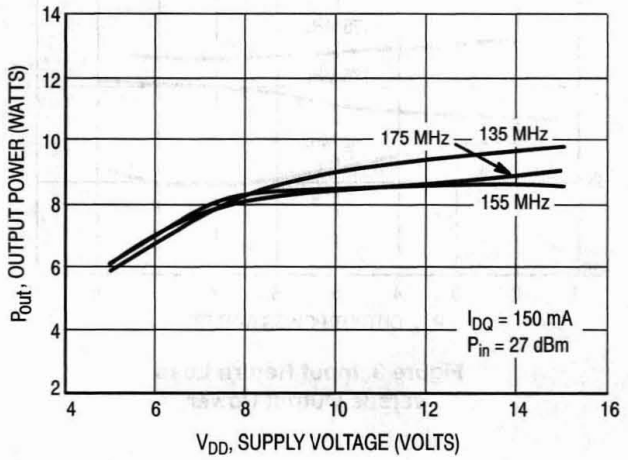


Figure 8. Output Power versus Supply Voltage

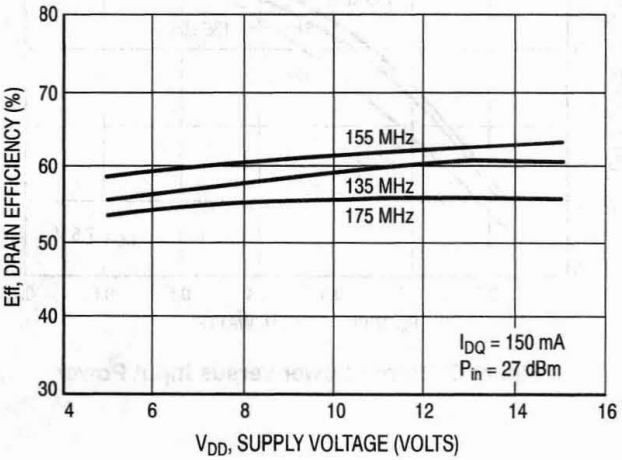
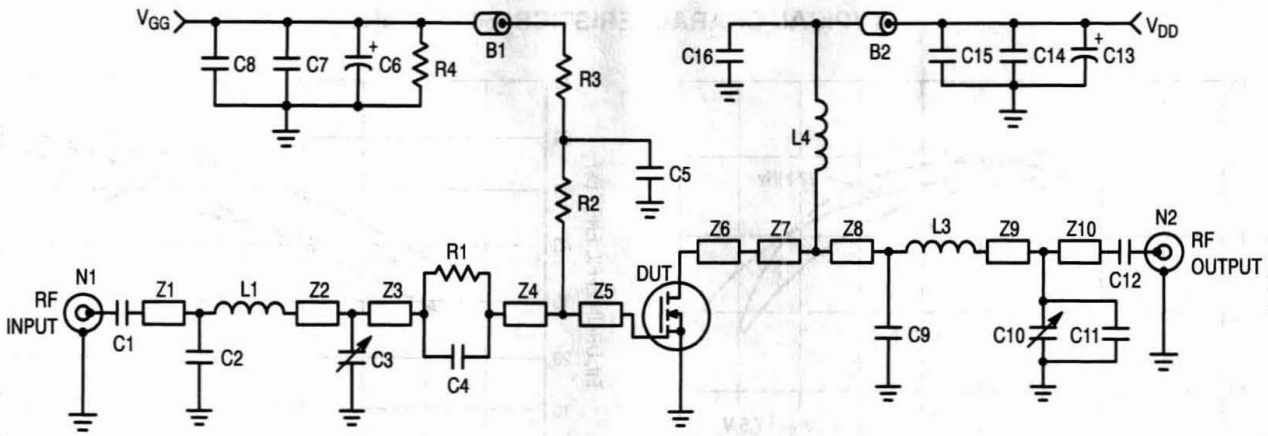


Figure 9. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	N1, N2	Type N Flange Mount
C1, C12	330 pF, 100 mil Chip Capacitor	R1	15 Ω, 0805 Chip Resistor
C2	43 pF, 100 mil Chip Capacitor	R2	51 Ω, 1/2 W Resistor
C3, C10	0 to 20 pF, Trimmer Capacitor	R3	100 Ω, 0805 Chip Resistor
C4	24 pF, 100 mil Chip Capacitor	R4	33 kΩ, 1/8 W Resistor
C5, C16	120 pF, 100 mil Chip Capacitor	Z1	0.136″ x 0.080″ Microstrip
C6, C13	10 μF, 50 V Electrolytic Capacitor	Z2	0.242″ x 0.080″ Microstrip
C7, C14	1,200 pF, 100 mil Chip Capacitor	Z3	1.032″ x 0.080″ Microstrip
C8, C15	0.1 μF, 100 mil Chip Capacitor	Z4	0.145″ x 0.080″ Microstrip
C9	380 pF, 100 mil Chip Capacitor	Z5, Z6	0.260″ x 0.223″ Microstrip
C11	75 pF, 100 mil Chip Capacitor	Z7	0.134″ x 0.080″ Microstrip
L1	82 nH, Coilcraft	Z8	0.490″ x 0.080″ Microstrip
L2	55.5 nH, 5 Turn, Coilcraft	Z9	0.872″ x 0.080″ Microstrip
L3	39 nH, 6 Turn, Coilcraft	Z10	0.206″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 10. 66 – 88 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 66 – 88 MHz

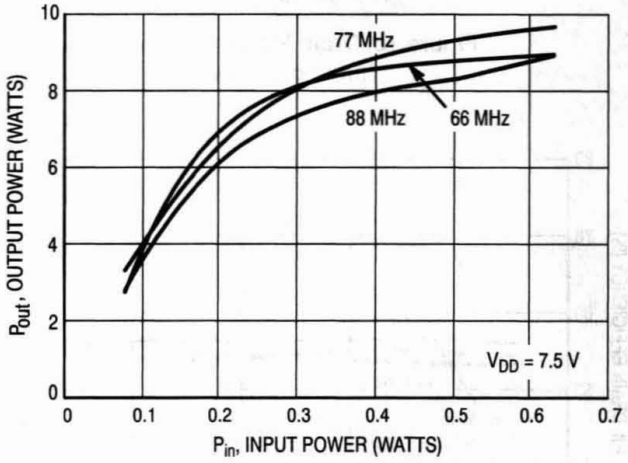


Figure 11. Output Power versus Input Power

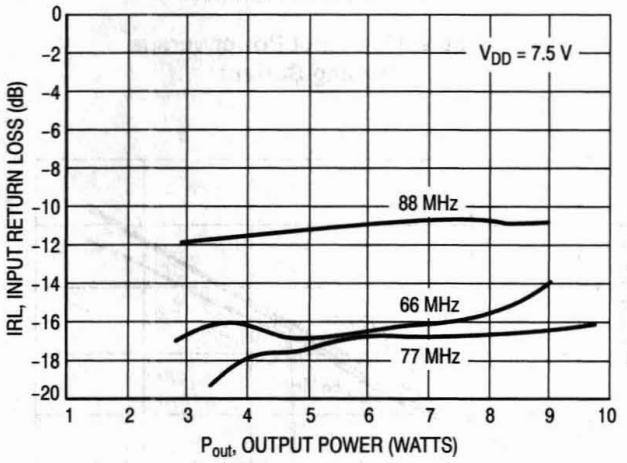


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 66 – 88 MHz

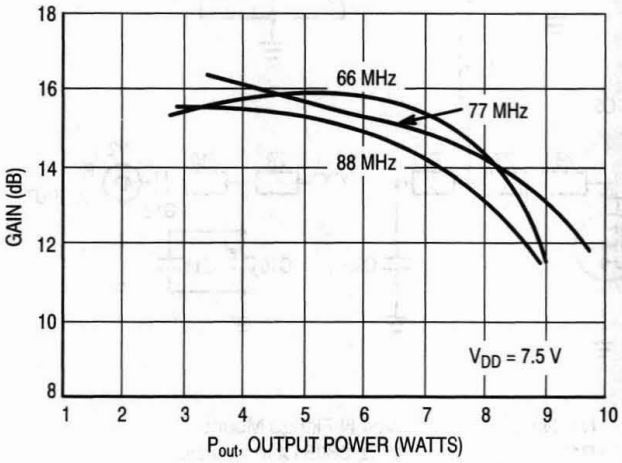


Figure 13. Gain versus Output Power

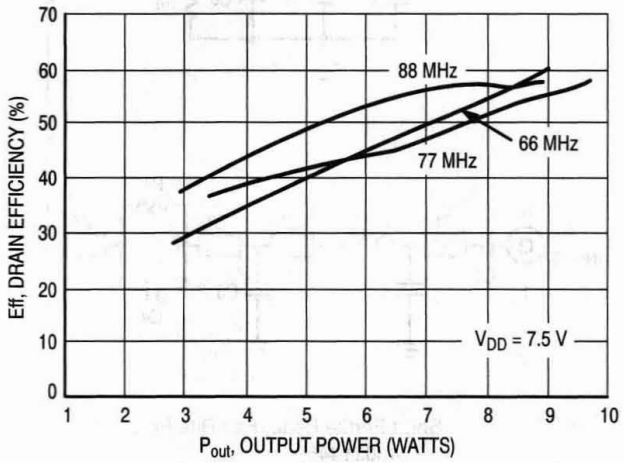


Figure 14. Drain Efficiency versus Output Power

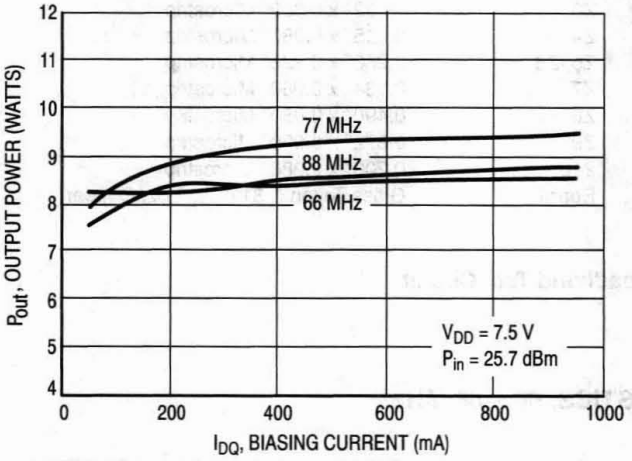


Figure 15. Output Power versus Biasing Current

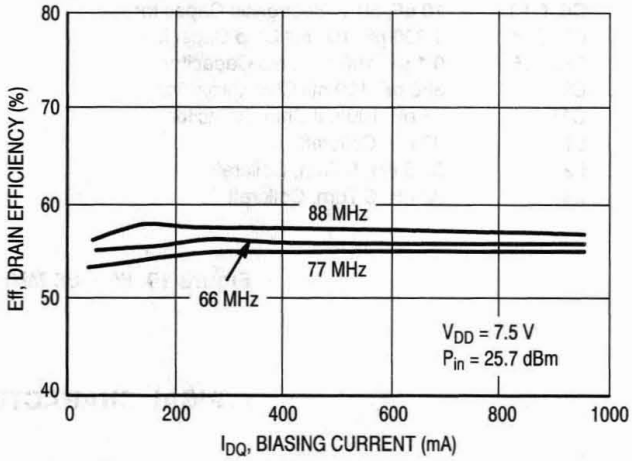


Figure 16. Drain Efficiency versus Biasing Current

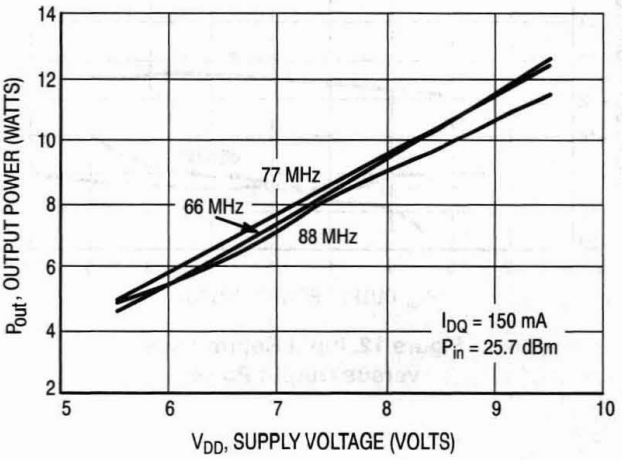


Figure 17. Output Power versus Supply Voltage

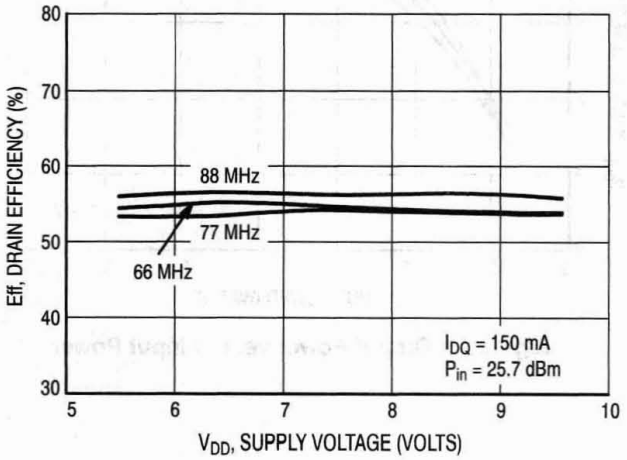
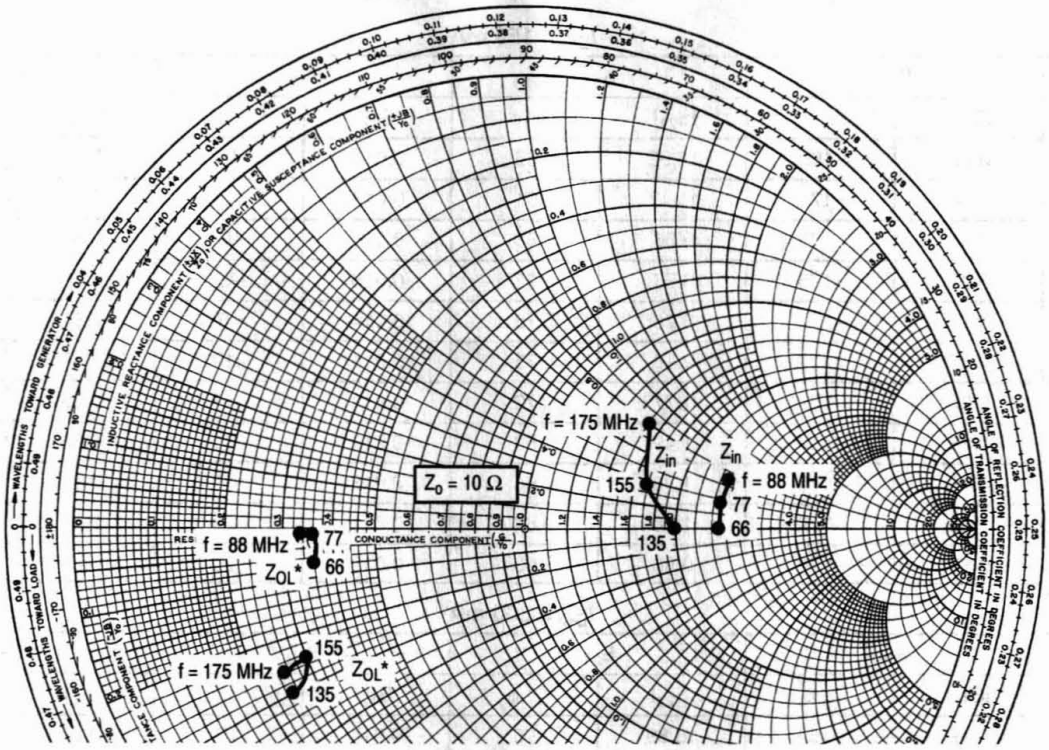


Figure 18. Drain Efficiency versus Supply Voltage



V_{DD} = 7.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	20.1 –j0.5	2.53 –j2.61
155	17.0 +j3.6	3.01 –j2.48
175	15.2 +j7.9	2.52 –j3.02

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 68 pF capacitor in series with gate. (See Figure 1).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 7.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
66	25.3 –j0.31	3.62 –j0.751
77	25.6 +j3.62	3.59 –j0.129
88	26.7 +j6.79	3.37 –j0.173

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 24 pF capacitor in series with gate. (See Figure 10).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

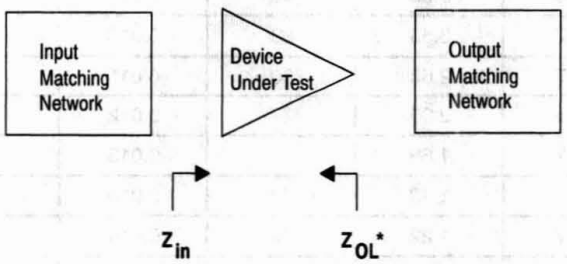


Figure 19. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 7.5 Vdc)

I_{DQ} = 150 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
30	0.88	–165	18.92	95	0.015	8	0.84	–169
50	0.88	–171	11.47	91	0.016	–5	0.84	–173
100	0.87	–175	5.66	85	0.016	–7	0.84	–176
150	0.87	–176	3.75	82	0.015	–5	0.85	–176
200	0.87	–177	2.78	78	0.014	–6	0.84	–176
250	0.87	–177	2.16	75	0.014	–10	0.85	–176
300	0.88	–177	1.77	72	0.012	–17	0.86	–176
350	0.88	–177	1.49	69	0.013	–11	0.86	–176
400	0.88	–177	1.26	66	0.013	–17	0.87	–175
450	0.88	–177	1.08	64	0.011	–20	0.87	–175
500	0.89	–176	0.96	63	0.012	–20	0.88	–175

I_{DQ} = 800 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
30	0.89	–166	18.89	95	0.014	10	0.85	–170
50	0.88	–172	11.44	91	0.015	8	0.84	–174
100	0.87	–175	5.65	86	0.016	–2	0.85	–176
150	0.87	–177	3.74	82	0.014	–8	0.84	–177
200	0.87	–177	2.78	78	0.013	–18	0.85	–177
250	0.88	–177	2.16	75	0.012	–11	0.85	–176
300	0.88	–177	1.77	73	0.015	–15	0.86	–176
350	0.88	–177	1.50	70	0.009	–7	0.87	–176
400	0.88	–177	1.26	67	0.012	–3	0.87	–176
450	0.88	–177	1.09	65	0.012	–18	0.87	–175
500	0.89	–177	0.97	64	0.009	–10	0.88	–175

I_{DQ} = 1.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
30	0.90	–168	17.89	95	0.013	2	0.86	–172
50	0.89	–173	10.76	91	0.013	3	0.86	–175
100	0.88	–176	5.32	86	0.014	–19	0.86	–177
150	0.88	–177	3.53	83	0.013	–6	0.86	–177
200	0.88	–177	2.63	80	0.011	–4	0.86	–177
250	0.88	–178	2.05	77	0.012	–14	0.86	–177
300	0.88	–177	1.69	75	0.013	–2	0.87	–177
350	0.89	–177	1.43	72	0.010	–9	0.87	–176
400	0.89	–177	1.22	70	0.014	–3	0.88	–176
450	0.89	–177	1.06	68	0.011	–8	0.88	–176
500	0.89	–177	0.94	67	0.011	–15	0.88	–176

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

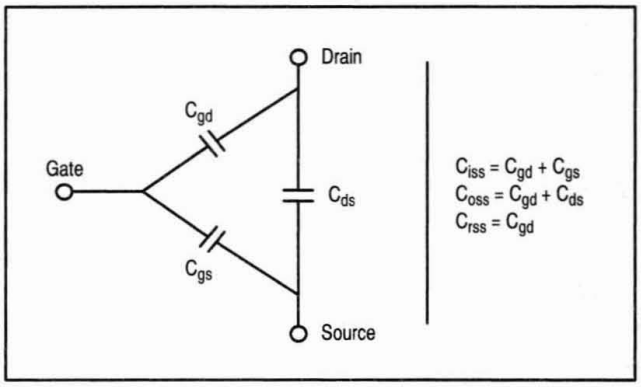
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD–1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two–port stability analysis with this device's S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

RF Power Field Effect Transistor

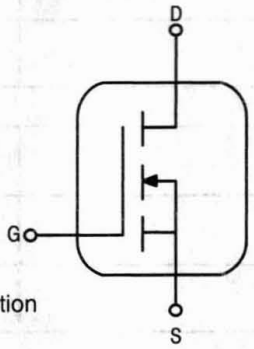
N–Channel Enhancement–Mode Lateral MOSFET

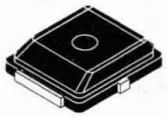
MRF1513T1

520 MHz, 3 W, 12.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

The MRF1513T1 is designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of this device make it ideal for large–signal, common source amplifier applications in 7.5 volt portable and 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
  Output Power — 3 Watts
  Power Gain — 11 dB
  Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 520 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- RF Power Plastic Surface Mount Package
- Available in Tape and Reel. T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.





CASE 466–02, STYLE 1
(PLD–1.5)

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	40	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	2	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	31.25 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

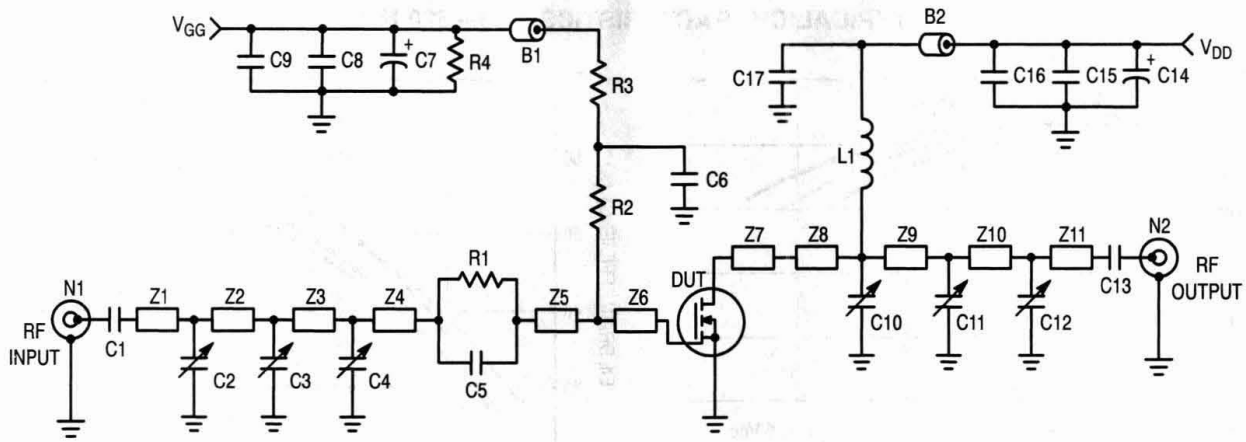
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4	°C/W

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current (V_{DS} = 40 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 12.5 Vdc, I_D = 60 μA)	$V_{GS(th)}$	1.0	1.7	2.1	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 500 mAdc)	$V_{DS(on)}$	—	0.65	—	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	33	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	16.5	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 3 Watts, I_{DQ} = 50 mA, f = 520 MHz)	G_{ps}	10	11	—	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 3 Watts, I_{DQ} = 50 mA, f = 520 MHz)	η	50	55	—	%



B1, B2	Short Ferrite Beads, Fair Rite Products #2743021446	R4	33 kΩ, 1/8 W Resistor
C1, C13	240 pF, 100 mil Chip Capacitors	Z1	0.236″ x 0.080″ Microstrip
C2, C3, C4, C10, C11, C12	0 to 20 pF Trimmer Capacitors	Z2	0.981″ x 0.080″ Microstrip
C5, C6, C17	120 pF, 100 mil Chip Capacitors	Z3	0.240″ x 0.080″ Microstrip
C7, C14	10 μF, 50 V Electrolytic Capacitors	Z4	0.098″ x 0.080″ Microstrip
C8, C15	1,200 pF, 100 mil Chip Capacitors	Z5	0.192″ x 0.080″ Microstrip
C9, C16	0.1 μF, 100 mil Chip Capacitors	Z6, Z7	0.260″ x 0.223″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z8	0.705″ x 0.080″ Microstrip
N1, N2	Type N Flange Mounts	Z9	0.342″ x 0.080″ Microstrip
R1, R3	15 Ω Chip Resistors (0805)	Z10	0.347″ x 0.080″ Microstrip
R2	1 kΩ, 1/8 W Resistor	Z11	0.846″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 1. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

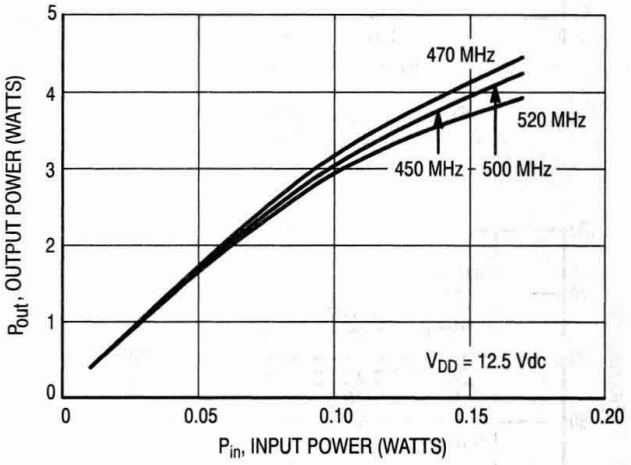


Figure 2. Output Power versus Input Power

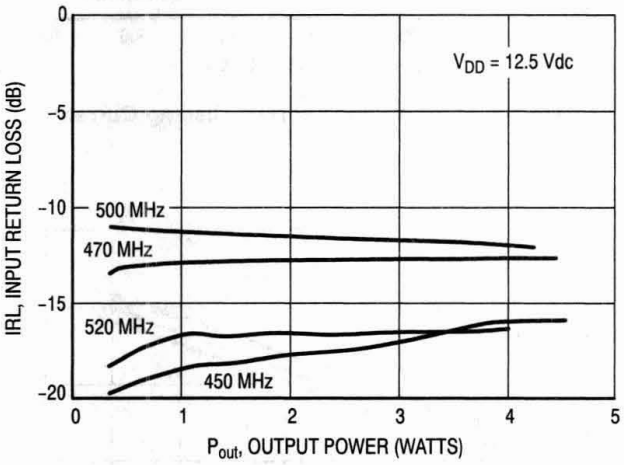


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 450 – 520 MHz

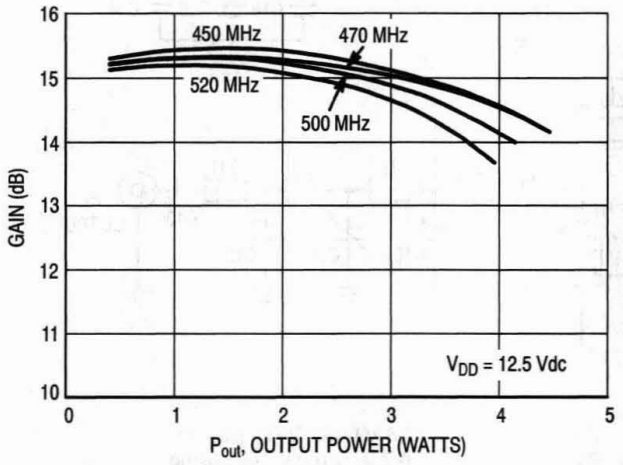


Figure 4. Gain versus Output Power

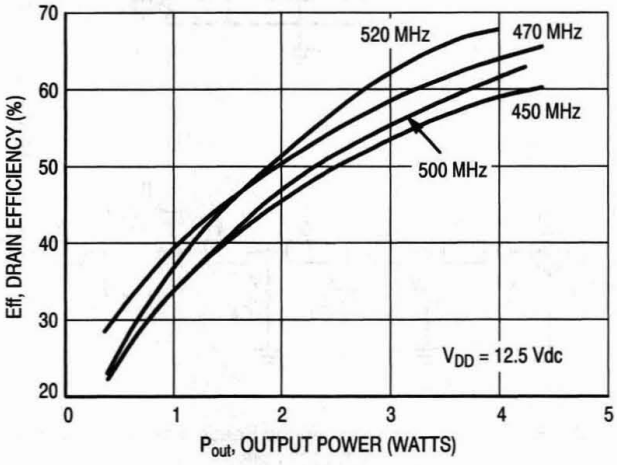


Figure 5. Drain Efficiency versus Output Power

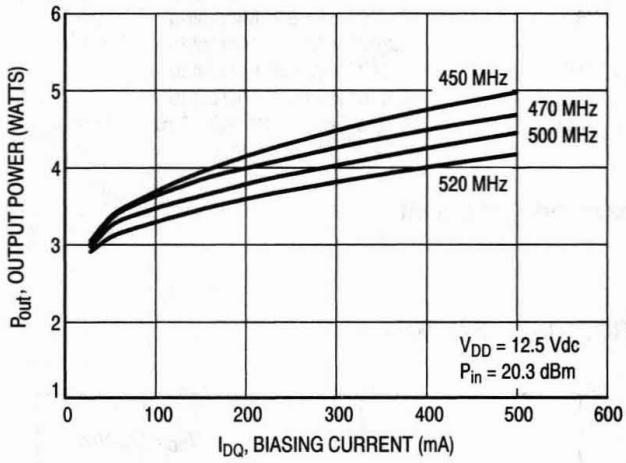


Figure 6. Output Power versus Biasing Current

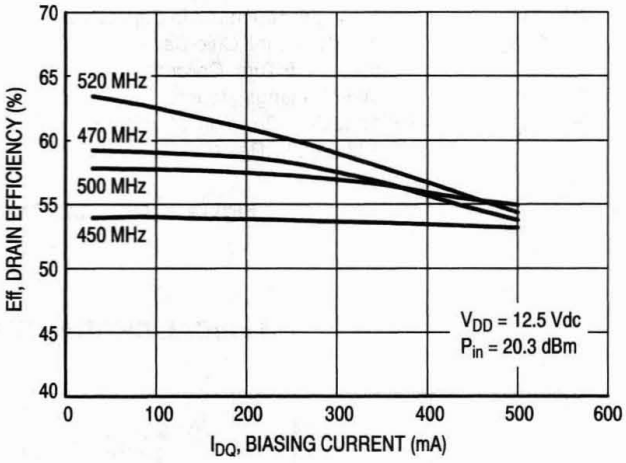


Figure 7. Drain Efficiency versus Biasing Current

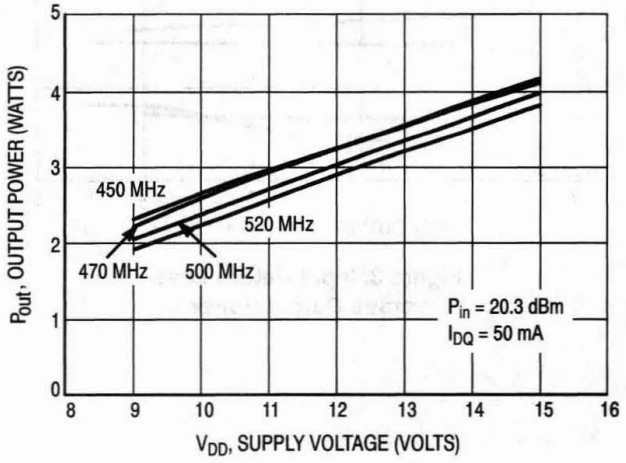


Figure 8. Output Power versus Supply Voltage

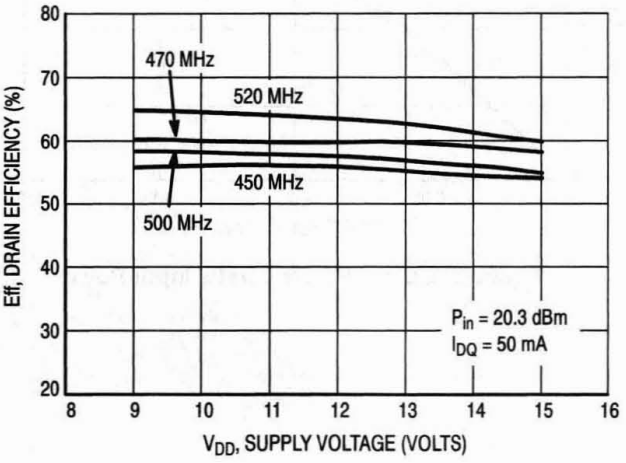
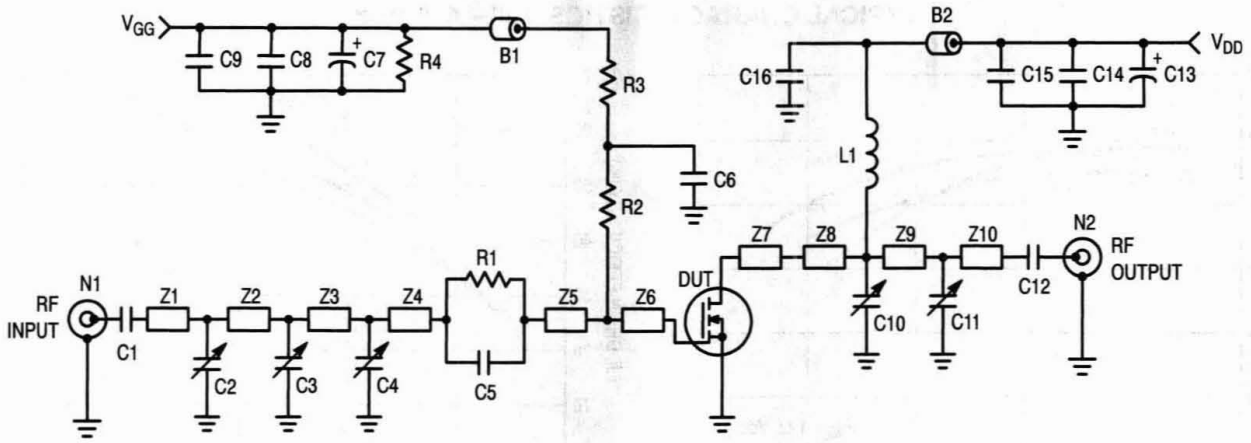


Figure 9. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Bead, Fair Rite Products #2743021446	R3	15 Ω Chip Resistor (0805)
C1, C12	330 pF, 100 mil Chip Capacitors	R4	33 kΩ, 1/8 W Resistor
C2, C3, C4, C10, C11	1 to 20 pF Trimmer Capacitors	Z1	0.253″ x 0.080″ Microstrip
C5, C6, C16	120 pF, 100 mil Chip Capacitors	Z2	0.958″ x 0.080″ Microstrip
C7, C13	10 μF, 50 V Electrolytic Capacitors	Z3	0.247″ x 0.080″ Microstrip
C8, C14	1,200 pF, 100 mil Chip Capacitors	Z4	0.193″ x 0.080″ Microstrip
C9, C15	0.1 μF, 100 mil Chip Capacitors	Z5	0.132″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z6, Z7	0.260″ x 0.223″ Microstrip
N1, N2	Type N Flange Mounts	Z8	0.494″ x 0.080″ Microstrip
R1	15 Ω Chip Resistor (0805)	Z9	0.941″ x 0.080″ Microstrip
R2	1 kΩ, 1/8 W Resistor	Z10	0.452″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 10. 400 – 470 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 400 – 470 MHz

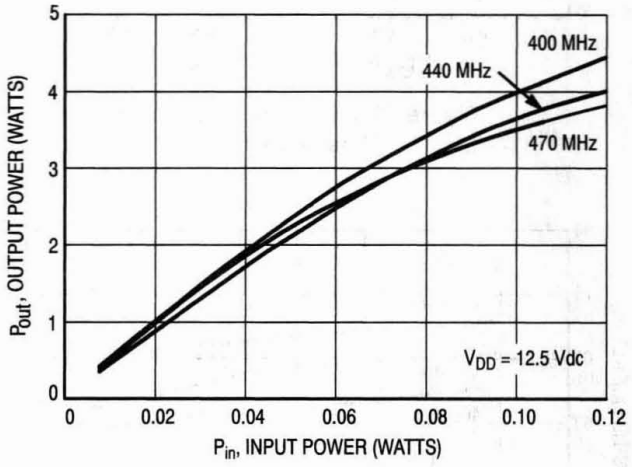


Figure 11. Output Power versus Input Power

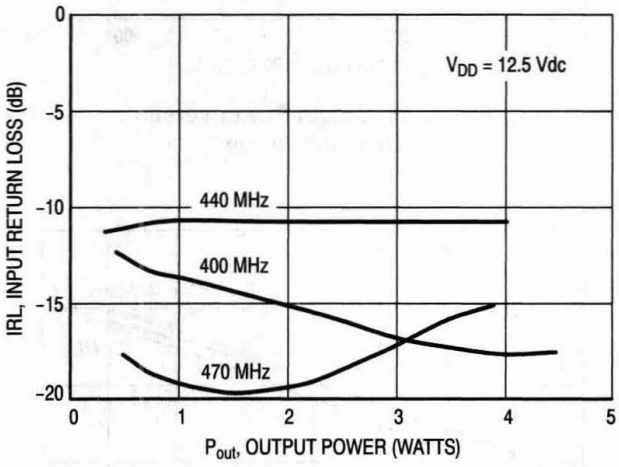


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 400 – 470 MHz

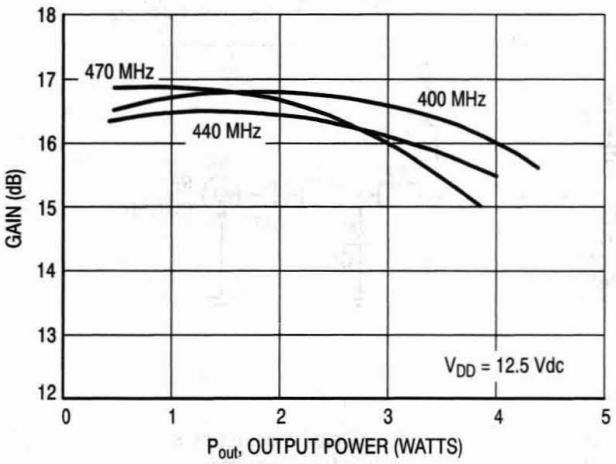


Figure 13. Gain versus Output Power

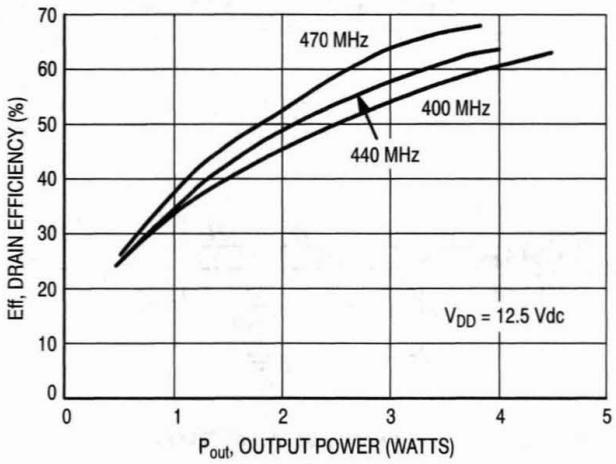


Figure 14. Drain Efficiency versus Output Power

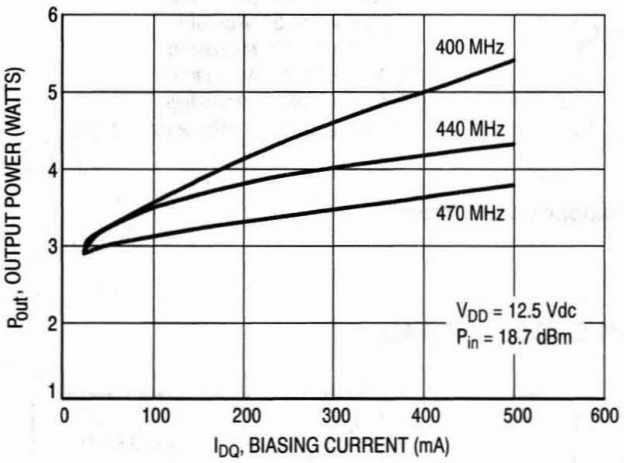


Figure 15. Output Power versus Biasing Current

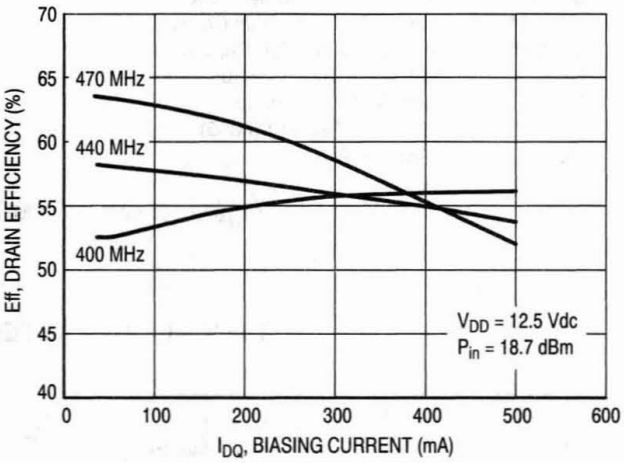


Figure 16. Drain Efficiency versus Biasing Current

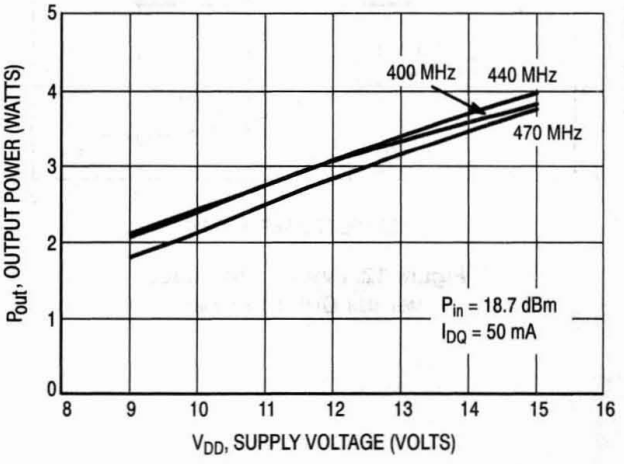


Figure 17. Output Power versus Supply Voltage

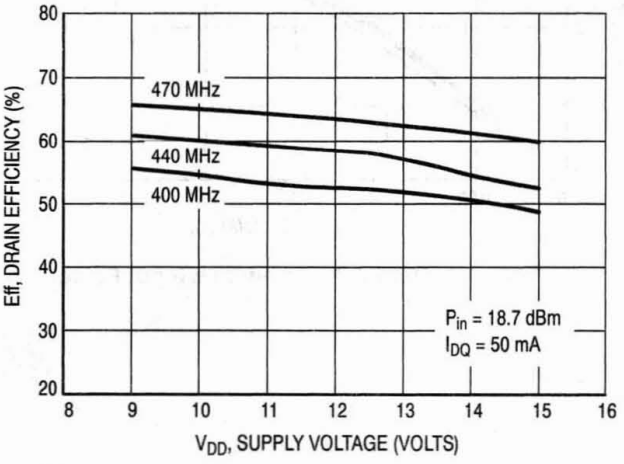
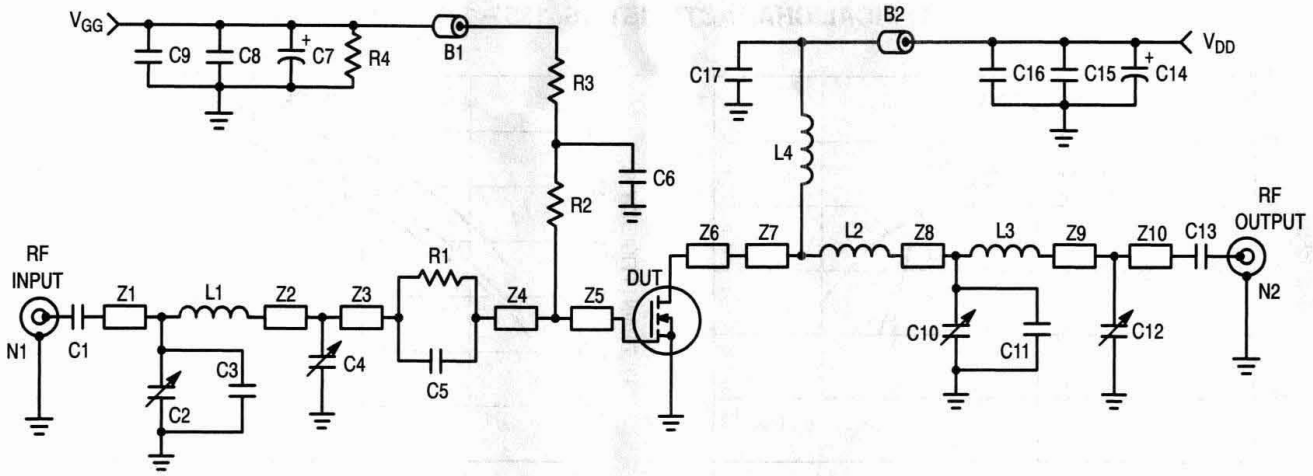


Figure 18. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Beads, Fair Rite Products #2743021446	L4	33 nH, 5 Turn, Coilcraft
C1, C13	330 pF, 100 mil Chip Capacitors	N1, N2	Type N Flange Mounts
C2, C4, C10, C12	0 to 20 pF Trimmer Capacitors	R1	15 Ω Chip Resistor (0805)
C3	12 pF, 100 mil Chip Capacitor	R2	56 Ω, 1/8 W Chip Resistor
C5	130 pF, 100 mil Chip Capacitor	R3	10 Ω, 1/8 W Chip Resistor
C6, C17	120 pF, 100 mil Chip Capacitors	R4	33 kΩ, 1/8 W Chip Resistor
C7, C14	10 µF, 50 V Electrolytic Capacitors	Z1	0.115″ x 0.080″ Microstrip
C8, C15	1,000 pF, 100 mil Chip Capacitors	Z2	0.230″ x 0.080″ Microstrip
C9, C16	0.1 µF, 100 mil Chip Capacitors	Z3	1.034″ x 0.080″ Microstrip
C11	18 pF, 100 mil Chip Capacitor	Z4	0.202″ x 0.080″ Microstrip
L1	26 nH, 4 Turn, Coilcraft	Z5, Z6	0.260″ x 0.223″ Microstrip
L2	8 nH, 3 Turn, Coilcraft	Z7	1.088″ x 0.080″ Microstrip
L3	55.5 nH, 5 Turn, Coilcraft	Z8	0.149″ x 0.080″ Microstrip
		Z9	0.171″ x 0.080″ Microstrip
		Z10	0.095″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 19. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

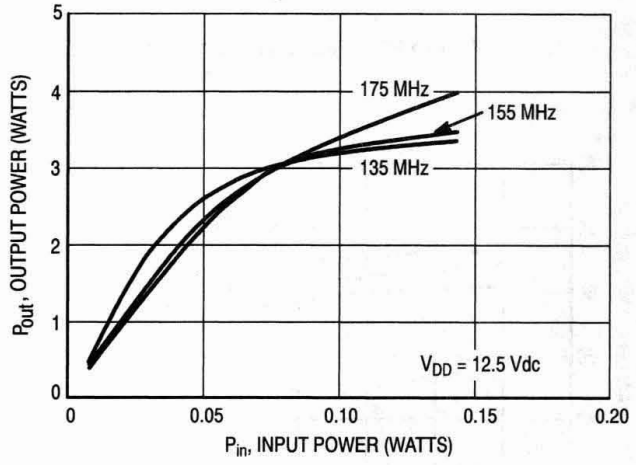


Figure 20. Output Power versus Input Power

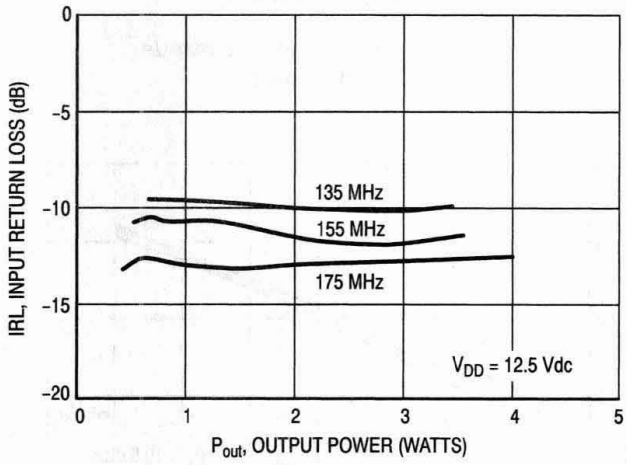


Figure 21. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 – 175 MHz

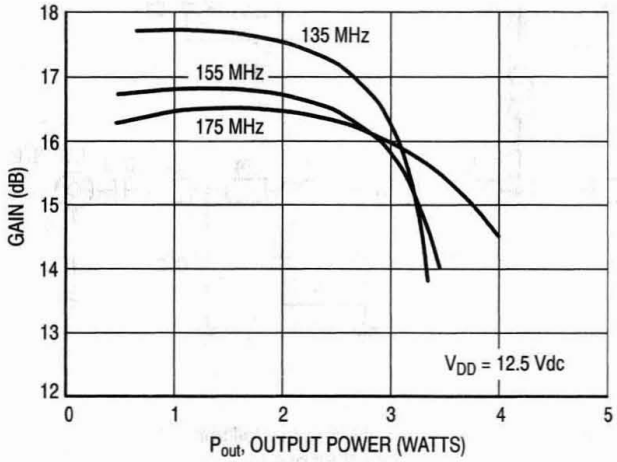


Figure 22. Gain versus Output Power

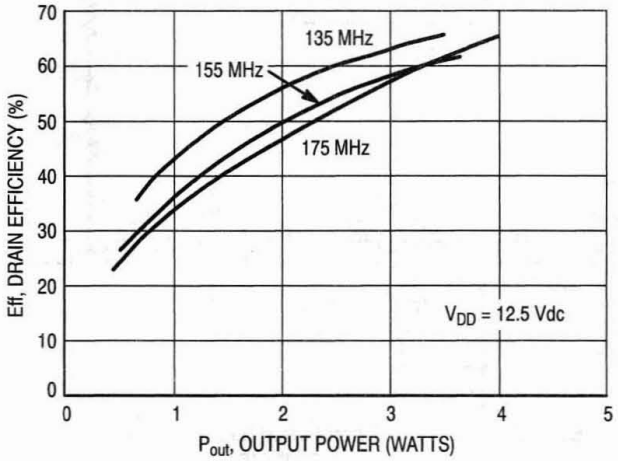


Figure 23. Drain Efficiency versus Output Power

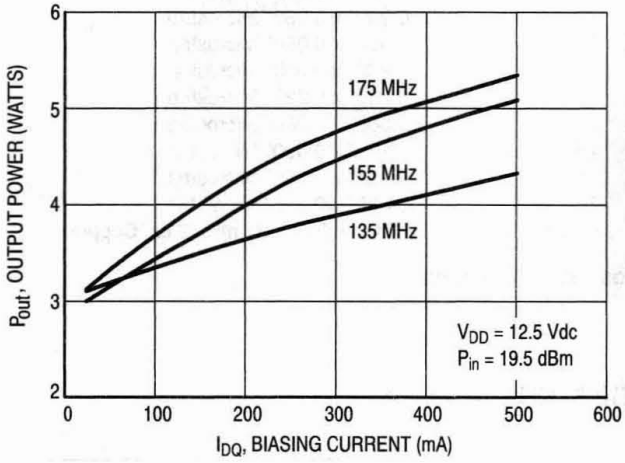


Figure 24. Output Power versus Biasing Current

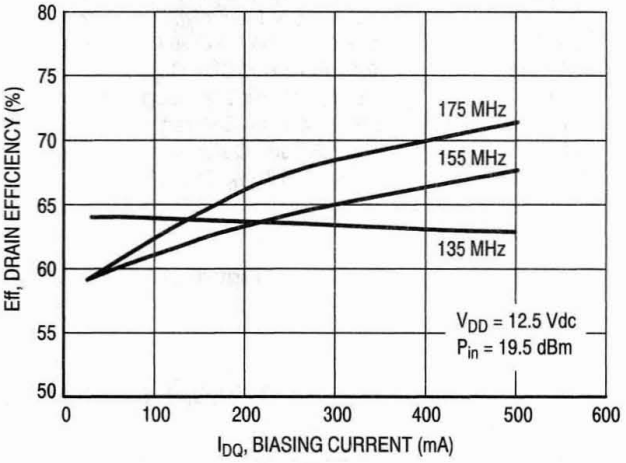


Figure 25. Drain Efficiency versus Biasing Current

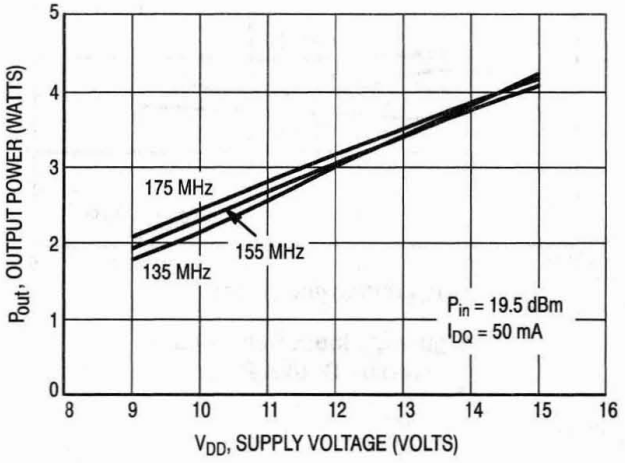


Figure 26. Output Power versus Supply Voltage

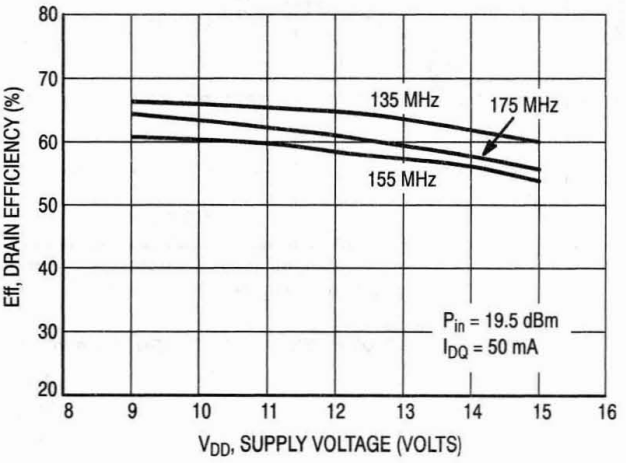
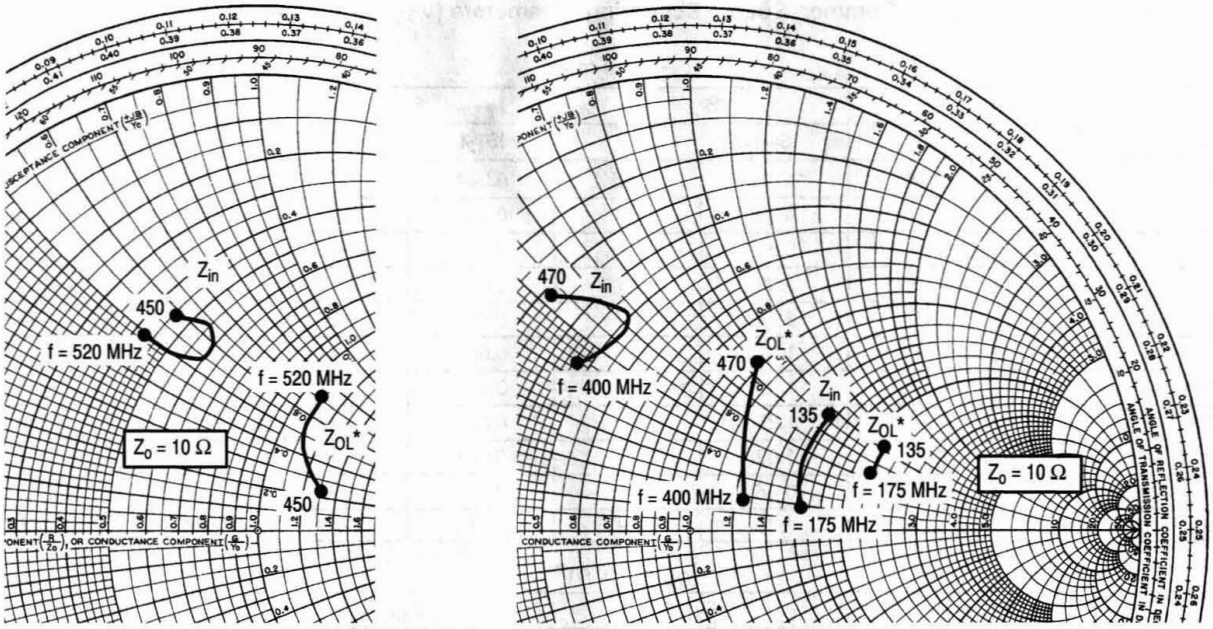


Figure 27. Drain Efficiency versus Supply Voltage



V_{DD} = 12.5 V, I_{DQ} = 50 mA, P_{out} = 3 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
450	4.64 +j5.82	13.11 +j2.15
470	5.42 +j6.34	12.16 +j3.26
500	5.96 +j5.45	11.03 +j5.42
520	4.28 +j4.94	10.99 +j7.18

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 120 pF capacitor in series with gate. (See Figure 1).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 12.5 V, I_{DQ} = 50 mA, P_{out} = 3 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
400	4.72 +j4.38	12.57 +j1.88
440	4.88 +j6.34	11.21 +j5.87
470	3.22 +j5.24	9.82 +j8.63

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 130 pF capacitor in series with gate. (See Figure 10).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 12.5 V, I_{DQ} = 50 mA, P_{out} = 3 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	16.55 +j1.82	22.01 +j10.32
155	15.59 +j5.38	22.03 +j8.07
175	15.55 +j9.43	22.08 +j6.85

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 130 pF capacitor in series with gate. (See Figure 19).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

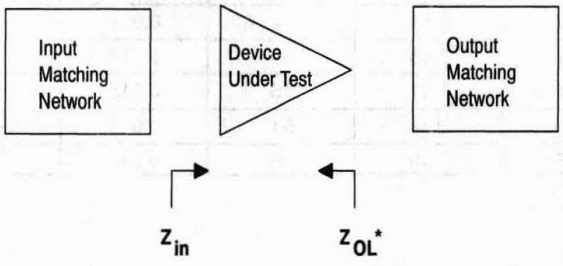


Figure 28. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 12.5 Vdc)

I_{DQ} = 50 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.93	–94	22.09	125	0.044	33	0.77	–81
100	0.81	–131	12.78	101	0.052	6	0.61	–115
200	0.76	–153	6.31	81	0.047	–10	0.59	–135
300	0.76	–160	3.92	69	0.044	–19	0.64	–142
400	0.77	–164	2.74	60	0.040	–26	0.70	–147
500	0.79	–167	1.99	54	0.036	–31	0.75	–151
600	0.80	–169	1.55	48	0.034	–37	0.80	–155
700	0.81	–171	1.25	44	0.028	–40	0.82	–158
800	0.82	–172	1.02	38	0.027	–42	0.86	–161
900	0.83	–173	0.85	35	0.017	–42	0.88	–163
1000	0.84	–175	0.70	29	0.018	–49	0.91	–166

I_{DQ} = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.84	–127	32.57	112	0.025	17	0.64	–130
100	0.80	–152	17.23	97	0.025	13	0.64	–153
200	0.78	–166	8.62	85	0.025	–9	0.65	–163
300	0.78	–171	5.58	79	0.023	–9	0.67	–166
400	0.78	–173	4.08	72	0.022	–9	0.69	–166
500	0.78	–175	3.14	68	0.020	–10	0.71	–167
600	0.79	–176	2.55	63	0.022	–15	0.74	–168
700	0.79	–177	2.14	60	0.019	–20	0.76	–168
800	0.80	–178	1.80	54	0.018	–31	0.79	–170
900	0.81	–178	1.54	51	0.015	–25	0.80	–170
1000	0.82	–179	1.31	46	0.012	–36	0.81	–172

I_{DQ} = 1 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.84	–129	32.57	111	0.023	24	0.61	–137
100	0.80	–153	17.04	97	0.024	13	0.64	–156
200	0.78	–167	8.52	85	0.023	5	0.65	–165
300	0.77	–172	5.53	79	0.020	–7	0.67	–167
400	0.77	–174	4.06	73	0.020	–11	0.69	–167
500	0.78	–175	3.13	69	0.021	–9	0.72	–167
600	0.78	–177	2.54	64	0.017	–26	0.74	–168
700	0.78	–177	2.13	60	0.017	–14	0.75	–168
800	0.79	–178	1.81	55	0.015	–23	0.78	–170
900	0.80	–178	1.54	51	0.013	–31	0.79	–170
1000	0.80	–179	1.30	46	0.011	–17	0.80	–172

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

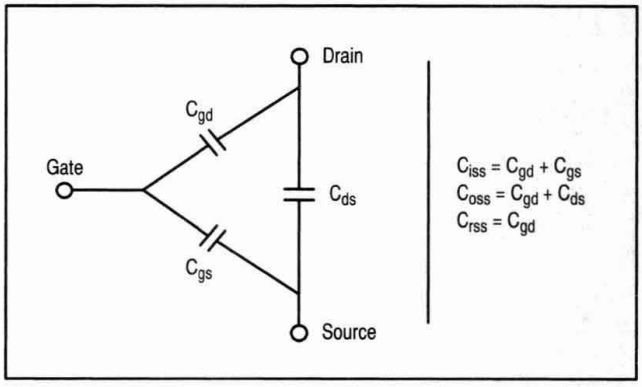
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD–1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two–port stability analysis with this device's S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

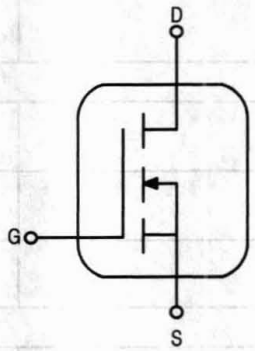
RF Power Field Effect Transistor

N–Channel Enhancement–Mode Lateral MOSFETs

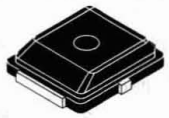
MRF1517T1

The MRF1517T1 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 7.5 volt portable FM equipment.

- Specified Performance @ 520 MHz, 7.5 Volts
  Output Power — 8 Watts
  Power Gain — 11 dB
  Efficiency — 55%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Excellent Thermal Stability
- Capable of Handling 20:1 VSWR, @ 9.5 Vdc, 520 MHz, 2 dB Overdrive
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- RF Power Plastic Surface Mount Package
- Available in Tape and Reel.
  T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.



520 MHz, 8 W, 7.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET



CASE 466–02, STYLE 1
(PLD–1.5)

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage (1)	V_{DSS}	25	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ T_C = 25°C (2) Derate above 25°C	P_D	62.5 0.50	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

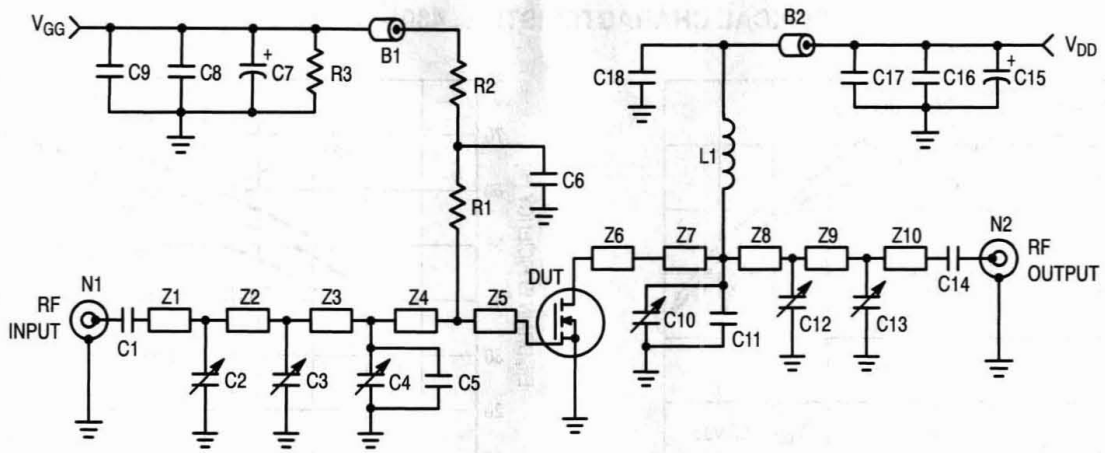
(1) Not designed for 12.5 volt applications.

(2) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current (V_{DS} = 35 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 7.5 Vdc, I_D = 120 μAdc)	$V_{GS(th)}$	1.0	1.7	2.1	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.5	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	0.9	—	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	66	—	pF
Output Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	38	—	pF
Reverse Transfer Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	6	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 7.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 520 MHz)	G_{ps}	10	11	—	dB
Drain Efficiency (V_{DD} = 7.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 520 MHz)	η	50	55	—	%



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R1	15 Ω, 0805 Chip Resistor
C1	300 pF, 100 mil Chip Capacitor	R2	1.0 kΩ, 1/8 W Resistor
C2, C3, C4, C10, C12, C13	0 to 20 pF, Trimmer Capacitor	R3	33 kΩ, 1/2 W Resistor
C5, C11	43 pF, 100 mil Chip Capacitor	Z1	0.315″ x 0.080″ Microstrip
C6, C18	120 pF, 100 mil Chip Capacitor	Z2	1.415″ x 0.080″ Microstrip
C7, C15	10 μF, 50 V Electrolytic Capacitor	Z3	0.322″ x 0.080″ Microstrip
C8, C16	0.1 μF, 100 mil Chip Capacitor	Z4	0.022″ x 0.080″ Microstrip
C9, C17	1,000 pF, 100 mil Chip Capacitor	Z5, Z6	0.260″ x 0.223″ Microstrip
C14	330 pF, 100 mil Chip Capacitor	Z7	0.050″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z8	0.625″ x 0.080″ Microstrip
N1, N2	Type N Flange Mount	Z9	0.800″ x 0.080″ Microstrip
		Z10	0.589″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 1. 480 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 480 – 520 MHz

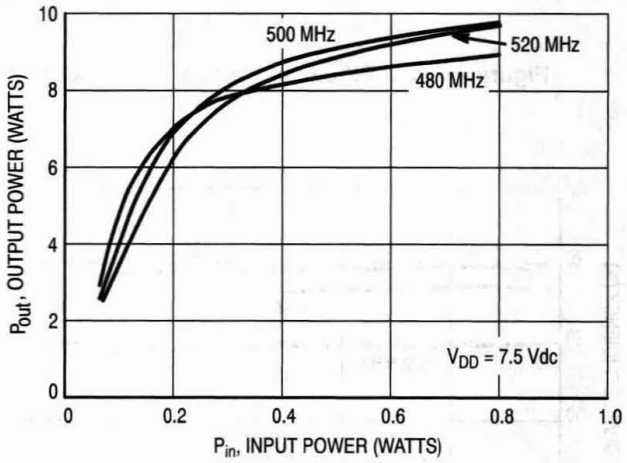


Figure 2. Output Power versus Input Power

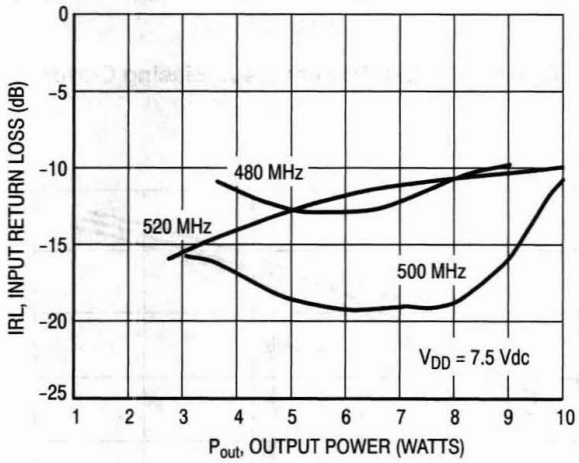


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 480 – 520 MHz

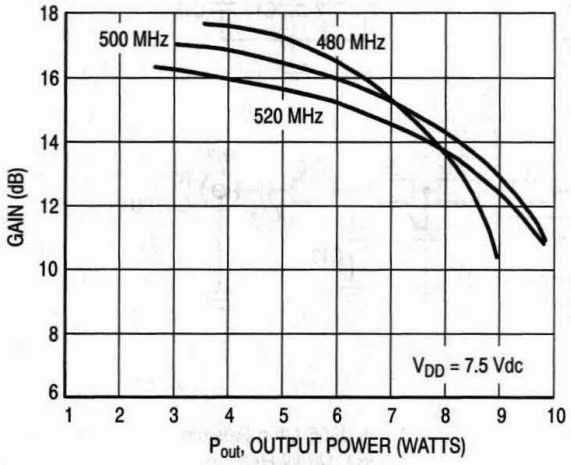


Figure 4. Gain versus Output Power

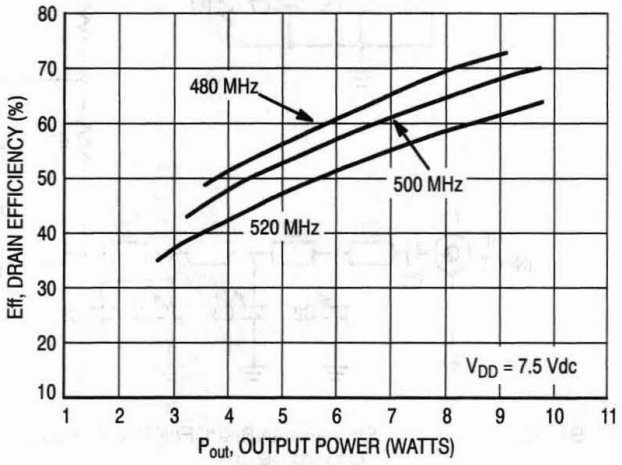


Figure 5. Drain Efficiency versus Output Power

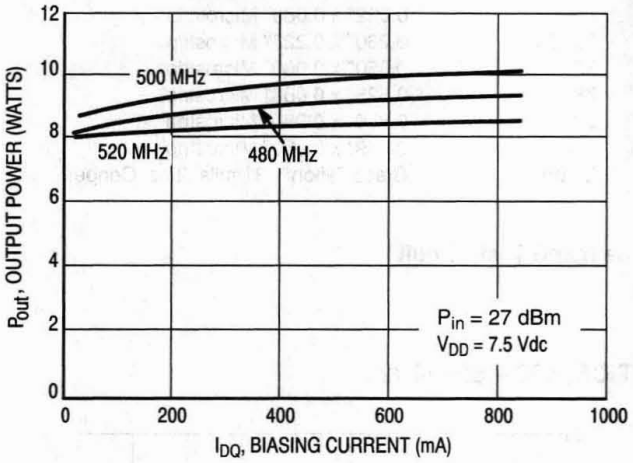


Figure 6. Output Power versus Biasing Current

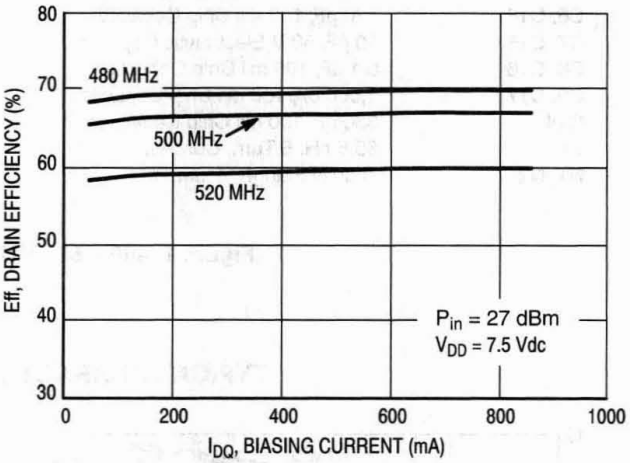


Figure 7. Drain Efficiency versus Biasing Current

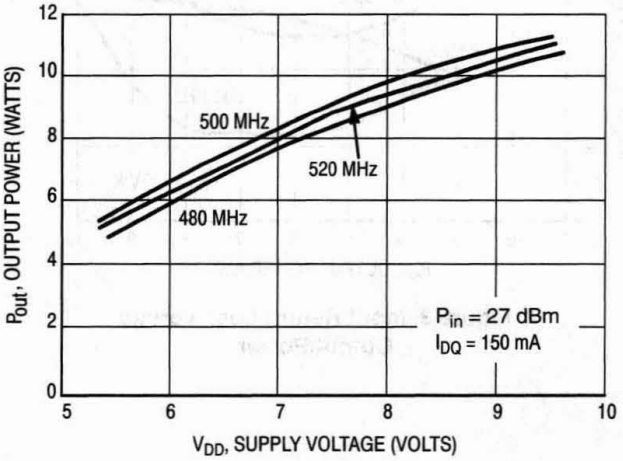


Figure 8. Output Power versus Supply Voltage

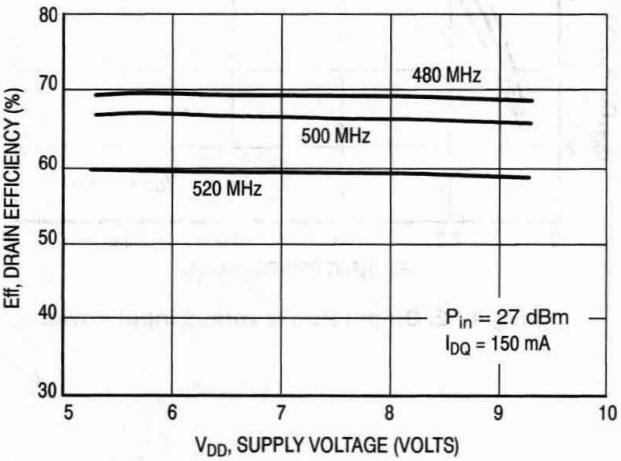
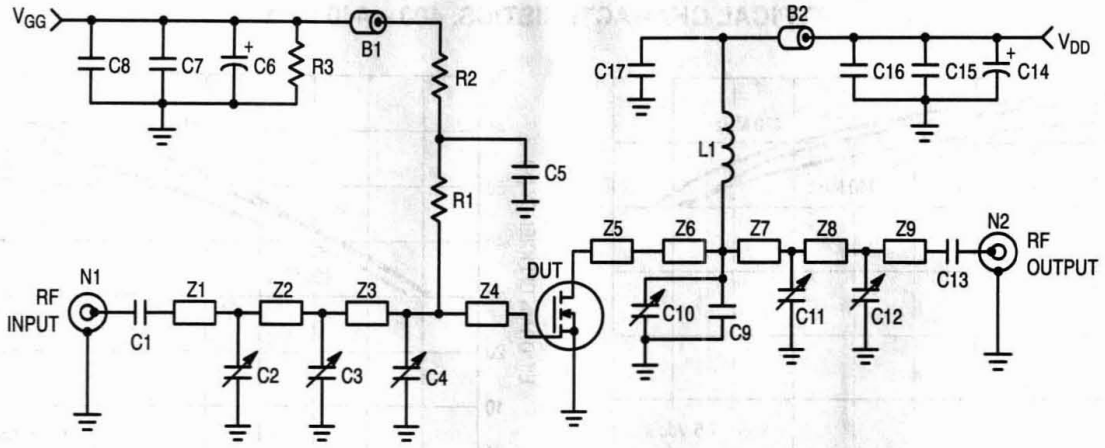


Figure 9. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R1	12 Ω, 0805 Chip Resistor
C1, C13	300 pF, 100 mil Chip Capacitor	R2	1.0 kΩ, 1/8 W Resistor
C2, C3, C4, C10, C11, C12	0 to 20 pF, Trimmer Capacitor	R3	33 kΩ, 1/2 W Resistor
C5, C17	130 pF, 100 mil Chip Capacitor	Z1	0.617″ x 0.080″ Microstrip
C6, C14	10 µF, 50 V Electrolytic Capacitor	Z2	0.723″ x 0.080″ Microstrip
C7, C15	0.1 µF, 100 mil Chip Capacitor	Z3	0.513″ x 0.080″ Microstrip
C8, C16	1,000 pF, 100 mil Chip Capacitor	Z4, Z5	0.260″ x 0.223″ Microstrip
C9	33 pF, 100 mil Chip Capacitor	Z6	0.048″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z7	0.577″ x 0.080″ Microstrip
N1, N2	Type N Flange Mount	Z8	1.135″ x 0.080″ Microstrip
		Z9	0.076″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 10. 400 – 440 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 400 – 440 MHz

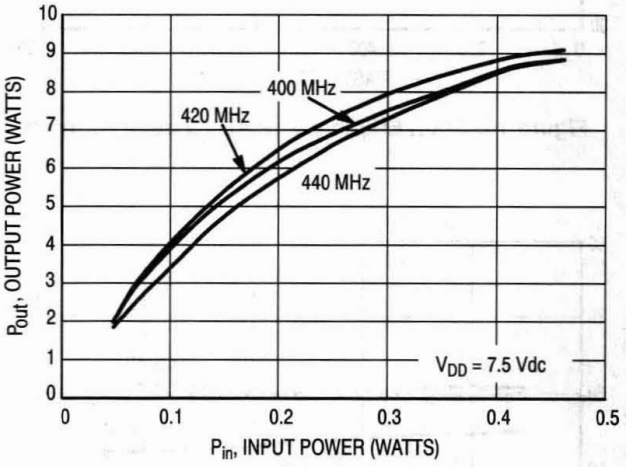


Figure 11. Output Power versus Input Power

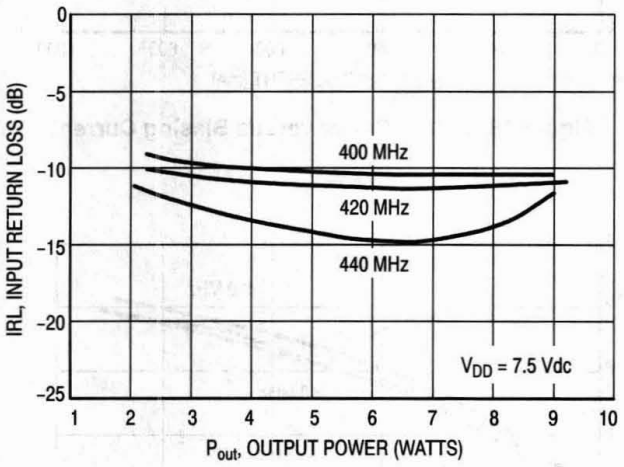


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 400 – 440 MHz

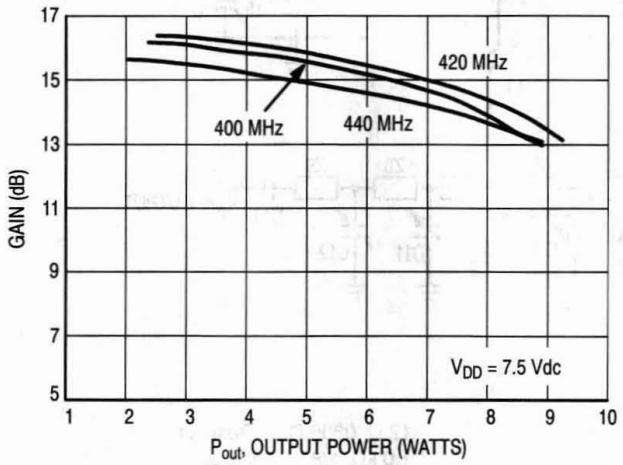


Figure 13. Gain versus Output Power

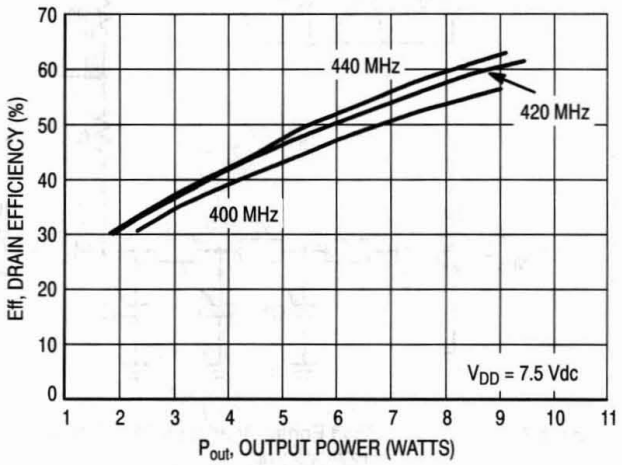


Figure 14. Drain Efficiency versus Output Power

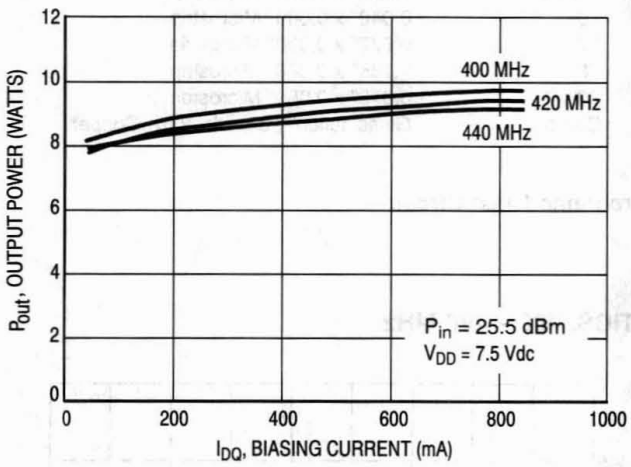


Figure 15. Output Power versus Biasing Current

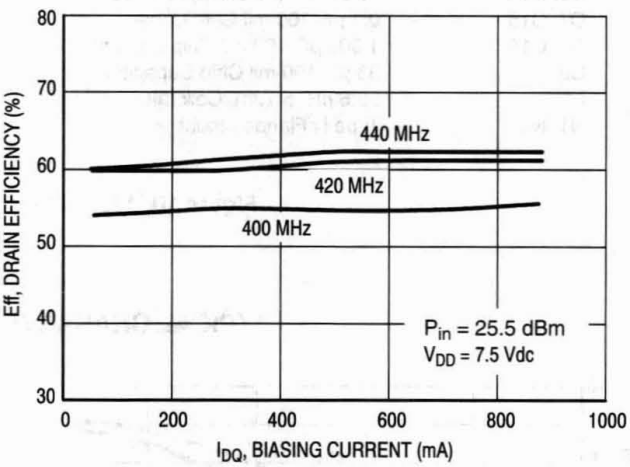


Figure 16. Drain Efficiency versus Biasing Current

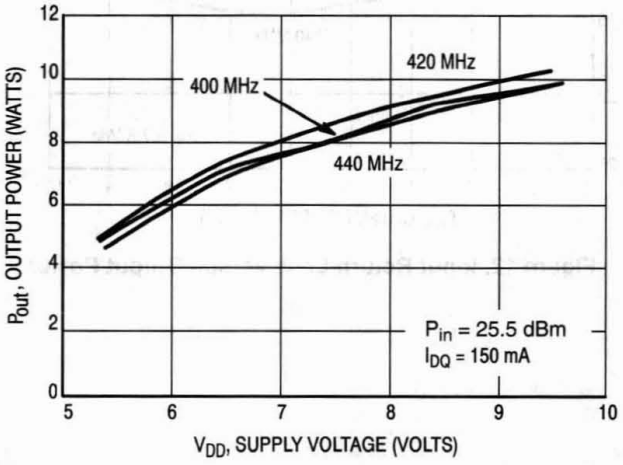


Figure 17. Output Power versus Supply Voltage

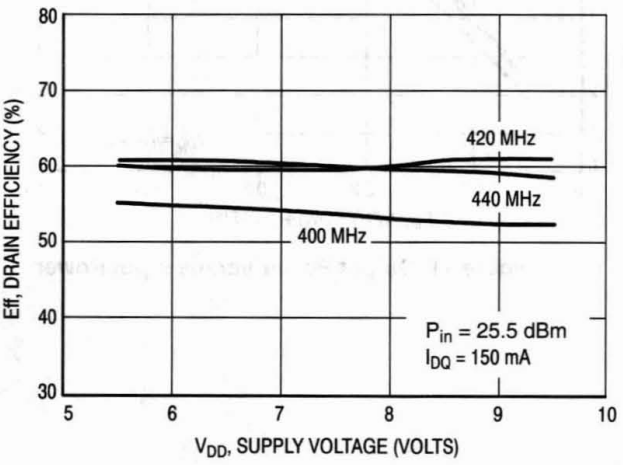
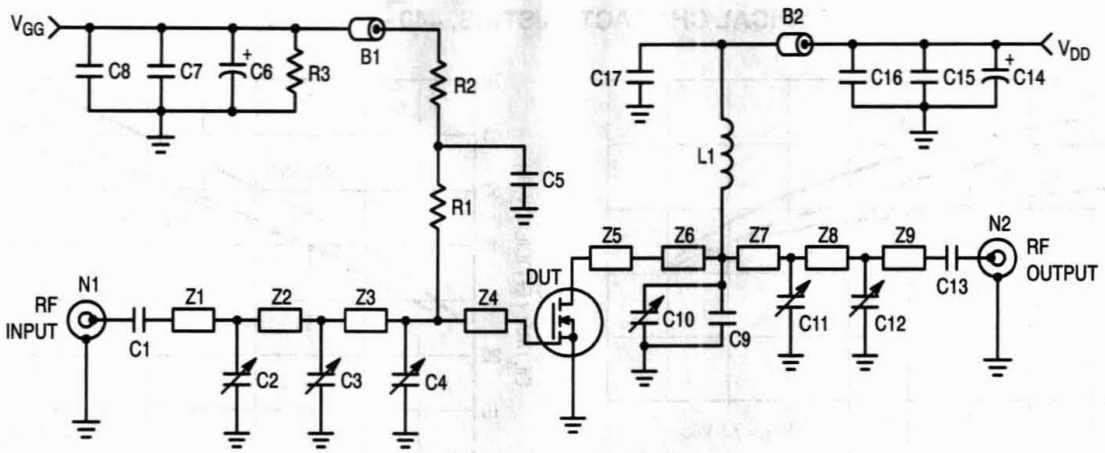


Figure 18. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R1	15 Ω, 0805 Chip Resistor
C1	240 pF, 100 mil Chip Capacitor	R2	1.0 kΩ, 1/8 W Resistor
C2, C3, C4, C10, C11, C12	0 to 20 pF, Trimmer Capacitor	R3	33 kΩ, 1/2 W Resistor
C5, C17	130 pF, 100 mil Chip Capacitor	Z1	0.471″ x 0.080″ Microstrip
C6, C14	10 mF, 50 V Electrolytic Capacitor	Z2	1.082″ x 0.080″ Microstrip
C7, C15	0.1 mF, 100 mil Chip Capacitor	Z3	0.372″ x 0.080″ Microstrip
C8, C16	1,000 pF, 100 mil Chip Capacitor	Z4, Z5	0.260″ x 0.223″ Microstrip
C9	39 pF, 100 mil Chip Capacitor	Z6	0.050″ x 0.080″ Microstrip
C13	330 pF, 100 mil Chip Capacitor	Z7	0.551″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z8	0.825″ x 0.080″ Microstrip
N1, N2	Type N Flange Mount	Z9	0.489″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 19. 440 – 480 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 440 – 480 MHz

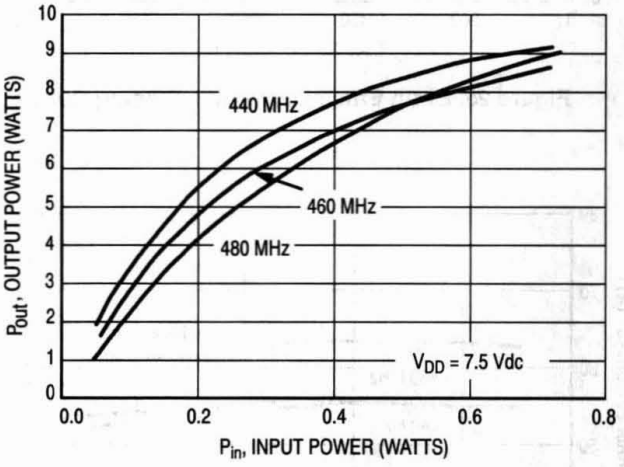


Figure 20. Output Power versus Input Power

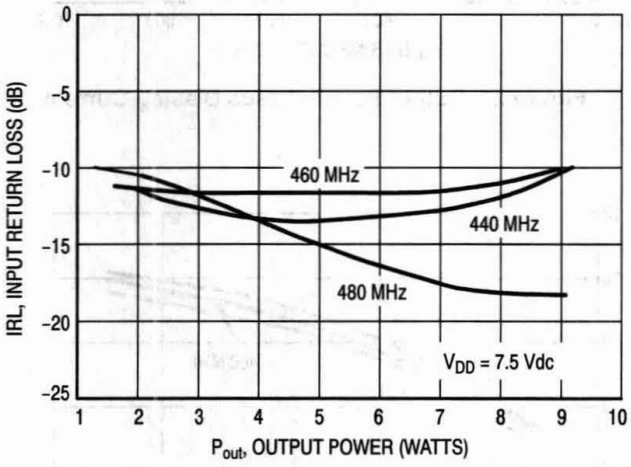


Figure 21. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 440 – 480 MHz

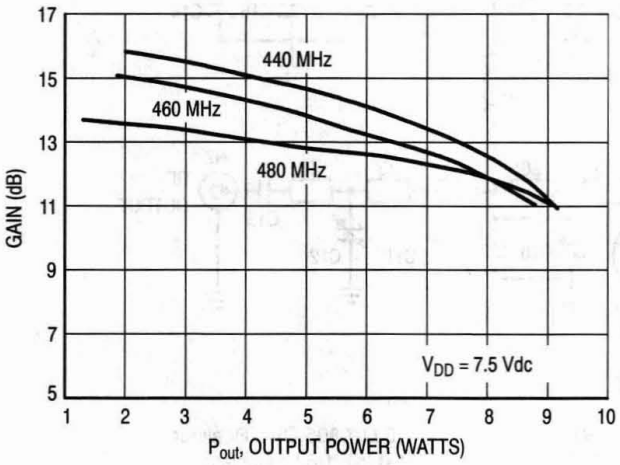


Figure 22. Gain versus Output Power

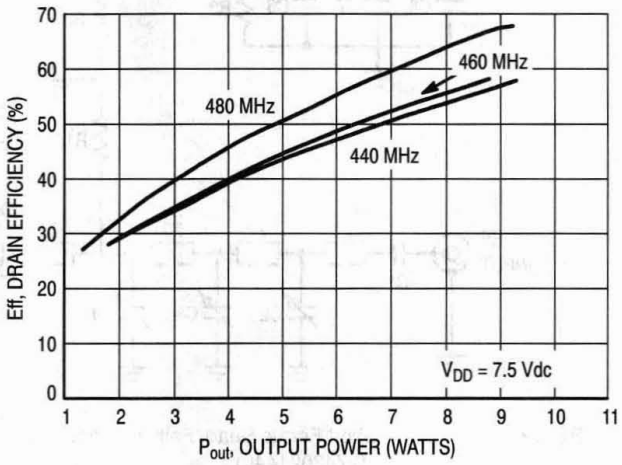


Figure 23. Drain Efficiency versus Output Power

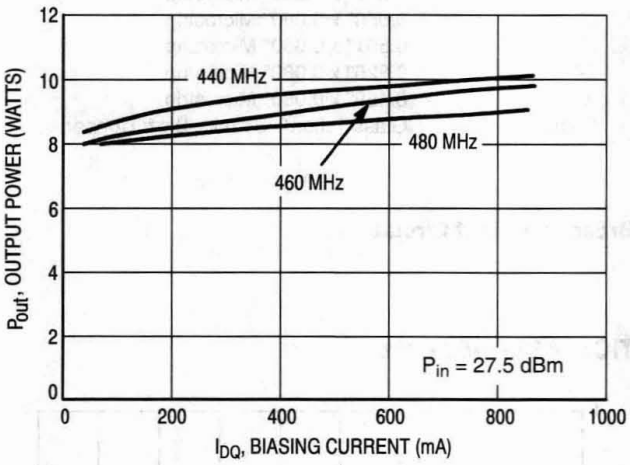


Figure 24. Output Power versus Biasing Current

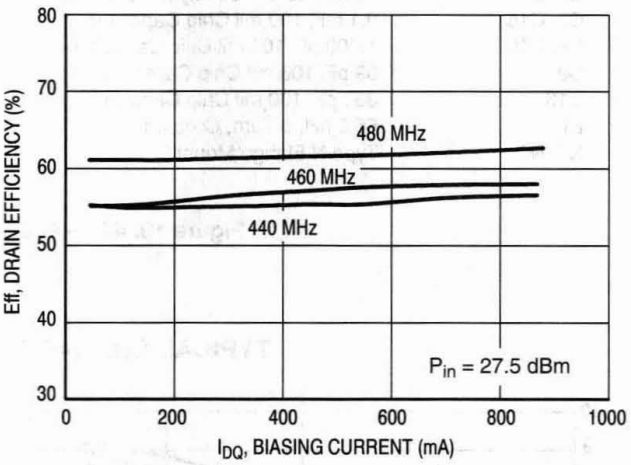


Figure 25. Drain Efficiency versus Biasing Current

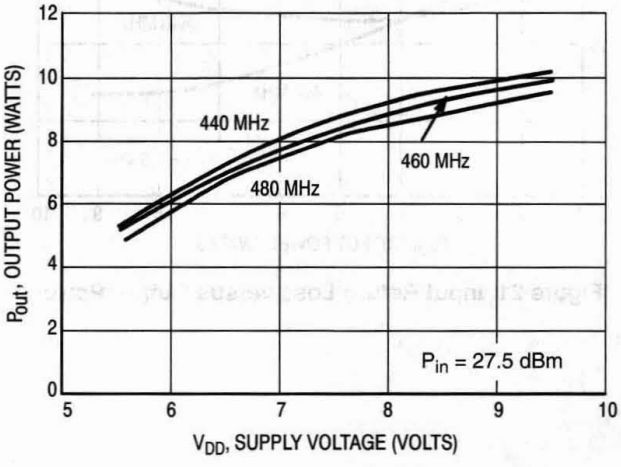


Figure 26. Output Power versus Supply Voltage

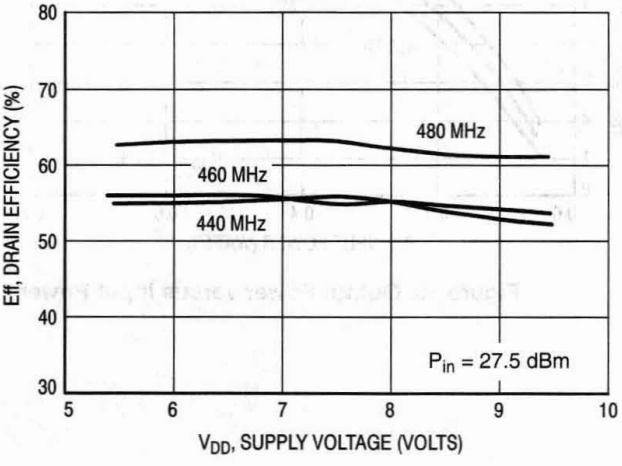
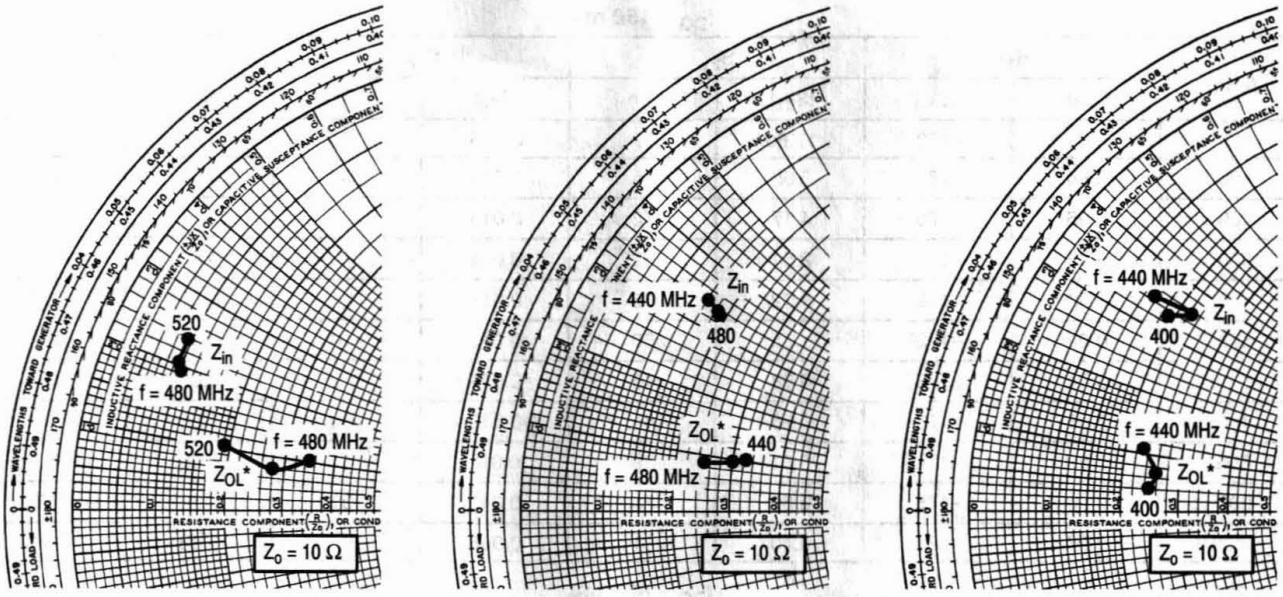


Figure 27. Drain Efficiency versus Supply Voltage



V_{DD} = 7.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
480	1.06 +j1.82	3.51 +j0.99
500	0.97 +j2.01	2.82 +j0.75
520	0.975 +j2.37	1.87 +j1.03

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 7.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
440	1.62 +j3.41	3.25 +j0.98
460	1.85 +j3.35	3.05 +j0.93
480	1.91 +j3.31	2.54 +j0.84

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 7.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
400	1.96 +j3.32	2.52 +j0.39
420	2.31 +j3.56	2.61 +j0.64
440	1.60 +j3.45	2.37 +j1.04

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

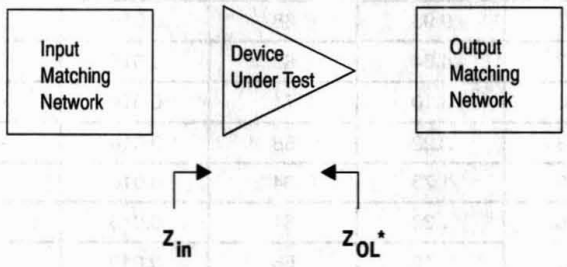


Figure 28. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 7.5 Vdc)

I_{DQ} = 150 mA

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.84	–152	17.66	97	0.016	0	0.77	–167
100	0.84	–164	8.86	85	0.016	5	0.78	–172
200	0.86	–170	4.17	72	0.015	–5	0.79	–173
300	0.88	–171	2.54	62	0.014	–8	0.80	–172
400	0.90	–172	1.72	55	0.013	–25	0.83	–172
500	0.92	–172	1.28	50	0.013	–10	0.84	–172
600	0.94	–173	0.98	46	0.014	–22	0.86	–171
700	0.95	–173	0.76	41	0.010	–30	0.86	–172
800	0.96	–174	0.61	38	0.011	–14	0.86	–171
900	0.96	–175	0.50	33	0.011	–31	0.85	–172
1000	0.97	–175	0.40	31	0.006	55	0.88	–171

I_{DQ} = 800 mA

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.90	–165	20.42	94	0.018	1	0.76	–164
100	0.89	–172	10.20	87	0.015	–7	0.77	–170
200	0.90	–175	4.96	79	0.015	–12	0.77	–172
300	0.90	–176	3.17	73	0.017	–2	0.80	–171
400	0.91	–176	2.26	67	0.013	1	0.82	–172
500	0.92	–176	1.75	63	0.011	–6	0.83	–171
600	0.93	–176	1.39	59	0.012	–31	0.85	–171
700	0.94	–176	1.14	55	0.015	–34	0.88	–171
800	0.94	–176	0.93	51	0.008	–22	0.87	–171
900	0.95	–177	0.78	45	0.007	2	0.87	–172
1000	0.96	–177	0.65	43	0.008	–40	0.90	–170

I_{DQ} = 1.5 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.92	–165	19.90	95	0.017	3	0.76	–164
100	0.90	–172	9.93	88	0.018	2	0.77	–170
200	0.91	–176	4.84	80	0.016	–4	0.77	–172
300	0.91	–176	3.10	74	0.014	–11	0.80	–172
400	0.92	–176	2.22	68	0.014	–14	0.81	–172
500	0.93	–176	1.73	64	0.016	–8	0.83	–171
600	0.94	–176	1.39	61	0.013	–24	0.85	–171
700	0.94	–176	1.12	56	0.013	–24	0.87	–171
800	0.95	–176	0.93	52	0.009	–12	0.87	–171
900	0.96	–177	0.78	46	0.008	10	0.87	–173
1000	0.97	–177	0.64	44	0.012	4	0.89	–169

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

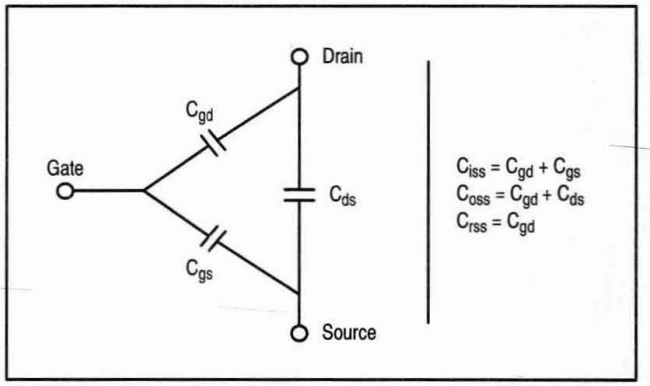
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD–1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two–port stability analysis with this device's S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

RF Power Field Effect Transistor

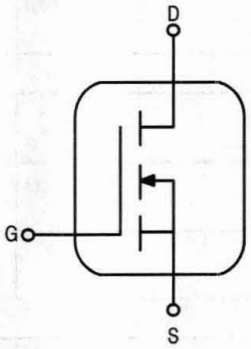
N–Channel Enhancement–Mode Lateral MOSFET

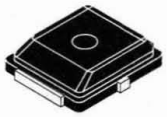
MRF1518T1

520 MHz, 8 W, 12.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

The MRF1518T1 is designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of this device make it ideal for large–signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
  Output Power — 8 Watts
  Power Gain — 11 dB
  Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 520 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- RF Power Plastic Surface Mount Package
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- Available in Tape and Reel. T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.





CASE 466–02, STYLE 1
(PLD–1.5)

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	40	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	62.5 0.50	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

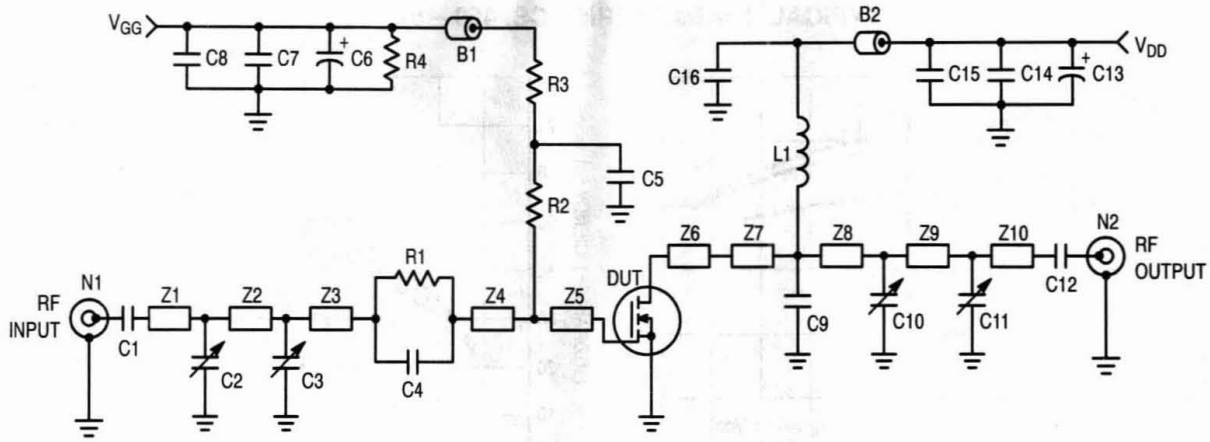
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current (V_{DS} = 40 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 12.5 Vdc, I_D = 100 μA)	$V_{GS(th)}$	1.0	1.6	2.1	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.4	—	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	66	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	33	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.5	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 520 MHz)	G_{ps}	10	11	—	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 520 MHz)	η	50	55	—	%



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	R4	33 kΩ, 1/8 W Resistor
C1, C12	240 pF, 100 mil Chip Capacitors	Z1	0.451″ x 0.080″ Microstrip
C2, C3, C10, C11	0 to 20 pF Trimmer Capacitors	Z2	1.005″ x 0.080″ Microstrip
C4	82 pF, 100 mil Chip Capacitor	Z3	0.020″ x 0.080″ Microstrip
C5, C16	120 pF, 100 mil Chip Capacitors	Z4	0.155″ x 0.080″ Microstrip
C6, C13	10 μF, 50 V Electrolytic Capacitors	Z5, Z6	0.260″ x 0.223″ Microstrip
C7, C14	1,200 pF, 100 mil Chip Capacitors	Z7	0.065″ x 0.080″ Microstrip
C8, C15	0.1 μF, 100 mil Chip Capacitors	Z8	0.266″ x 0.080″ Microstrip
C9	30 pF, 100 mil Chip Capacitor	Z9	1.113″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z10	0.433″ x 0.080″ Microstrip
N1, N2	Type N Flange Mounts	Board	Glass Teflon®, 31 mils, 2 oz. Copper
R1	15 Ω Chip Resistor (0805)		
R2	51 Ω, 1/2 W Resistor		
R3	10 Ω Chip Resistor (0805)		

Figure 1. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

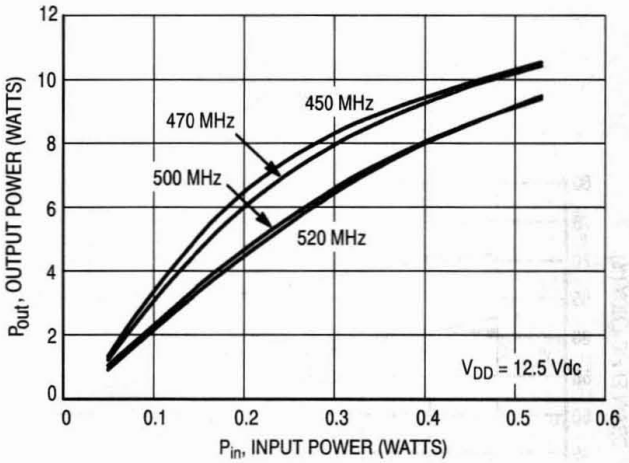


Figure 2. Output Power versus Input Power

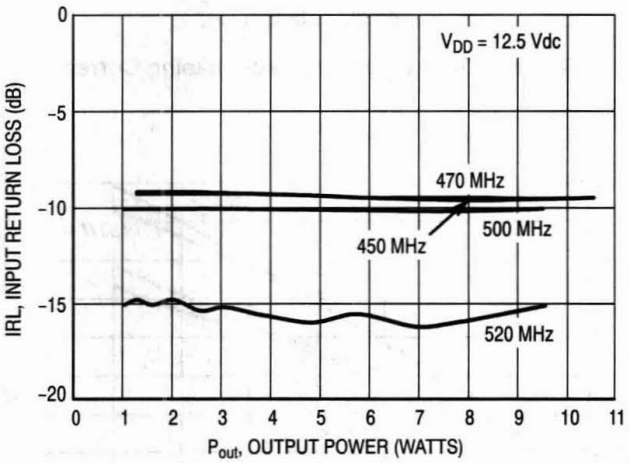


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 450 – 520 MHz

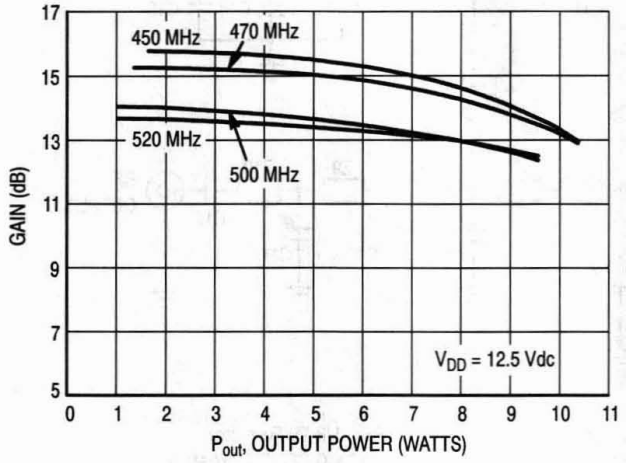


Figure 4. Gain versus Output Power

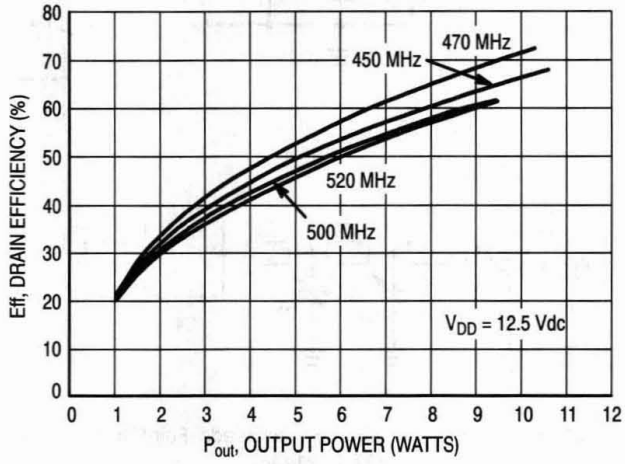


Figure 5. Drain Efficiency versus Output Power

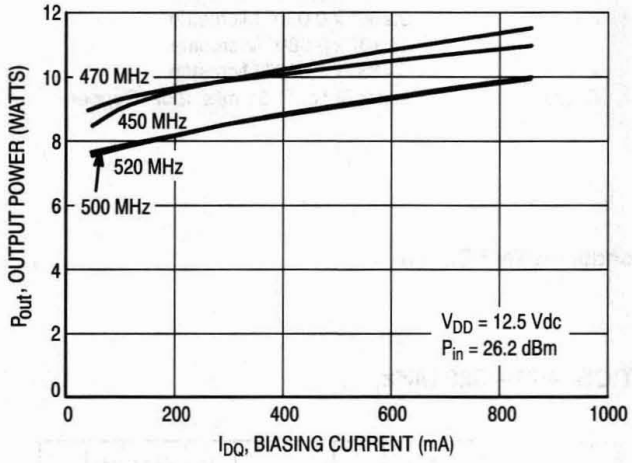


Figure 6. Output Power versus Biasing Current

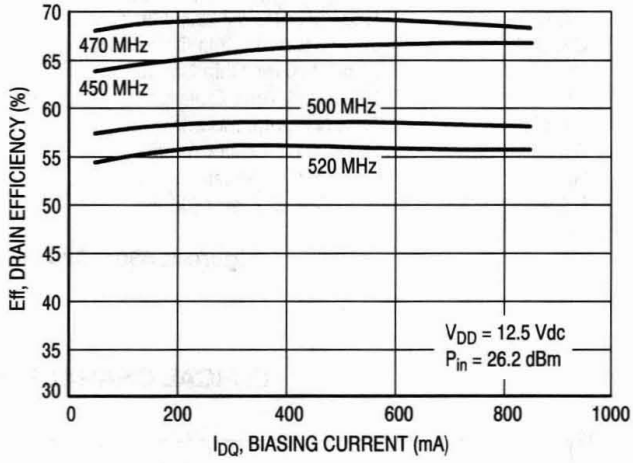


Figure 7. Drain Efficiency versus Biasing Current

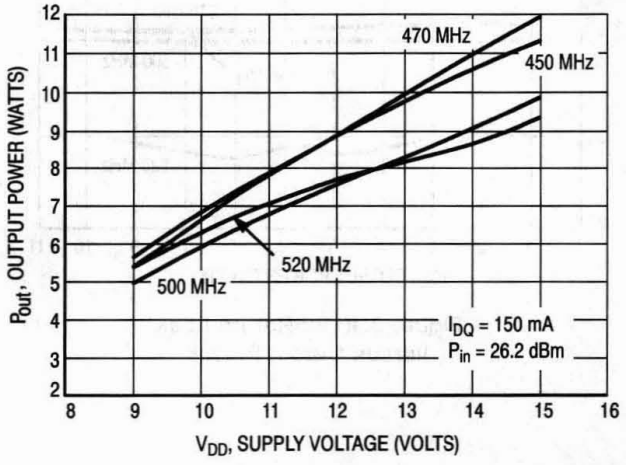


Figure 8. Output Power versus Supply Voltage

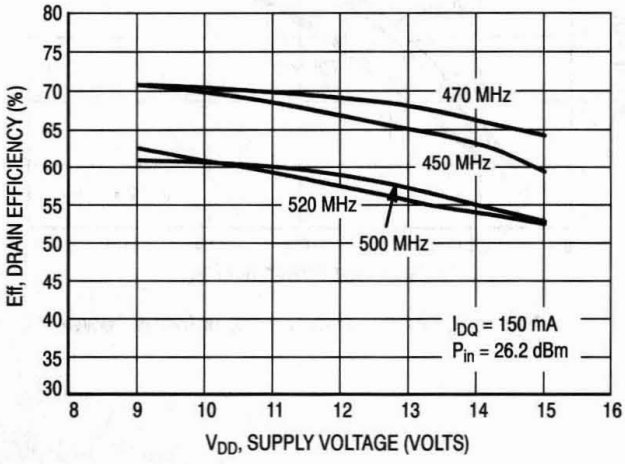
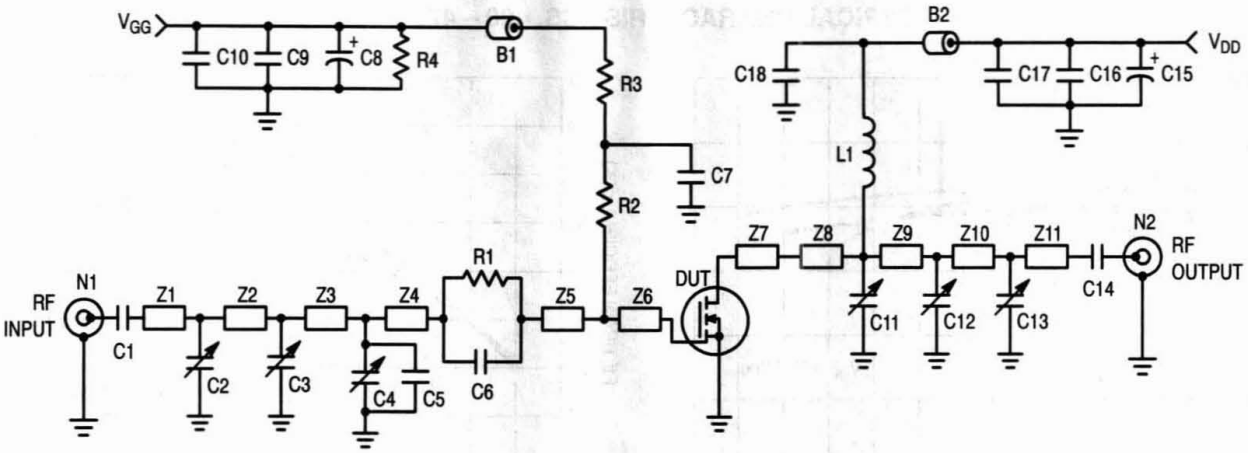


Figure 9. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	R3	10 Ω Chip Resistor (0805)
		R4	33 kΩ, 1/8 W Resistor
C1, C14	240 pF, 100 mil Chip Capacitors	Z1	0.476″ x 0.080″ Microstrip
C2, C3, C4, C11,		Z2	0.724″ x 0.080″ Microstrip
C12, C13	0 to 20 pF Trimmer Capacitors	Z3	0.348″ x 0.080″ Microstrip
C5	30 pF, 100 mil Chip Capacitor	Z4	0.048″ x 0.080″ Microstrip
C6	47 pF, 100 mil Chip Capacitor	Z5	0.175″ x 0.080″ Microstrip
C7, C18	120 pF, 100 mil Chip Capacitors	Z6, Z7	0.260″ x 0.223″ Microstrip
C8, C15	10 µF, 50 V Electrolytic Capacitors	Z8	0.239″ x 0.080″ Microstrip
C9, C16	1,200 pF, 100 mil Chip Capacitors	Z9	0.286″ x 0.080″ Microstrip
C10, C17	0.1 µF, 100 mil Chip Capacitors	Z10	0.806″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z11	0.553″ x 0.080″ Microstrip
N1, N2	Type N Flange Mounts	Board	Glass Teflon®, 31 mils, 2 oz. Copper
R1	15 Ω Chip Resistor (0805)		
R2	51 Ω, 1/2 W Resistor		

Figure 10. 400 – 470 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 400 – 470 MHz

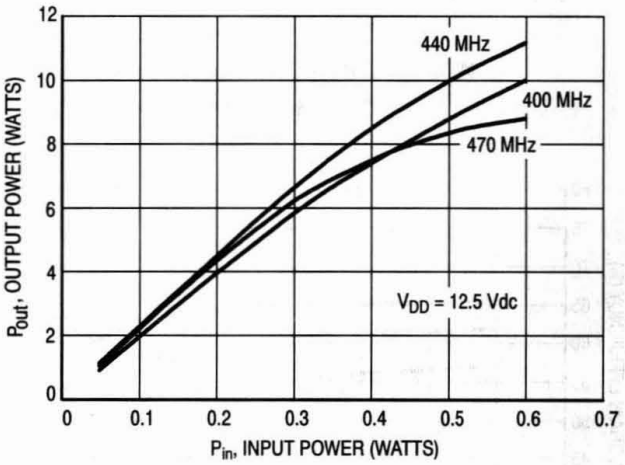


Figure 11. Output Power versus Input Power

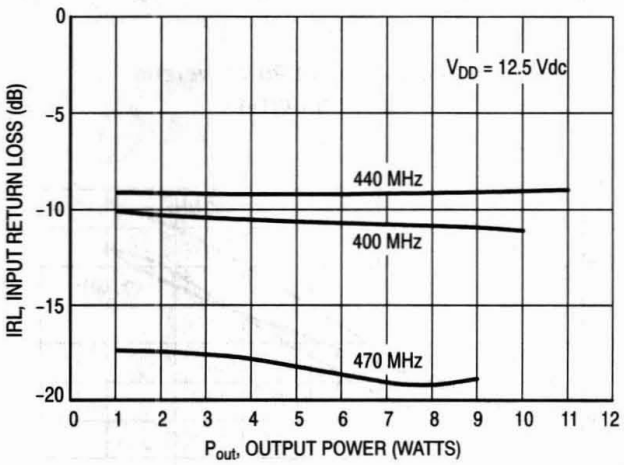


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 400 – 470 MHz

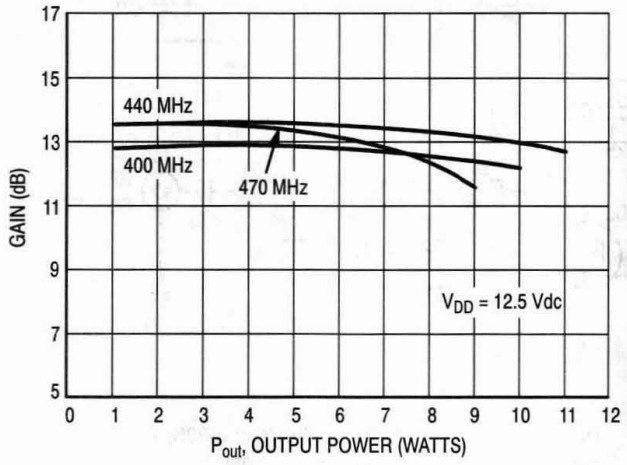


Figure 13. Gain versus Output Power

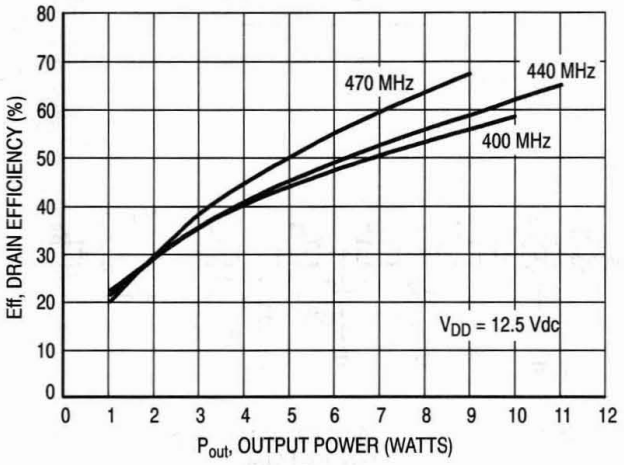


Figure 14. Drain Efficiency versus Output Power

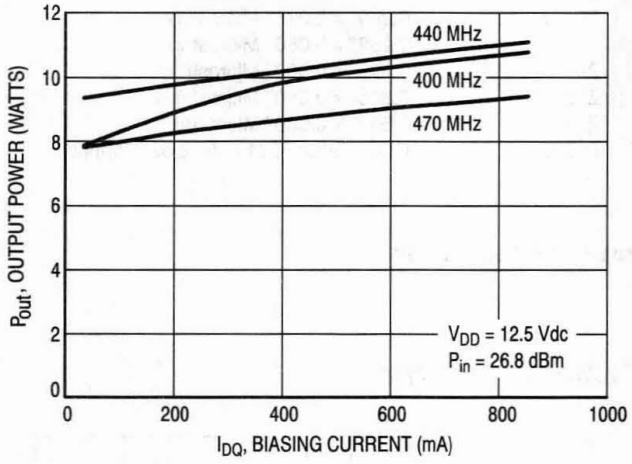


Figure 15. Output Power versus Biasing Current

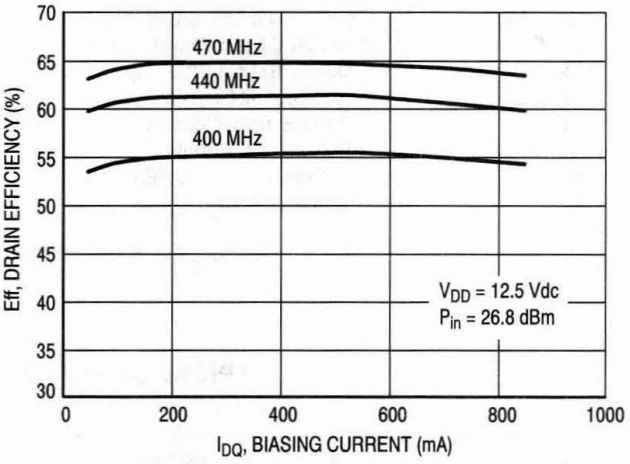


Figure 16. Drain Efficiency versus Biasing Current

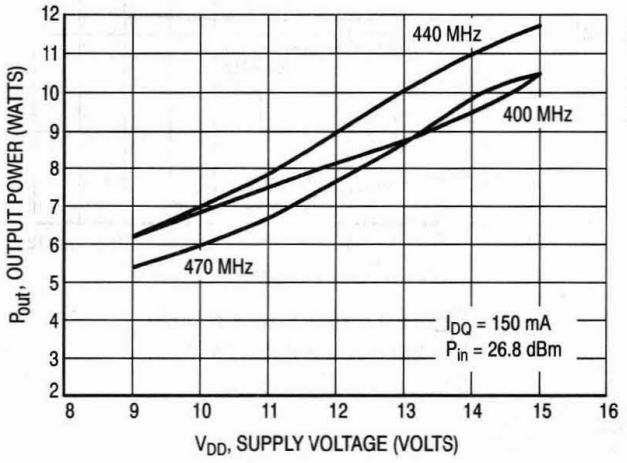


Figure 17. Output Power versus Supply Voltage

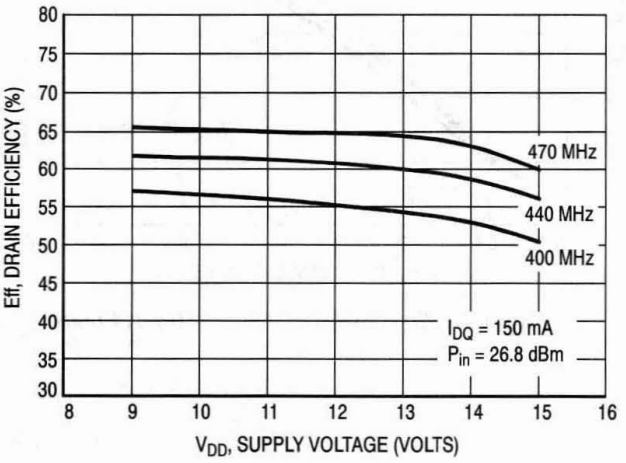
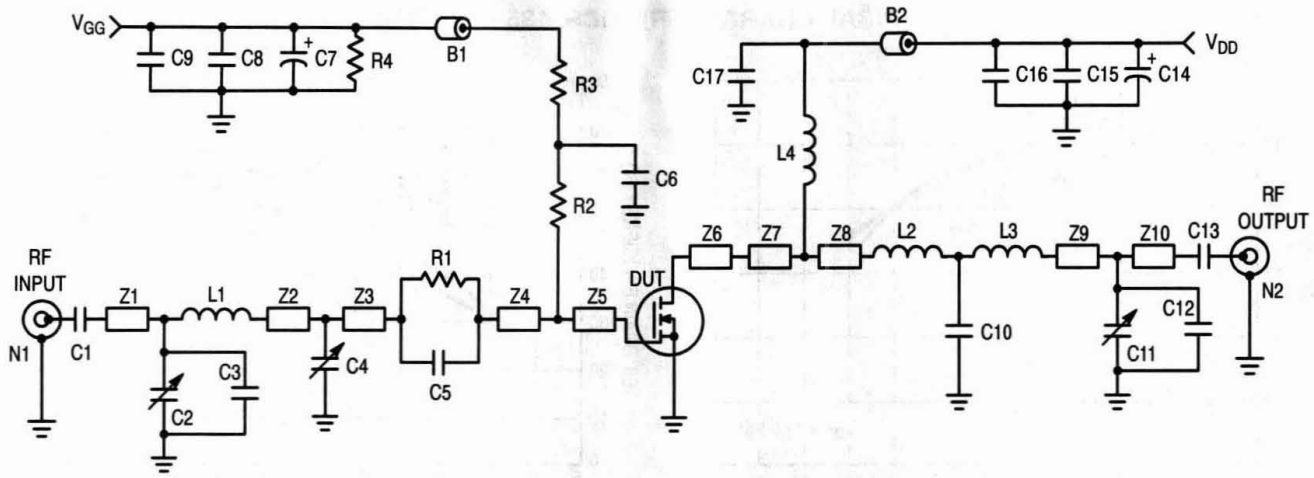


Figure 18. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	L4	55.5 nH, 5 Turn, Coilcraft
C1, C13	330 pF, 100 mil Chip Capacitors	N1, N2	Type N Flange Mounts
C2, C4, C11	0 to 20 pF Trimmer Capacitors	R1	15 Ω Chip Resistor (0805)
C3	12 pF, 100 mil Chip Capacitor	R2	56 Ω, 1/4 W Carbon Resistor
C5	43 pF, 100 mil Chip Capacitor	R3	100 Ω Chip Resistor (0805)
C6, C17	75 pF, 100 mil Chip Capacitors	R4	33 kΩ, 1/8 W Carbon Resistor
C7, C14	10 µF, 50 V Electrolytic Capacitors	Z1	0.115″ x 0.080″ Microstrip
C8, C15	1,200 pF, 100 mil Chip Capacitors	Z2	0.255″ x 0.080″ Microstrip
C9, C16	0.1 µF, 100 mil Chip Capacitors	Z3	1.037″ x 0.080″ Microstrip
C10	75 pF, 100 mil Chip Capacitor	Z4	0.192″ x 0.080″ Microstrip
C12	13 pF, 100 mil Chip Capacitor	Z5, Z6	0.260″ x 0.223″ Microstrip
L1	26 nH, 4 Turn, Coilcraft	Z7	0.125″ x 0.080″ Microstrip
L2	5 nH, 2 Turn, Coilcraft	Z8	0.962″ x 0.080″ Microstrip
L3	33 nH, 5 Turn, Coilcraft	Z9	0.305″ x 0.080″ Microstrip
		Z10	0.155″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 19. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

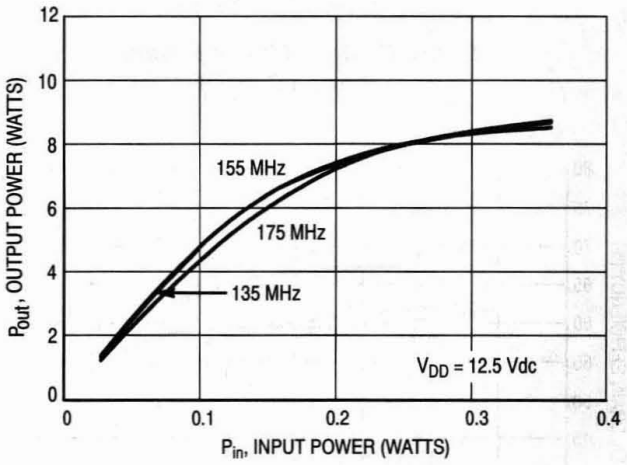


Figure 20. Output Power versus Input Power

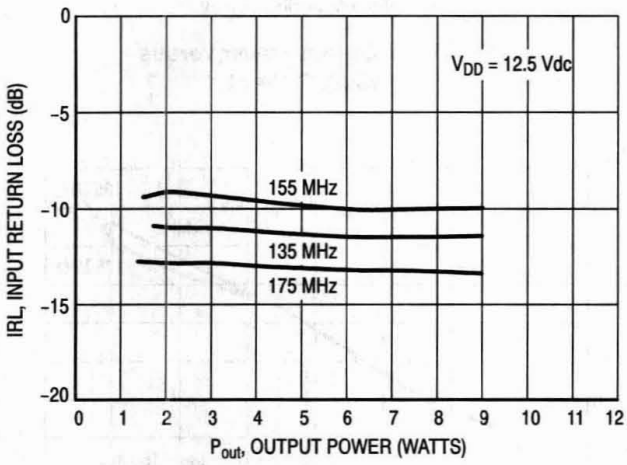


Figure 21. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 – 175 MHz

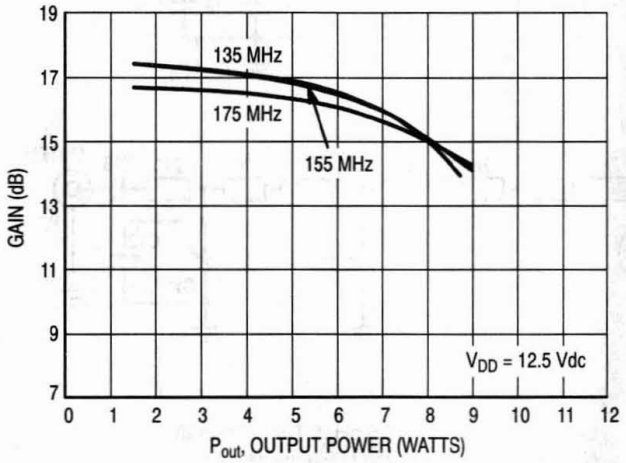


Figure 22. Gain versus Output Power

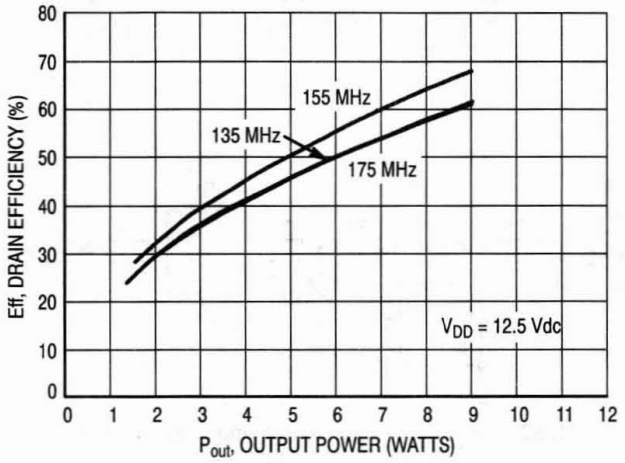


Figure 23. Drain Efficiency versus Output Power

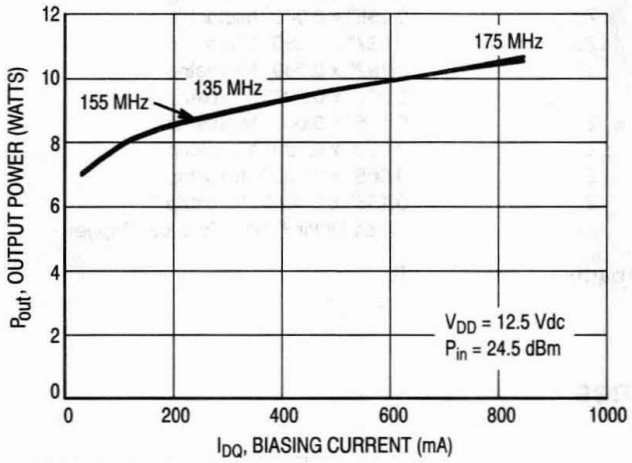


Figure 24. Output Power versus Biasing Current

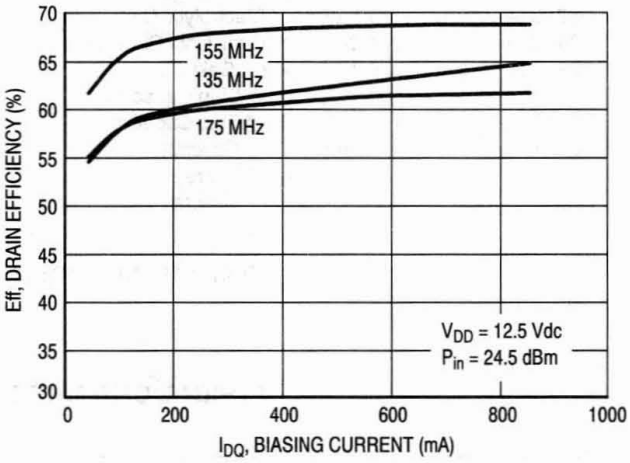


Figure 25. Drain Efficiency versus Biasing Current

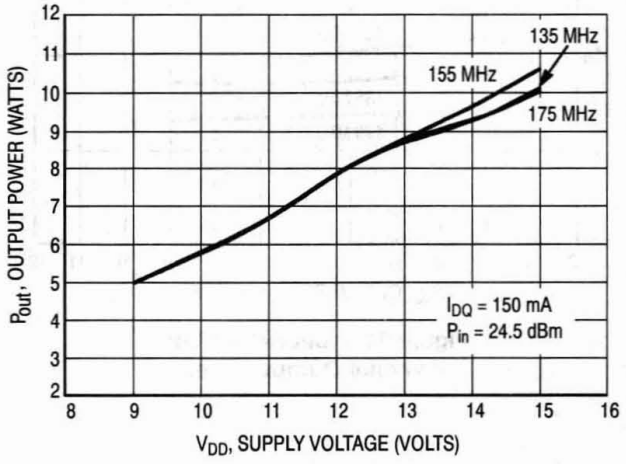


Figure 26. Output Power versus Supply Voltage

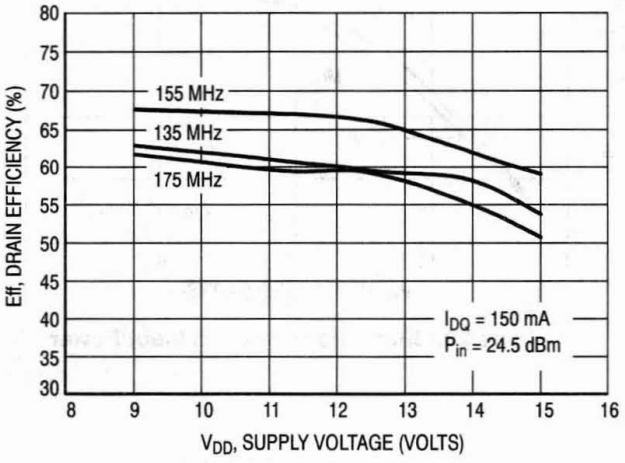
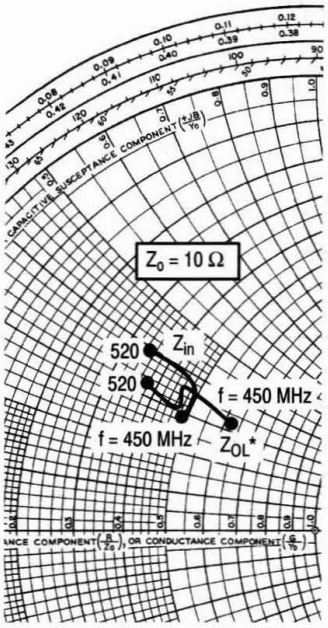
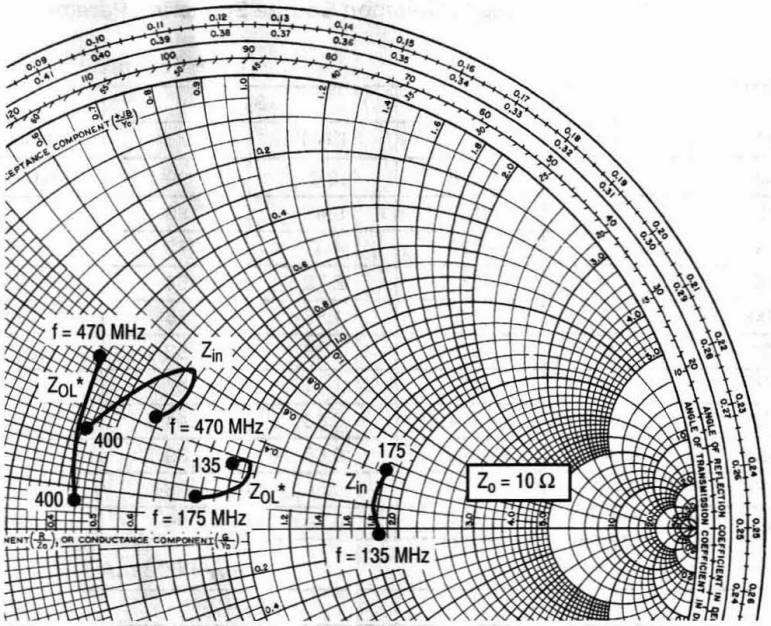


Figure 27. Drain Efficiency versus Supply Voltage





V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
450	4.9 +j2.85	6.42 +j3.23
470	4.85 +j3.71	4.59 +j3.61
500	4.63 +j3.84	4.72 +j3.12
520	3.52 +j3.92	3.81 +j3.27

V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
400	4.28 +j2.36	4.41 +j0.67
440	6.45 +j5.13	4.14 +j2.53
470	5.91 +j3.34	3.92 +j4.02

V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	18.31 –j0.76	8.97 +j2.62
155	17.72 +j1.85	9.69 +j2.81
175	18.06 +j5.23	7.94 +j1.14

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 82 pF capacitor in series with gate. (See Figure 1).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 47 pF capacitor in series with gate. (See Figure 10).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 43 pF capacitor in series with gate. (See Figure 19).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

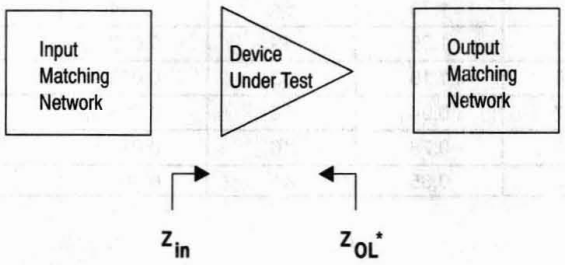


Figure 28. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 12.5 Vdc)

I_{DQ} = 150 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.88	−148	18.91	99	0.033	11	0.67	−144
100	0.85	−163	9.40	86	0.033	−6	0.66	−158
200	0.85	−170	4.47	73	0.026	−17	0.69	−162
300	0.87	−171	2.72	64	0.025	−28	0.74	−163
400	0.88	−172	1.85	56	0.021	−21	0.79	−164
500	0.90	−173	1.35	52	0.019	−30	0.83	−165
600	0.92	−173	1.04	47	0.014	−26	0.85	−167
700	0.93	−174	0.83	44	0.015	−39	0.88	−168
800	0.94	−175	0.68	39	0.014	−31	0.90	−169
900	0.94	−175	0.55	36	0.010	−41	0.91	−170
1000	0.96	−176	0.46	30	0.011	−38	0.95	−170

I_{DQ} = 800 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.90	−159	20.80	97	0.020	14	0.73	−162
100	0.88	−169	10.35	88	0.018	1	0.74	−169
200	0.88	−174	5.09	79	0.017	−9	0.75	−171
300	0.89	−175	3.23	73	0.015	−18	0.77	−171
400	0.89	−175	2.30	67	0.015	−17	0.80	−171
500	0.90	−176	1.74	63	0.014	−22	0.82	−170
600	0.91	−176	1.39	59	0.014	−19	0.83	−171
700	0.92	−176	1.16	55	0.009	−23	0.85	−171
800	0.93	−176	0.96	50	0.011	−14	0.87	−172
900	0.94	−177	0.80	46	0.007	4	0.88	−173
1000	0.94	−177	0.67	41	0.010	−15	0.89	−173

I_{DQ} = 1.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.91	−159	20.18	97	0.015	11	0.73	−165
100	0.89	−169	10.05	89	0.016	−5	0.74	−171
200	0.88	−174	4.93	80	0.015	−3	0.75	−172
300	0.89	−175	3.14	73	0.014	−14	0.78	−172
400	0.89	−176	2.24	67	0.014	−20	0.80	−171
500	0.90	−176	1.70	64	0.014	−22	0.82	−170
600	0.92	−176	1.36	59	0.010	−16	0.84	−171
700	0.92	−176	1.13	55	0.013	−10	0.85	−171
800	0.93	−177	0.94	50	0.008	−13	0.87	−172
900	0.94	−177	0.78	46	0.013	−26	0.87	−173
1000	0.94	−178	0.65	41	0.007	8	0.87	−172

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

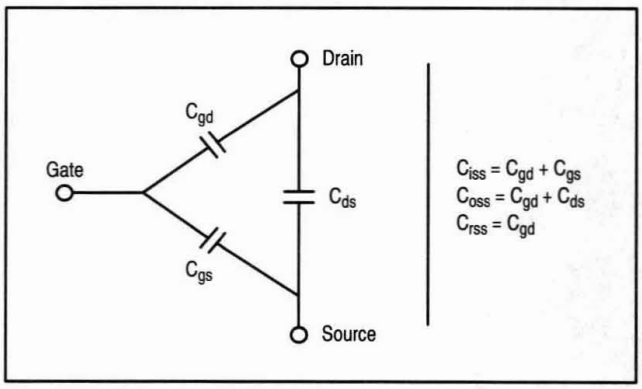
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD–1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two–port stability analysis with this device's S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

RF Power Field Effect Transistor

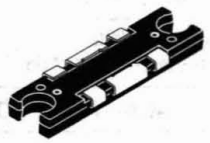
N–Channel Enhancement–Mode Lateral MOSFET

MRF1535T1

520 MHz, 35 W, 12.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

The MRF1535T1 is designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of this device make it ideal for large–signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
  Output Power — 35 Watts
  Power Gain — 10.0 dB
  Efficiency — 50%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 520 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Broadband–Full Power Across the Band: 135–175 MHz
  400–470 MHz
  450–520 MHz
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- RF Power Plastic Surface Mount Package
- Available in Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.



CASE 1264–07, STYLE 1
(TO–272)

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	40	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	6	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	135 0.50	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	175	°C

THERMAL CHARACTERISTICS

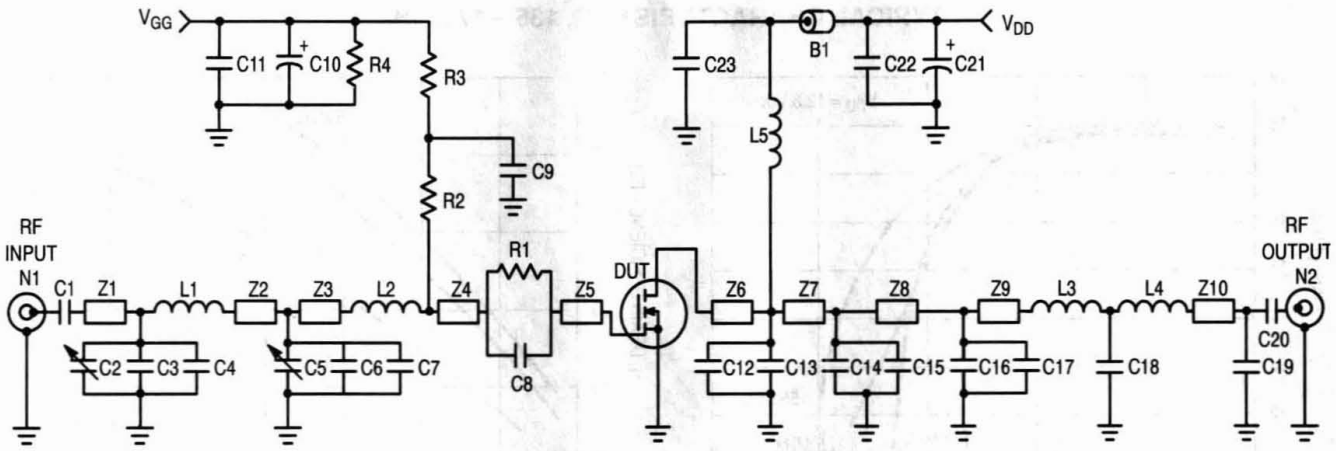
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.90	°C/W

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	0.3	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 12.5 Vdc, I_D = 400 μA)	$V_{GS(th)}$	1	—	2.6	Vdc
Drain–Source On–Voltage (V_{GS} = 5 Vdc, I_D = 0.6 A)	$R_{DS(on)}$	—	—	0.7	Ω
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$V_{DS(on)}$	—	—	1	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (Includes Input Matching Capacitance) (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	—	—	250	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	—	—	150	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	—	—	20	pF
RF CHARACTERISTICS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 35 Watts, I_{DQ} = 500 mA) f = 520 MHz	G_{ps}	10	—	—	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 35 Watts, I_{DQ} = 500 mA) f = 520 MHz	η	50	—	—	%
Load Mismatch (V_{DD} = 15.6 Vdc, f = 520 MHz, 2 dB Input Overdrive, VSWR 20:1 at All Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			



B1	Ferroxcube #VK200	L4	1 Turn, #26 AWG, 0.240″ ID
C1, C9, C20, C23	330 pF, 100 mil Chip Capacitors	L5	4 Turn, #24 AWG, 0.180″ ID
C2, C5	0 to 20 pF Trimmer Capacitors	N1, N2	Type N Flange Mounts
C3, C15	33 pF, 100 mil Chip Capacitors	R1	6.5 Ω, 1/4 W Chip Resistor
C4, C6, C19	18 pF, 100 mil Chip Capacitors	R2	39 Ω Chip Resistor (0805)
C7	160 pF, 100 mil Chip Capacitor	R3	1.2 kΩ, 1/8 W Chip Resistor
C8	240 pF, 100 mil Chip Capacitor	R4	33 kΩ, 1/4 W Chip Resistor
C10, C21	10 µF, 50 V Electrolytic Capacitors	Z1	0.970″ x 0.080″ Microstrip
C11, C22	470 pF, 100 mil Chip Capacitors	Z2	0.380″ x 0.080″ Microstrip
C12, C13	150 pF, 100 mil Chip Capacitors	Z3	0.190″ x 0.080″ Microstrip
C14	110 pF, 100 mil Chip Capacitor	Z4	0.160″ x 0.080″ Microstrip
C16	68 pF, 100 mil Chip Capacitor	Z5, Z6	0.110″ x 0.200″ Microstrip
C17	120 pF, 100 mil Chip Capacitor	Z7	0.490″ x 0.080″ Microstrip
C18	51 pF, 100 mil Chip Capacitor	Z8	0.250″ x 0.080″ Microstrip
L1	17.5 nH, Coilcraft #A05T	Z9	0.320″ x 0.080″ Microstrip
L2	5 nH, Coilcraft #A02T	Z10	0.240″ x 0.080″ Microstrip
L3	1 Turn, #26 AWG, 0.250″ ID	Board	Glass Teflon®, 31 mils

Figure 1. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

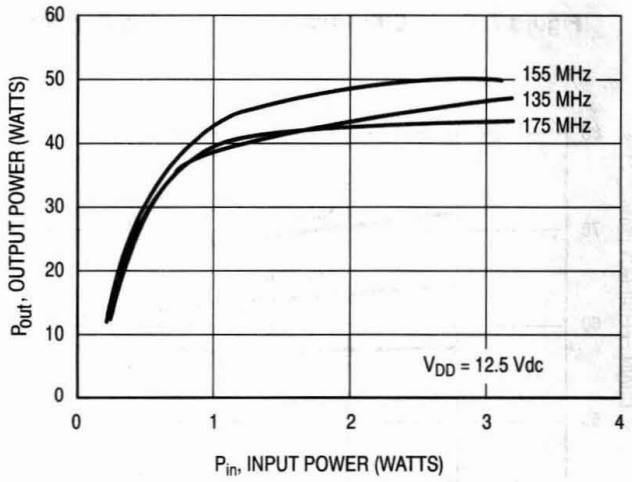


Figure 2. Output Power versus Input Power

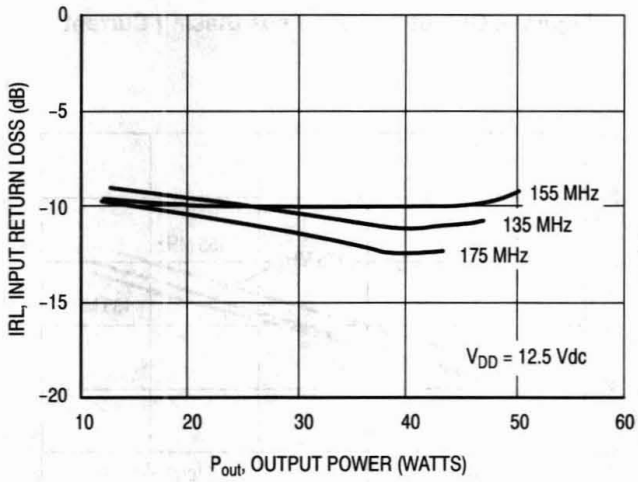


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 – 175 MHz

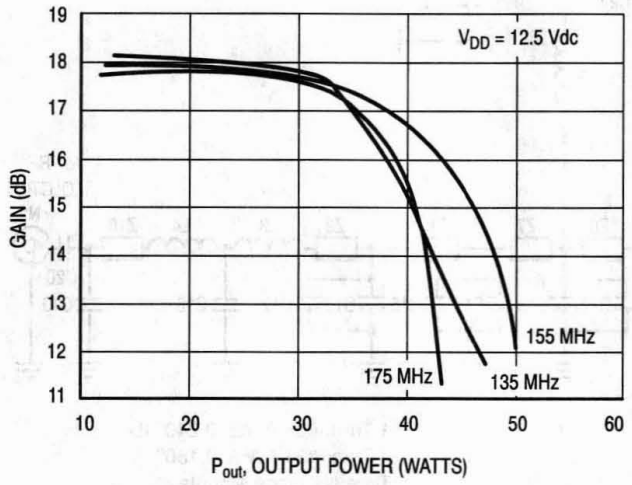


Figure 4. Gain versus Output Power

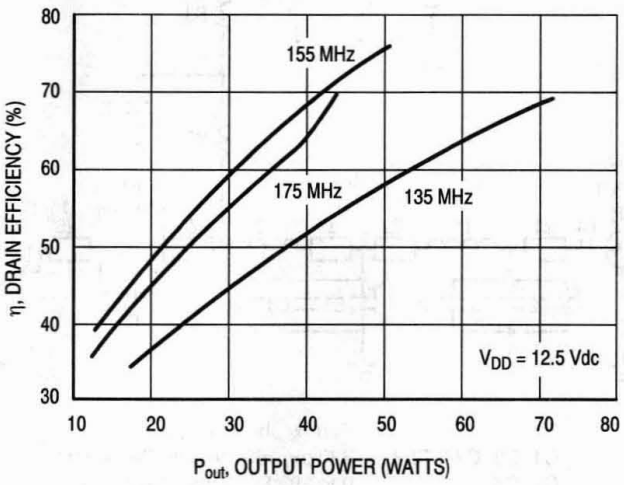


Figure 5. Drain Efficiency versus Output Power

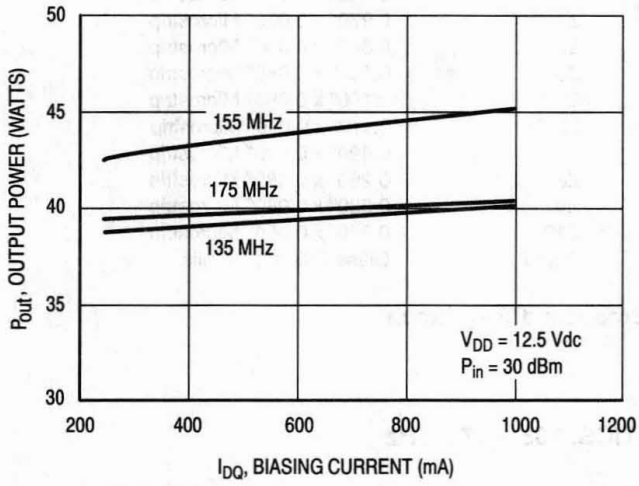


Figure 6. Output Power versus Biasing Current

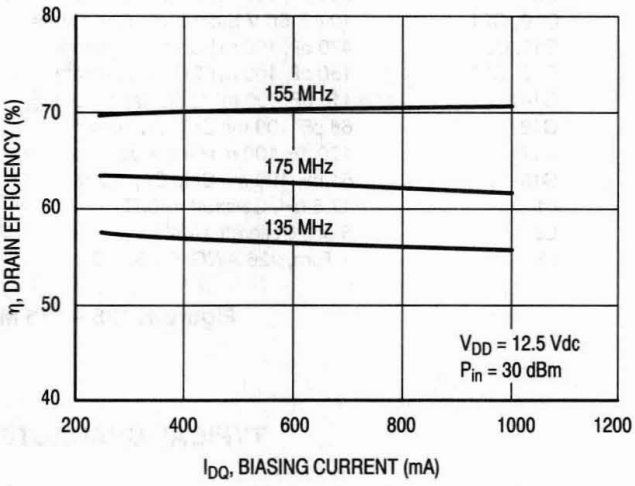


Figure 7. Drain Efficiency versus Biasing Current

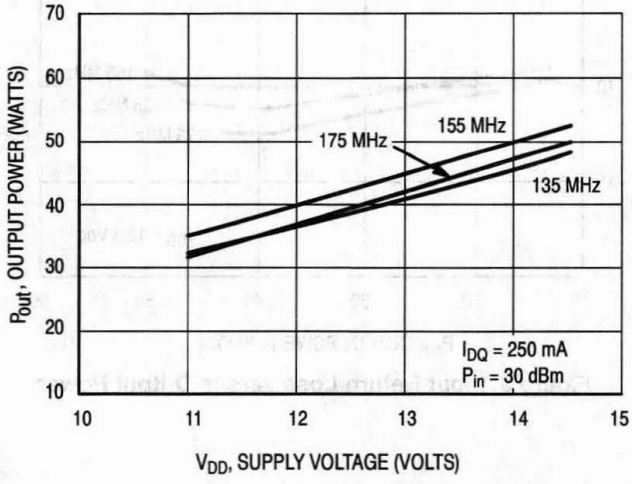


Figure 8. Output Power versus Supply Voltage

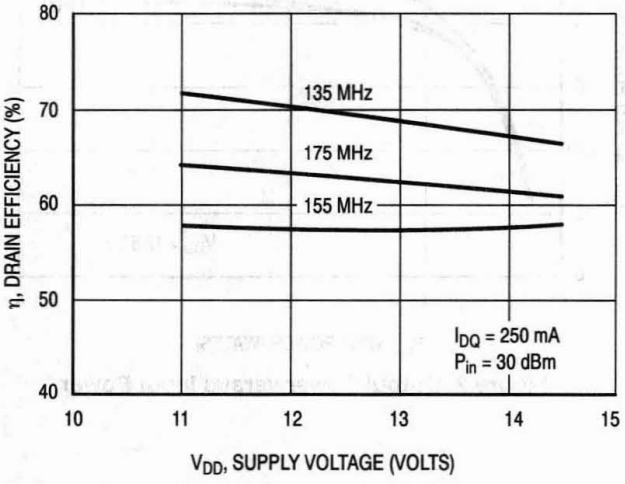
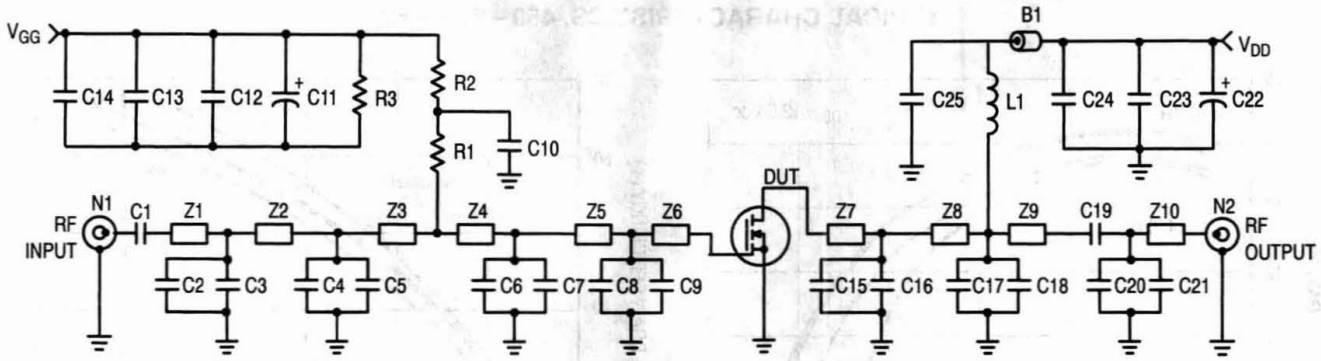


Figure 9. Drain Efficiency versus Supply Voltage



B1	Ferroxcube VK200	C21	1.8 pF, 100 mil Chip Capacitor
C1	160 pF, 100 mil Chip Capacitor	L1	47.5 nH, 5 Turn, Coilcraft
C2	3 pF, 100 mil Chip Capacitor	N1, N2	Type N Flange Mounts
C3	3.6 pF, 100 mil Chip Capacitor	R1	500 Ω Chip Resistor (0805)
C4	2.2 pF, 100 mil Chip Capacitor	R2	1 kΩ Chip Resistor (0805)
C5	10 pF, 100 mil Chip Capacitor	R3	33 kΩ, 1/8 W Chip Resistor
C6, C7	16 pF, 100 mil Chip Capacitors	Z1	0.480″ x 0.080″ Microstrip
C8, C15, C16	27 pF, 100 mil Chip Capacitors	Z2	1.070″ x 0.080″ Microstrip
C9	43 pF, 100 mil Chip Capacitor	Z3	0.290″ x 0.080″ Microstrip
C10, C14, C25	160 pF, 100 mil Chip Capacitors	Z4	0.160″ x 0.080″ Microstrip
C11, C22	10 µF, 50 V Electrolytic Capacitors	Z5, Z8	0.120″ x 0.080″ Microstrip
C12, C24	1,200 pF, 100 mil Chip Capacitors	Z6, Z7	0.120″ x 0.223″ Microstrip
C13, C23	0.1 µF, 100 mil Chip Capacitors	Z9	1.380″ x 0.080″ Microstrip
C17, C18	24 pF, 100 mil Chip Capacitors	Z10	0.625″ x 0.080″ Microstrip
C19	160 pF, 100 mil Chip Capacitor	Board	Glass Teflon®, 31 mils
C20	8.2 pF, 100 mil Chip Capacitor		

Figure 10. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

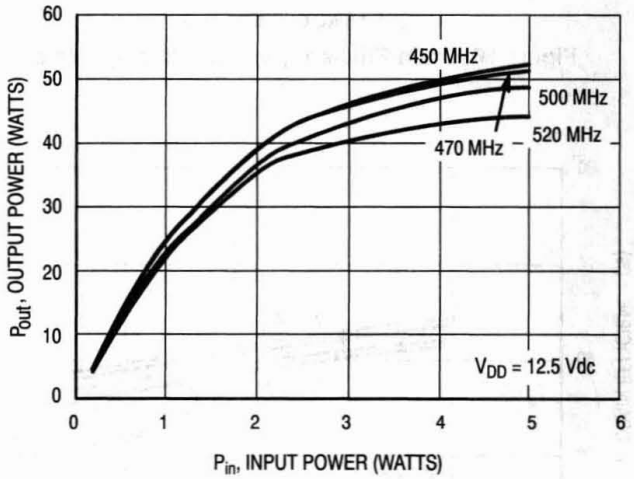


Figure 11. Output Power versus Input Power

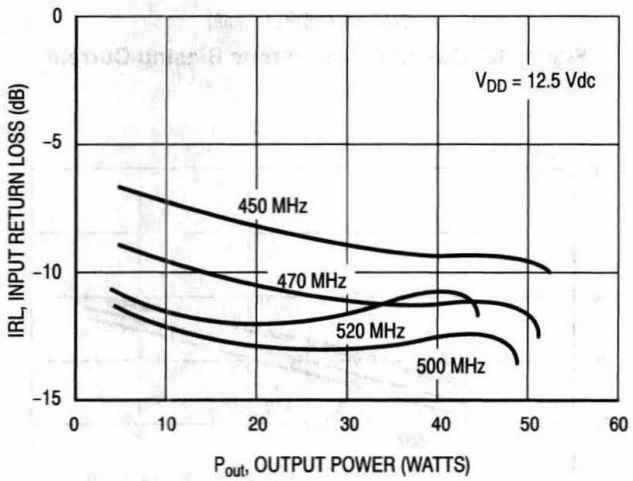


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 450 – 520 MHz

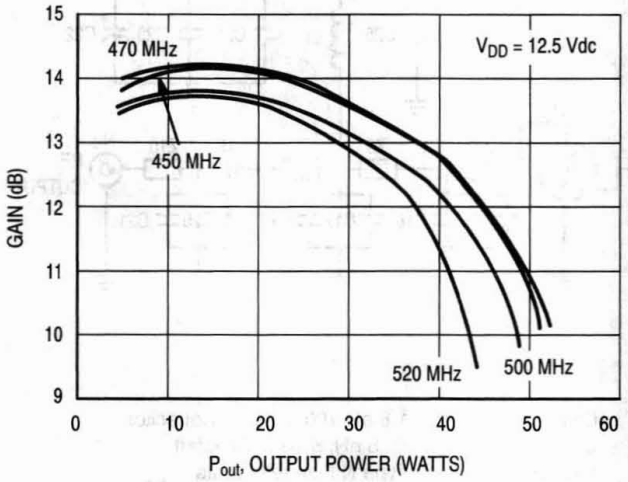


Figure 13. Gain versus Output Power

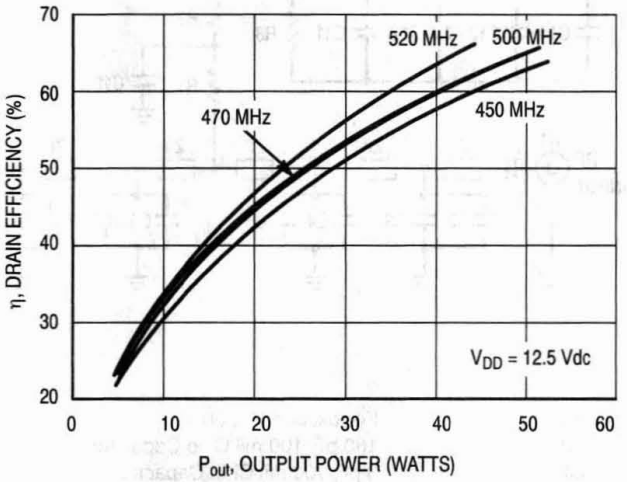


Figure 14. Drain Efficiency versus Output Power

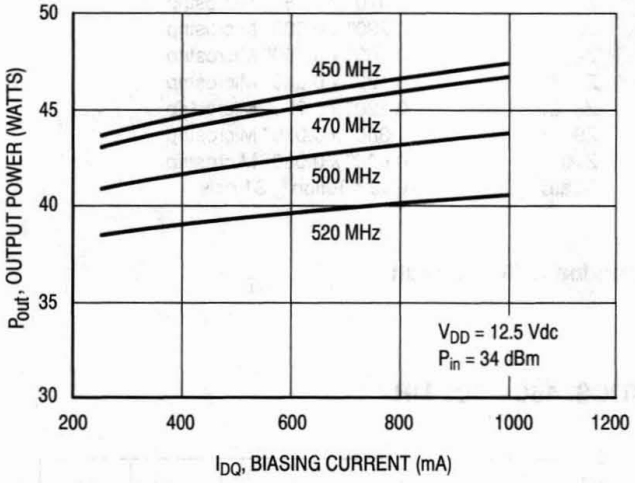


Figure 15. Output Power versus Biasing Current

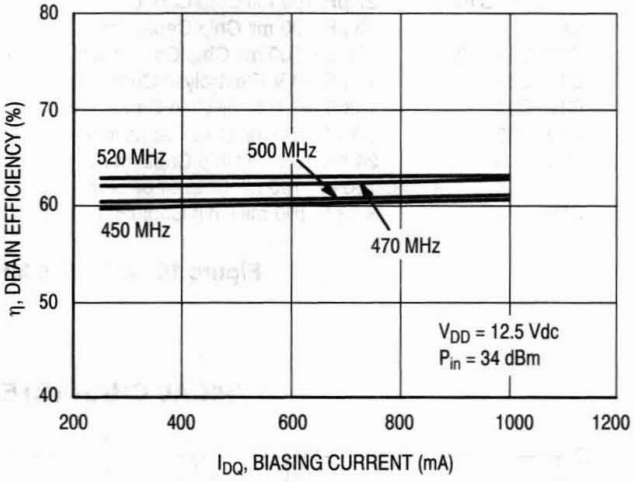


Figure 16. Drain Efficiency versus Biasing Current

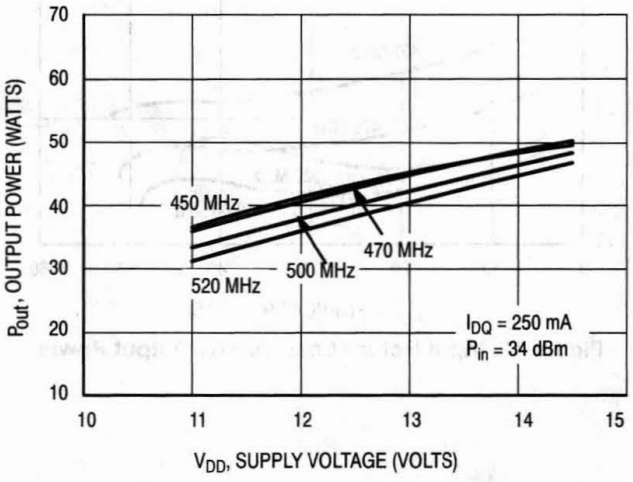


Figure 17. Output Power versus Supply Voltage

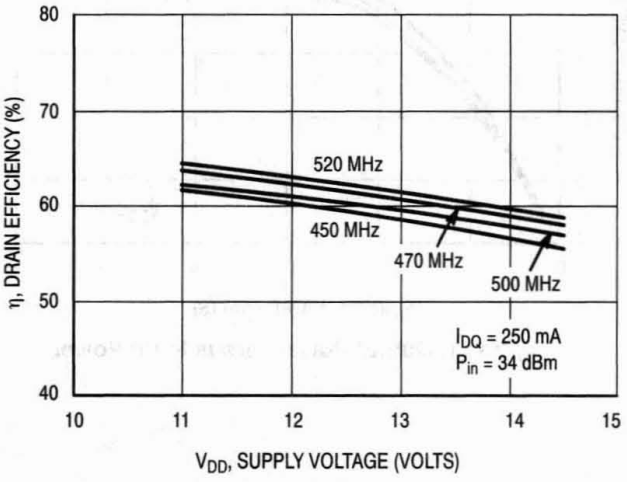
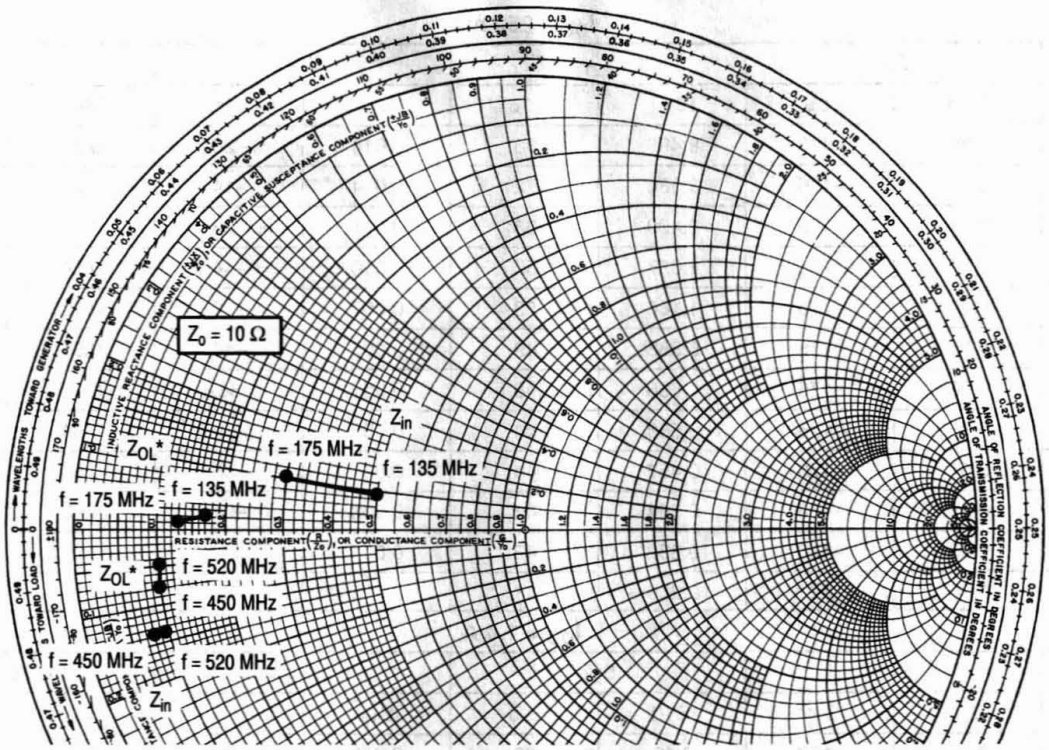


Figure 18. Drain Efficiency versus Supply Voltage



V_{DD} = 12.5 V, I_{DQ} = 250 mA, P_{out} = 35 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	5.0 + j0.9	1.7 + j0.2
155	5.0 + j0.9	1.7 + j0.2
175	3.0 + j1.0	1.3 + j0.1

V_{DD} = 12.5 V, I_{DQ} = 500 mA, P_{out} = 35 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
450	0.8 – j1.4	1.0 – j0.8
470	0.9 – j1.4	1.1 – j0.6
500	1.0 – j1.4	1.1 – j0.6
520	0.9 – j1.4	1.1 – j0.5

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

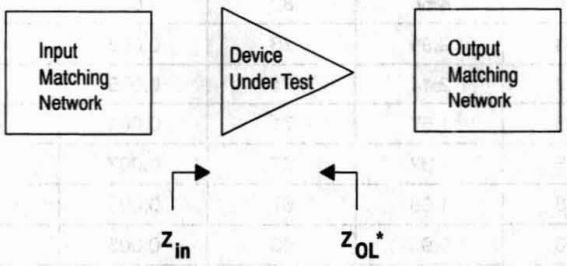


Figure 19. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 12.5 Vdc)

I_{DQ} = 250 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
50	0.89	–173	8.496	83	0.014	–26	0.76	–170
100	0.90	–175	3.936	72	0.014	–14	0.79	–170
150	0.91	–175	2.429	63	0.011	–23	0.82	–170
200	0.92	–175	1.627	57	0.010	–44	0.86	–170
250	0.94	–176	1.186	53	0.007	–16	0.88	–170
300	0.95	–176	0.888	49	0.005	–44	0.91	–171
350	0.96	–176	0.686	48	0.005	36	0.92	–170
400	0.96	–176	0.568	44	0.005	–1	0.94	–171
450	0.97	–176	0.457	44	0.004	49	0.94	–172
500	0.97	–176	0.394	44	0.003	–51	0.95	–171
550	0.98	–176	0.332	42	0.001	31	0.95	–173
600	0.98	–177	0.286	41	0.013	99	0.94	–173

I_{DQ} = 1.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
50	0.90	–173	8.49	83	0.006	–39	0.86	–176
100	0.90	–175	3.92	72	0.009	–5	0.86	–176
150	0.91	–175	2.44	63	0.006	7	0.87	–176
200	0.92	–175	1.62	57	0.008	21	0.88	–175
250	0.94	–176	1.19	53	0.006	8	0.89	–174
300	0.95	–176	0.89	48	0.008	3	0.89	–174
350	0.96	–176	0.69	48	0.007	48	0.91	–174
400	0.96	–176	0.57	44	0.004	41	0.93	–173
450	0.97	–176	0.46	44	0.004	43	0.93	–173
500	0.97	–176	0.39	44	0.003	57	0.94	–173
550	0.98	–176	0.33	41	0.006	62	0.94	–174
600	0.98	–177	0.28	41	0.009	96	0.93	–173

I_{DQ} = 2.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
50	0.94	–176	9.42	88	0.005	–72	0.89	–177
100	0.94	–178	4.56	82	0.005	4	0.89	–177
150	0.94	–178	2.99	78	0.003	7	0.89	–177
200	0.94	–178	2.14	74	0.005	17	0.90	–176
250	0.95	–178	1.67	71	0.004	40	0.90	–175
300	0.95	–178	1.32	67	0.007	35	0.91	–175
350	0.95	–178	1.08	67	0.005	57	0.92	–174
400	0.96	–178	0.93	63	0.003	50	0.93	–173
450	0.96	–178	0.78	62	0.007	68	0.93	–173
500	0.96	–177	0.68	61	0.004	99	0.94	–173
550	0.97	–177	0.59	58	0.008	78	0.93	–175
600	0.97	–178	0.51	57	0.009	92	0.92	–174

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

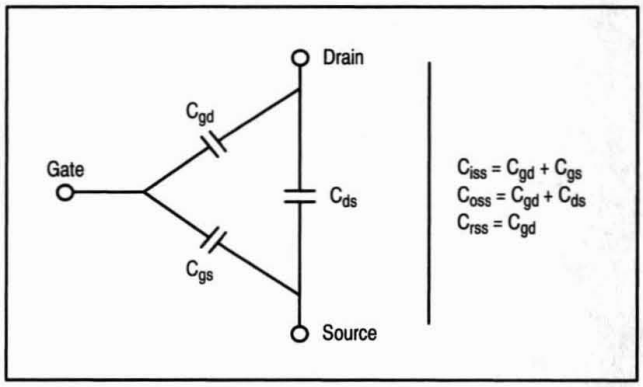
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD–1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two–port stability analysis with this device's S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

RF Power Field Effect Transistor

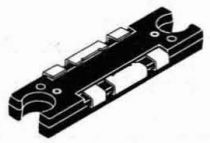
N–Channel Enhancement–Mode Lateral MOSFET

MRF1550T1

175 MHz, 50 W, 12.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

The MRF1550T1 is designed for broadband commercial and industrial applications with frequencies to 175 MHz. The high gain and broadband performance of this device make it ideal for large–signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 175 MHz, 12.5 Volts
  Output Power — 50 Watts
  Power Gain — 12 dB
  Efficiency — 50%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 175 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- RF Power Plastic Surface Mount Package
- Broadband–Full Power Across the Band: 135–175 MHz
- Broadband Demonstration Amplifier Information Available Upon Request
- Available in Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.



CASE 1264–07, STYLE 1
(TO–272)

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	40	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	12	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	165 0.50	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.75	°C/W

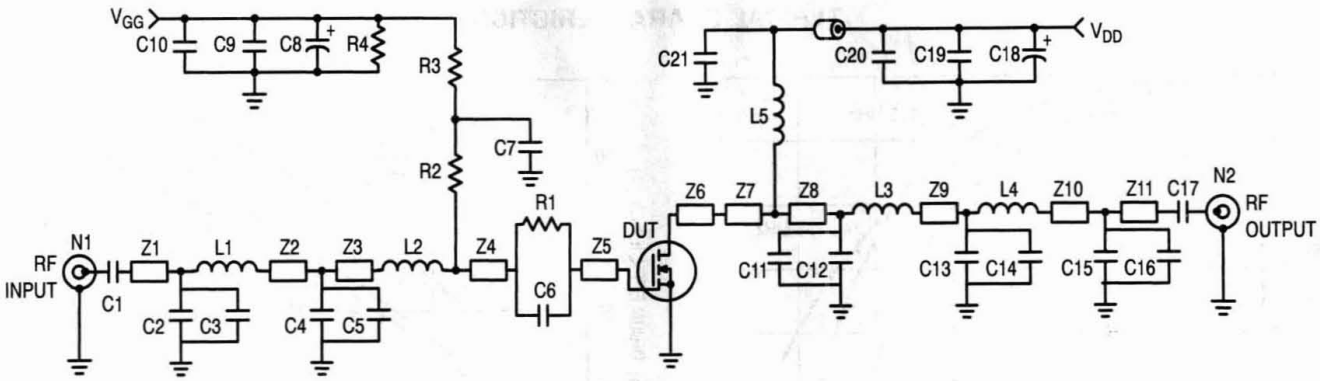
(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 4

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	0.5	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 12.5 Vdc, I_D = 800 μA)	$V_{GS(th)}$	1	—	3	Vdc
Drain–Source On–Voltage (V_{GS} = 5 Vdc, I_D = 1.2 A)	$R_{DS(on)}$	—	—	0.5	Ω
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	$V_{DS(on)}$	—	—	1	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (Includes Input Matching Capacitance) (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	—	—	500	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	—	—	250	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	—	—	35	pF
RF CHARACTERISTICS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 50 Watts, I_{DQ} = 500 mA) f = 175 MHz	G_{ps}	10	—	—	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 50 Watts, I_{DQ} = 500 mA) f = 175 MHz	η	50	—	—	%
Load Mismatch (V_{DD} = 15.6 Vdc, f = 175 MHz, 2 dB Input Overdrive, VSWR 20:1 at All Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			



B1	Ferroxcube #VK200
C1	180 pF, 100 mil Chip Capacitor
C2	10 pF, 100 mil Chip Capacitor
C3	33 pF, 100 mil Chip Capacitor
C4, C16	24 pF, 100 mil Chip Capacitors
C5	160 pF, 100 mil Chip Capacitor
C6	240 pF, 100 mil Chip Capacitor
C7, C17	300 pF, 100 mil Chip Capacitors
C8, C18	10 µF, 50 V Electrolytic Capacitors
C9, C19	0.1 µF, 100 mil Chip Capacitors
C10	470 pF, 100 mil Chip Capacitor
C11, C12	200 pF, 100 mil Chip Capacitors
C13	22 pF, 100 mil Chip Capacitor
C14	30 pF, 100 mil Chip Capacitor
C15	6.8 pF, 100 mil Chip Capacitor
C20	1,000 pF, 100 mil Chip Capacitor
L1	18.5 nH, Coilcraft #A05T
L2	5 nH, Coilcraft #A02T
L3	1 Turn, #24 AWG, 0.250″ ID
L4	1 Turn, #26 AWG, 0.240″ ID
L5	3 Turn, #24 AWG, 0.180″ ID
N1, N2	Type N Flange Mounts
R1	5.1 Ω, 1/4 W Chip Resistor
R2	39 Ω Chip Resistor (0805)
R3	1 kΩ, 1/8 W Chip Resistor
R4	33 kΩ, 1/4 W Chip Resistor
Z1	1.000″ x 0.080″ Microstrip
Z2	0.400″ x 0.080″ Microstrip
Z3	0.200″ x 0.080″ Microstrip
Z4	0.200″ x 0.080″ Microstrip
Z5, Z6	0.100″ x 0.223″ Microstrip
Z7	0.160″ x 0.080″ Microstrip
Z8	0.260″ x 0.080″ Microstrip
Z9	0.280″ x 0.080″ Microstrip
Z10	0.270″ x 0.080″ Microstrip
Z11	0.730″ x 0.080″ Microstrip
Board	Glass Teflon®, 31 mils

Figure 1. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS

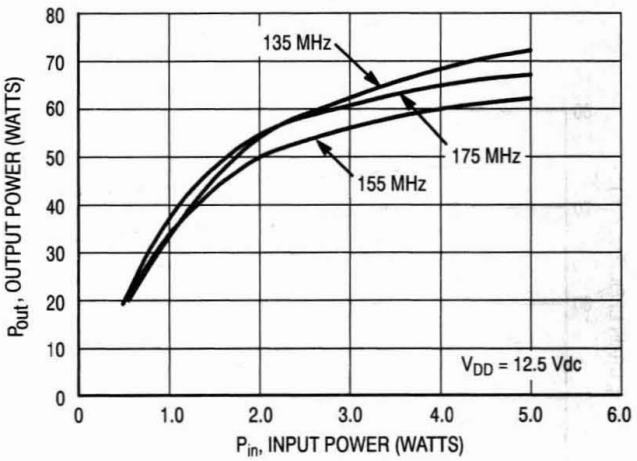


Figure 2. Output Power versus Input Power

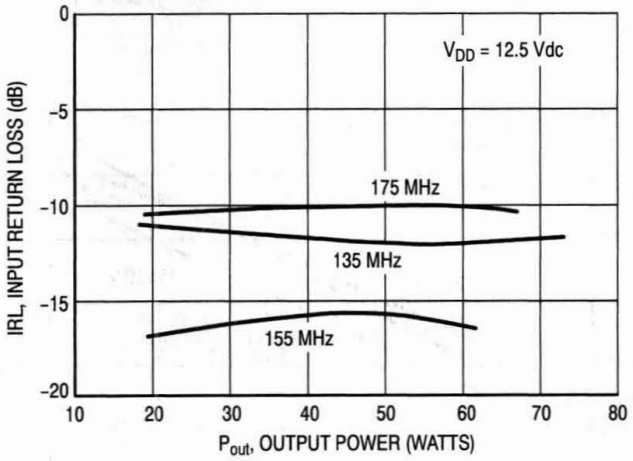


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS

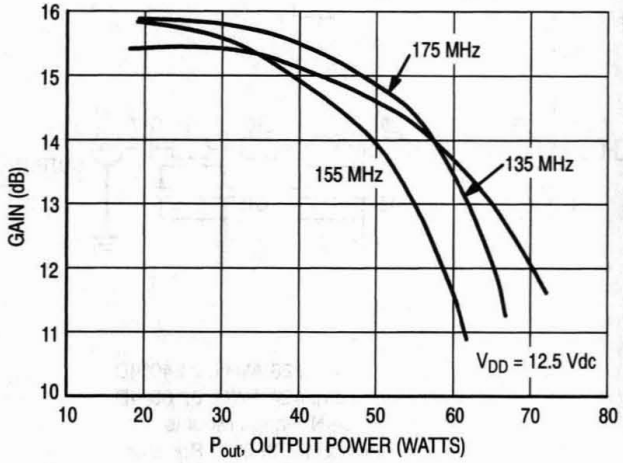


Figure 4. Gain versus Output Power

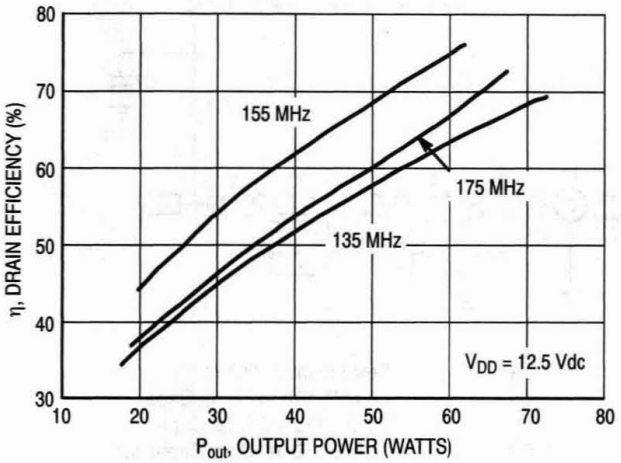


Figure 5. Drain Efficiency versus Output Power

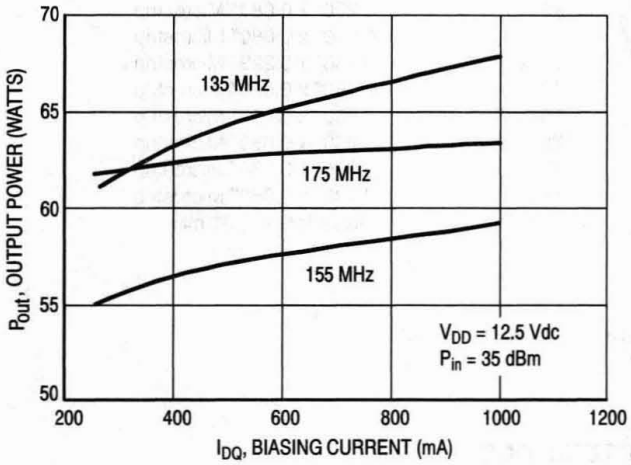


Figure 6. Output Power versus Biasing Current

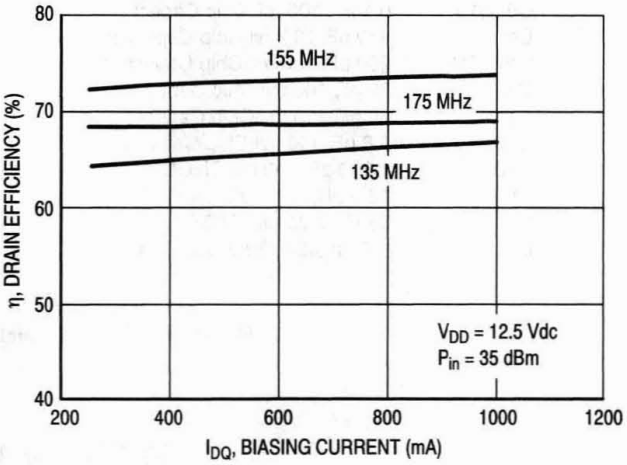


Figure 7. Drain Efficiency versus Biasing Current

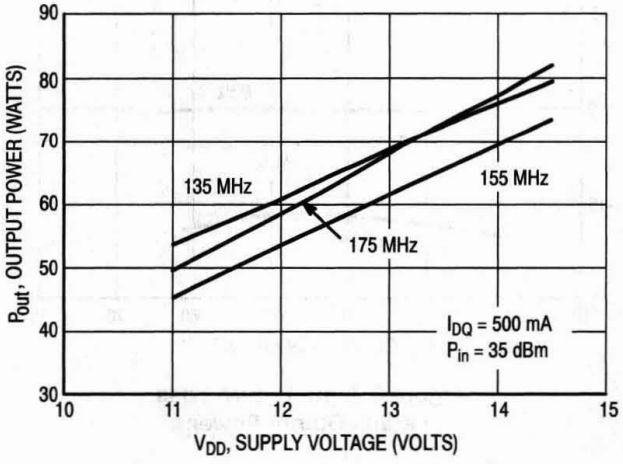


Figure 8. Output Power versus Supply Voltage

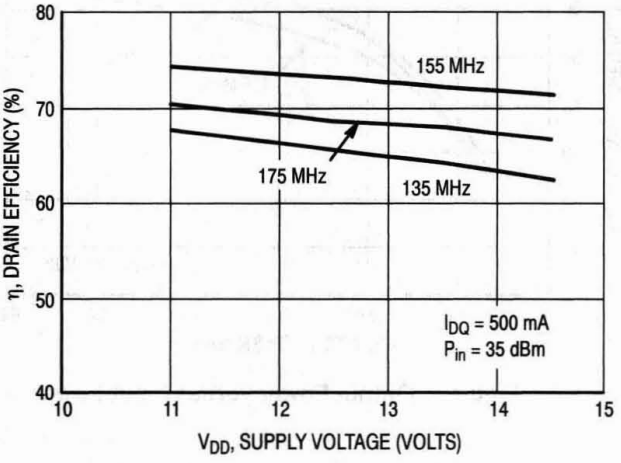
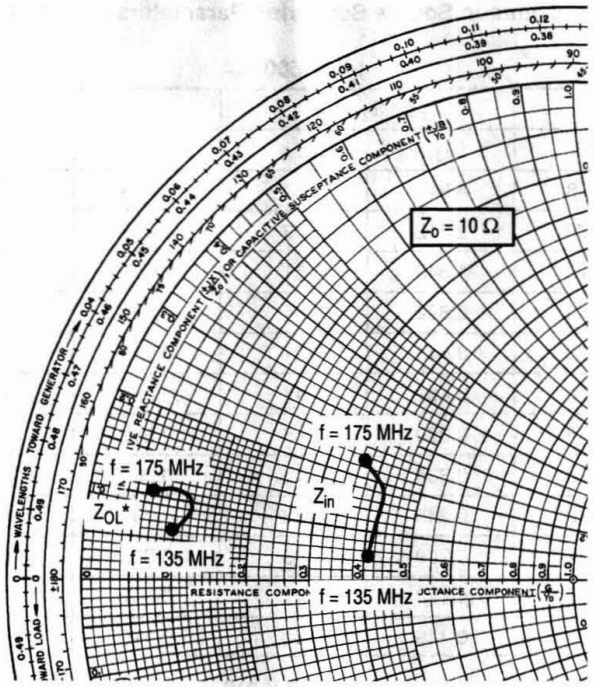


Figure 9. Drain Efficiency versus Supply Voltage



V_{DD} = 12.5 V, I_{DQ} = 500 mA, P_{out} = 50 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	4.1 + j0.5	1.0 + j0.6
155	4.2 + j1.7	1.2 + j.09
175	3.7 + j2.3	0.7 + j1.1

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

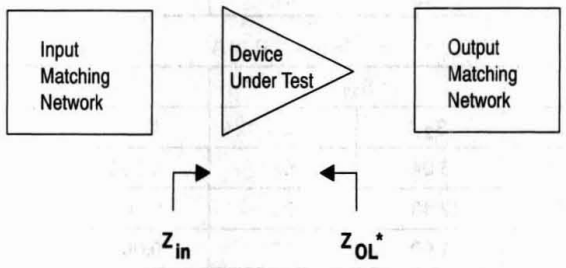


Figure 10. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 12.5 Vdc)

I_{DQ} = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
50	0.93	–178	4.817	80	0.009	–39	0.86	–176
100	0.94	–178	2.212	69	0.009	–3	0.88	–175
150	0.95	–178	1.349	61	0.008	–8	0.90	–174
200	0.95	–178	0.892	54	0.006	–13	0.92	–174
250	0.96	–178	0.648	51	0.005	–7	0.93	–174
300	0.97	–178	0.481	47	0.004	–8	0.95	–174
350	0.97	–178	0.370	46	0.005	4	0.95	–174
400	0.98	–178	0.304	43	0.001	15	0.97	–174
450	0.98	–178	0.245	43	0.005	81	0.97	–174
500	0.98	–178	0.209	43	0.003	84	0.97	–174
550	0.99	–177	0.178	41	0.007	70	0.98	–175
600	0.98	–178	0.149	41	0.010	106	0.96	–175

I_{DQ} = 2.0 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
50	0.93	–177	4.81	80	0.003	–119	0.93	–178
100	0.94	–178	2.20	69	0.006	4	0.93	–178
150	0.95	–178	1.35	61	0.003	–1	0.93	–177
200	0.95	–178	0.89	54	0.004	18	0.93	–176
250	0.96	–178	0.65	51	0.001	28	0.94	–176
300	0.97	–178	0.48	47	0.004	77	0.94	–175
350	0.97	–178	0.37	46	0.006	85	0.95	–175
400	0.98	–178	0.30	43	0.007	53	0.96	–174
450	0.98	–178	0.25	43	0.006	74	0.97	–174
500	0.98	–177	0.21	44	0.006	84	0.97	–174
550	0.99	–177	0.18	41	0.002	106	0.97	–175
600	0.98	–178	0.15	41	0.004	116	0.96	–174

I_{DQ} = 4.0 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
50	0.97	–179	5.04	87	0.002	–116	0.94	–179
100	0.96	–179	2.43	82	0.006	42	0.94	–178
150	0.96	–179	1.60	77	0.004	13	0.94	–177
200	0.96	–179	1.14	74	0.003	43	0.95	–176
250	0.97	–179	0.89	71	0.004	65	0.95	–175
300	0.97	–179	0.71	68	0.006	68	0.95	–175
350	0.97	–179	0.57	67	0.006	74	0.97	–174

Table 1. Common Source Scattering Parameters (V_{DD} = 12.5 Vdc) (continued)

I_{DQ} = 4.0 mA (continued)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
400	0.97	–179	0.49	63	0.005	58	0.97	–173
450	0.98	–178	0.41	63	0.005	73	0.98	–173
500	0.98	–178	0.36	62	0.003	128	0.98	–173
550	0.98	–178	0.32	58	0.004	57	0.99	–174
600	0.98	–178	0.27	58	0.009	83	0.98	–174

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

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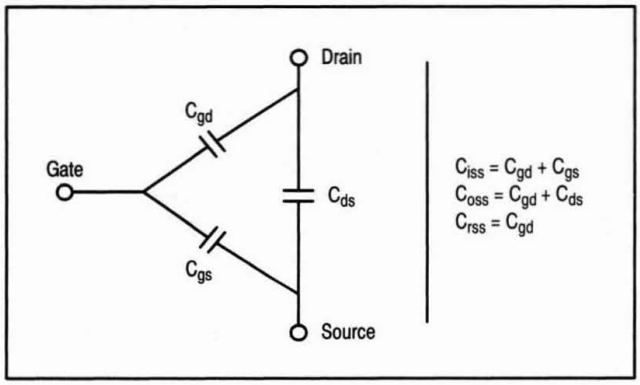
MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

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BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD–1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two–port stability analysis with this device's S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

RF Power Field Effect Transistors

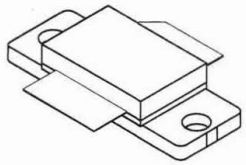
N–Channel Enhancement–Mode Lateral MOSFETs

MRF6522-70
MRF6522-70R3

Designed for GSM 900 frequency band, the high gain and broadband performance of these devices make them ideal for large–signal, common source amplifier applications in 26 volt base station equipment.

- Specified Performance @ Full GSM Band, 921–960 MHz, 26 Volts
  Output Power, P1dB — 80 Watts (Typ)
  Power Gain @ P1dB — 16 dB (Typ)
  Efficiency @ P1dB — 58% (Typ)
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

921 – 960 MHz, 70 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465D–05, STYLE 1
(NI–600)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	7	Adc
Total Device Dissipation @ $T_C \geq 25°C$ Derate above 25°C	P_D	159 0.9	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

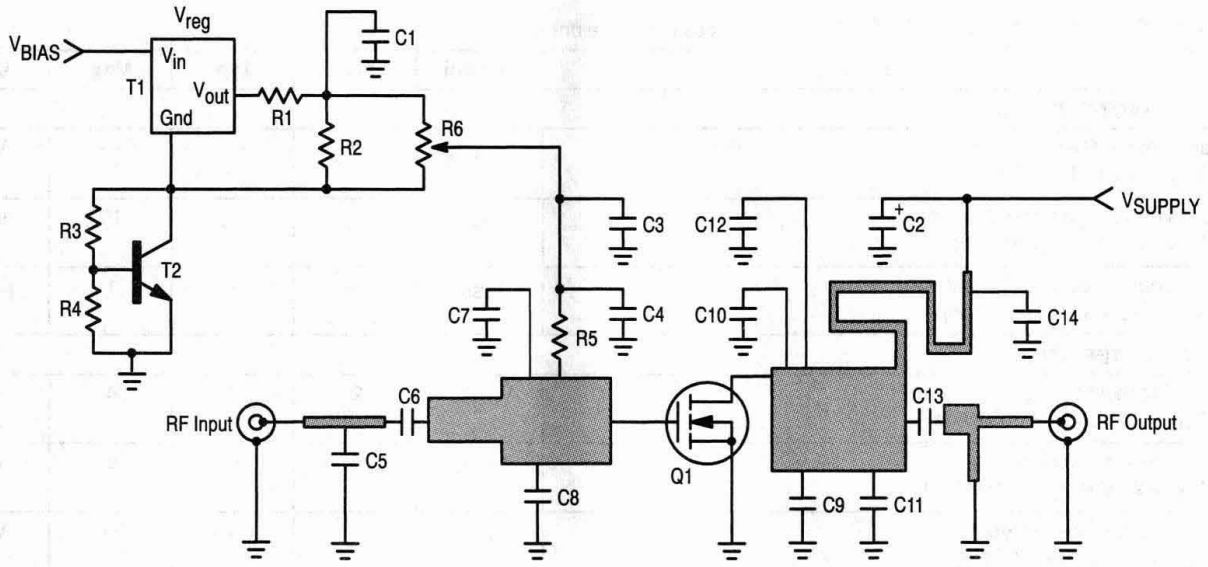
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 400 mAdc)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.15	0.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	2	3	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	130	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	41	47	52	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	2.4	3	3.4	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Output Power (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	P1dB	73	80	—	W
Common–Source Amplifier Power Gain @ P1dB (Min) (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	G_{ps}	14	16	18	dB
Drain Efficiency @ P_{out} = 50 W (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	η_1	47	51	—	%
Drain Efficiency @ P1dB (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	η_2	—	58	—	%
Input Return Loss @ P_{out} = 50 W (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = 921 MHz and 960 MHz f = 940 MHz)	IRL	 — —	 — —	 –10 –15	dB
Output Mismatch Stress (2) (V_{DD} = 26 Vdc, I_{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz, VSWR = 5:1, All Phase Angles)	Ψ	No Degradation In Output Power Before and After Test			

(1) Value excludes the input matching.

(2) To meet application requirements, Motorola test fixtures have been designed to cover full GSM 900 band ensuring batch–to–batch consistency.



C1	1.0 μF Chip Capacitor (0805)
C2	10 μF, 35 Vdc Tantalum Capacitor
C3	100 nF Chip Capacitor
C4, C6, C14	22 pF Chip Capacitors, ACCU–P (0805)
C5	2.7 pF Chip Capacitor, ACCU–P (0805)
C7, C8, C13	4.7 pF Chip Capacitors, ACCU–P (0805)
C9, C10	8.2 pF Chip Capacitors, ACCU–P (0805)
C11, C12	2.2 pF Chip Capacitors, ACCU–P (0805)
R1	10 Ω Chip Resistor (0805)
R2	1.0 kΩ Chip Resistor (0805)
R3	1.2 kΩ Chip Resistor (0805)
R4	2.2 kΩ Chip Resistor (0805)
R5	220 Ω Chip Resistor (0805)
R6	5.0 kΩ SMD Potentiometer
T1	LP2951 Micro–8
T2	BC847 SOT–23
SUBSTRATE	GI180 0.8 mm

Figure 1. MRF6522–70 Test Circuit Schematic

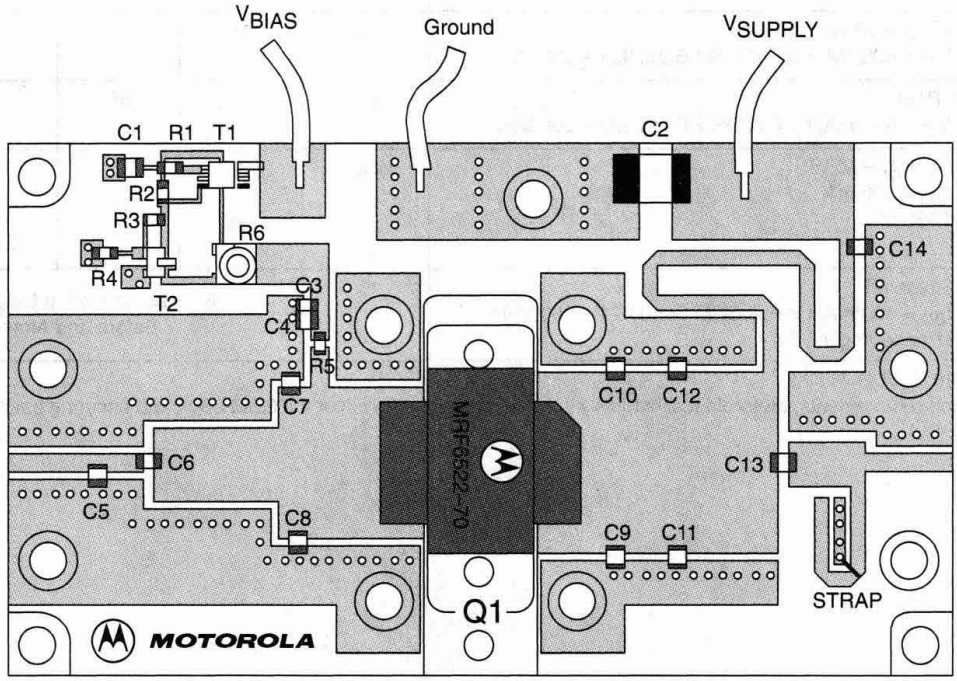


Figure 2. MRF6522–70 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

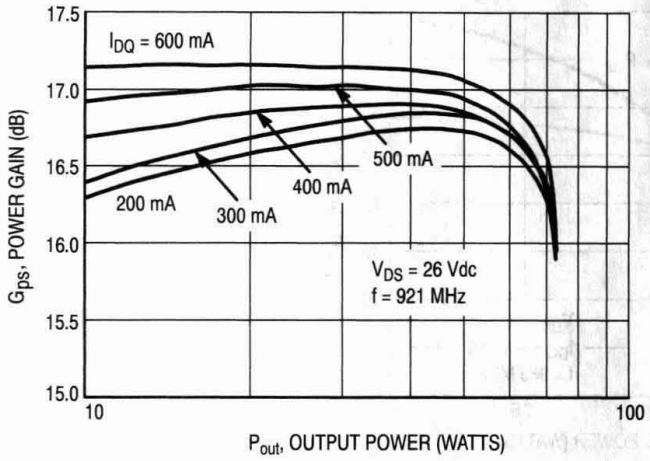


Figure 3. Power Gain versus Output Power

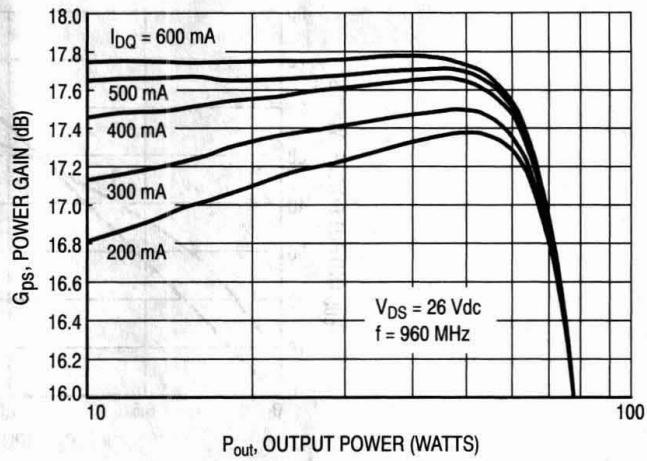


Figure 4. Power Gain versus Output Power

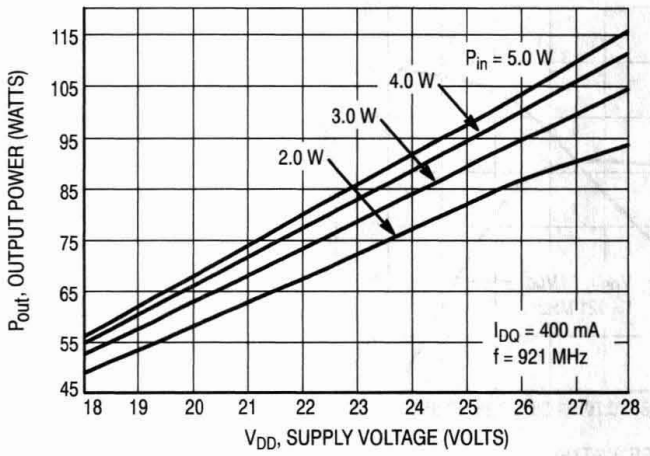


Figure 5. Output Power versus Supply Voltage

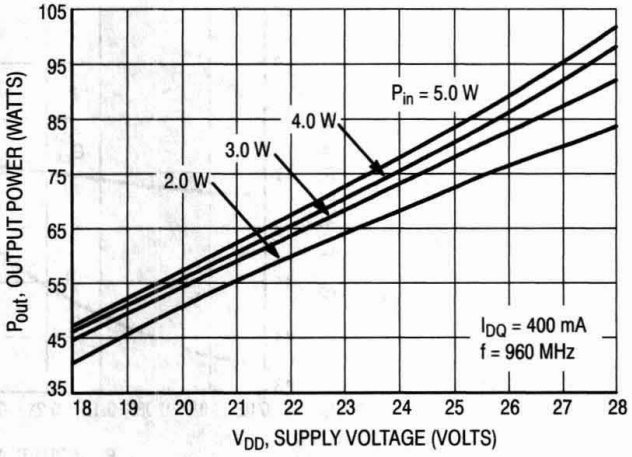


Figure 6. Output Power versus Supply Voltage

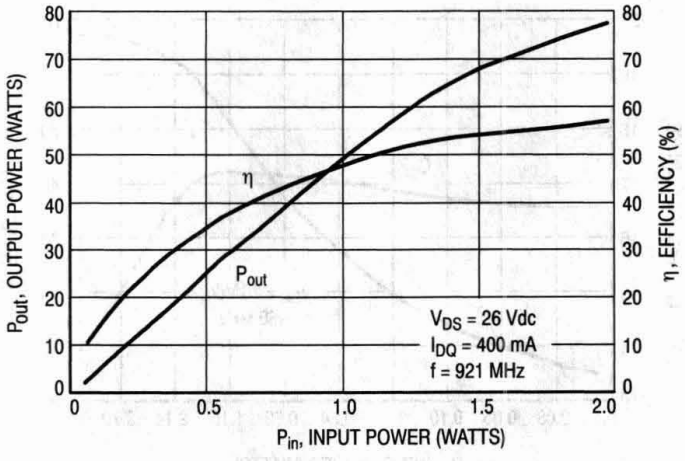


Figure 7. Efficiency and Output Power versus Input Power

TYPICAL CHARACTERISTICS

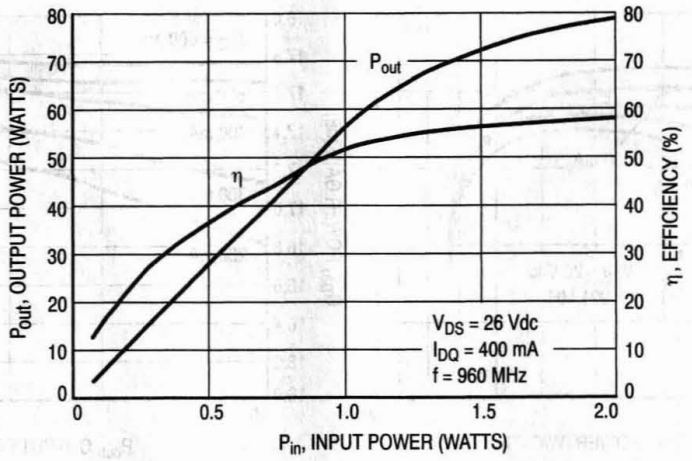


Figure 8. Efficiency and Output Power versus Input Power

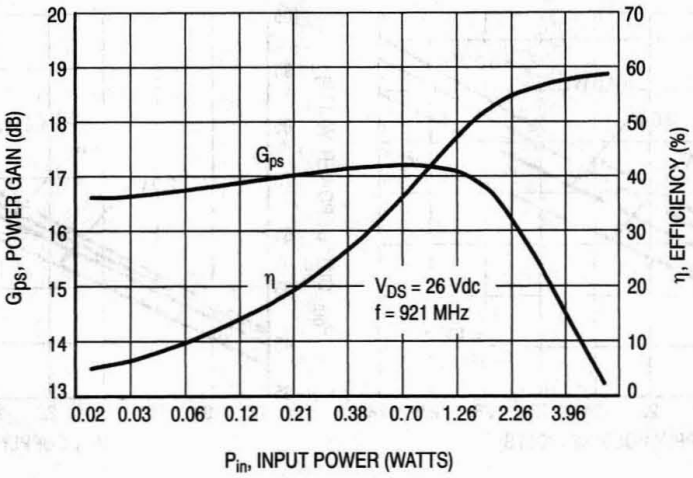


Figure 9. Power Gain and Efficiency versus Input Power

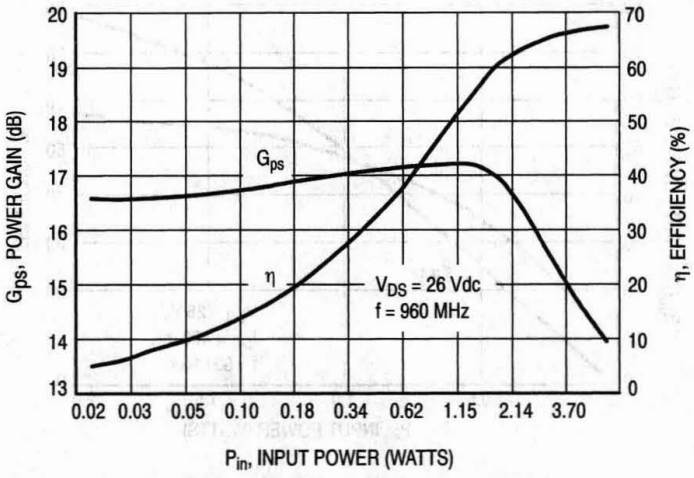


Figure 10. Power Gain and Efficiency versus Input Power

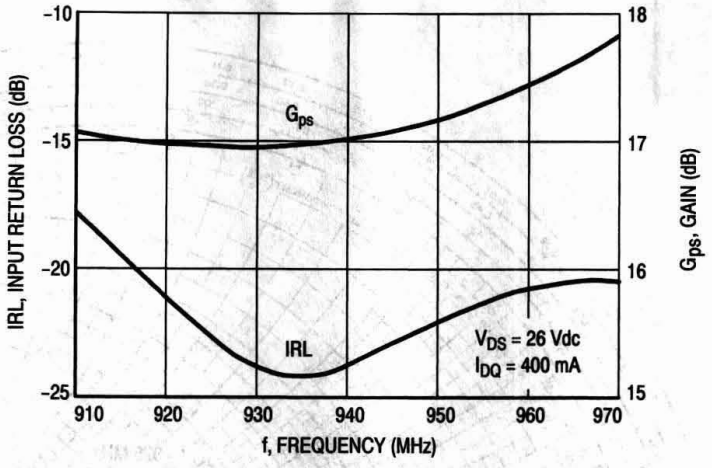
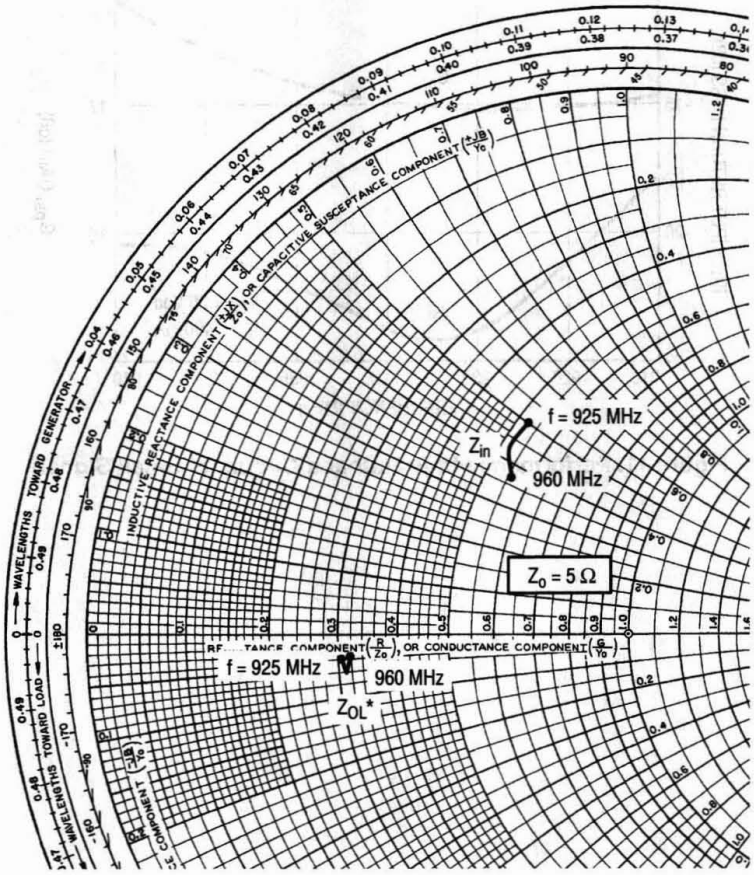


Figure 11. Performance in Broadband Circuit (at Small Signal)



V_{SUPPLY} = 26 Vdc, I_{BIAS} = 400 mA, CW = Room Temperature

f MHz	Z_{in} Ω	Z_{OL}* Ω
925	2.65 + j2.53	1.62 – j0.2
940	2.67 + j2.14	1.56 – j0.34
960	2.85 + j1.87	1.55 – j0.2

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

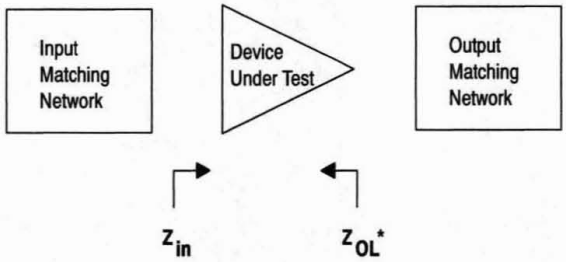


Figure 12. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistor Array

N–Channel Enhancement–Mode Lateral MOSFET

MRF9002R2

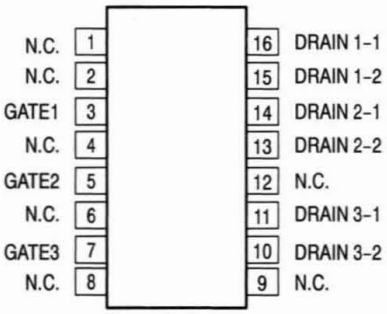
1.0 GHz, 2 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

Designed for broadband commercial and industrial applications with frequencies to 1.0 GHz. The high gain and broadband performance of this device make it ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Guaranteed Performance at 960 MHz, 26 Volts
  Output Power — 2 Watts Per Transistor
  Power Gain — 15 dB
  Efficiency — 35%
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 960 MHz, 2 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

CASE 978–03
(PFP–16)

PIN CONNECTIONS



(Top View)

NOTE: Exposed backside flag is source terminal for transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Dissipation Per Transistor @ T_C = 25°C	P_D	4	Watts
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case, Single Transistor	$R_{\theta JC}$	12	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 20 μAdc)	$V_{GS(th)}$	2.4	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 25 mAdc)	$V_{GS(Q)}$	3	—	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.1 Adc)	$V_{DS(on)}$	—	0.3	—	Vdc
FUNCTIONAL TESTS (Per Transistor in Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 25 mA, f = 960.0 MHz)	G_{ps}	15	16	—	dB
Drain Efficiency @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 25 mA, f = 960.0 MHz)	η	35	50	—	%
Input Return Loss @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 25 mA, f = 960.0 MHz)	IRL	—	–15	–9	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 25 mA, f = 960.0 MHz)	P_{1dB}	2.5	3	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 2 W CW, I_{DQ} = 25 mA, f = 960.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			

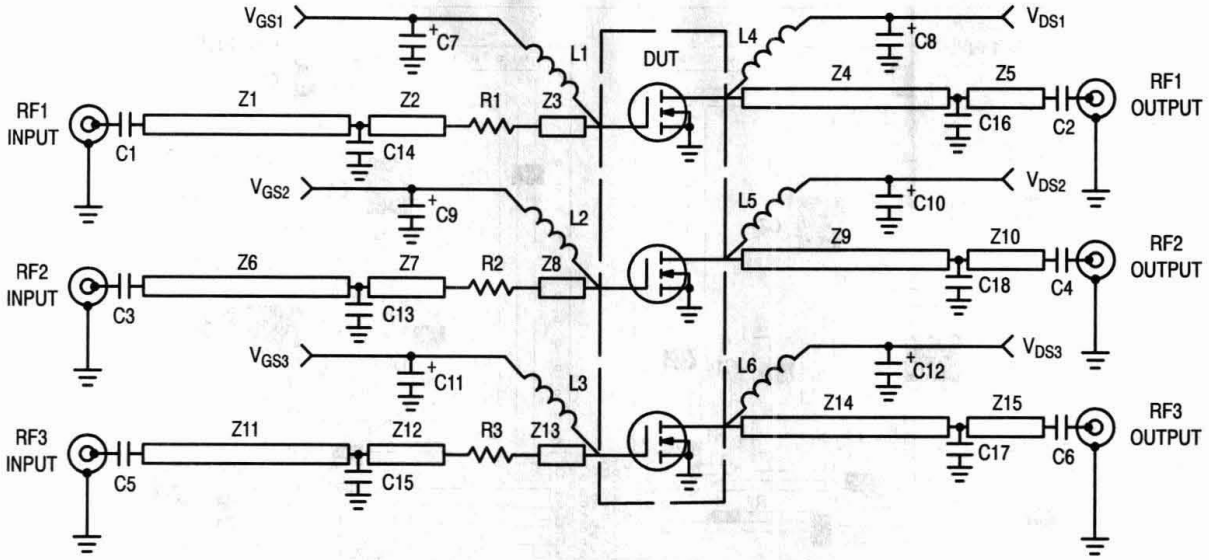


Figure 1. MRF9002R2 Broadband Test Circuit Schematic

Table 1. MRF9002R2 Broadband Test Circuit Component Designations and Values

Designators	Description
C1–C6	33 pF Chip Capacitors (0805)
C7–C12	1.0 µF, 35 V Tantalum Capacitors, B Case, Kemet
C13	8.2 pF Chip Capacitor (0805)
C14, C15	10 pF Chip Capacitors (0805)
C16, C17	2.7 pF Chip Capacitors (0805)
C18	3.3 pF Chip Capacitor (0805)
L1–L6	12 nH Chip Inductors (0805)
R1–R3	0 Ω Chip Resistors (0805)
Z1, Z11	1.16 x 28.5 mm Microstrip
Z2, Z7, Z12	0.65 x 5.6 mm Microstrip
Z3, Z8, Z13	0.65 x 2.6 mm Microstrip
Z4, Z14	1.16 x 19.5 mm Microstrip
Z5, Z15	1.16 x 17.5 mm Microstrip
Z6	1.16 x 12.9 mm Microstrip
Z9	1.16 x 27.2 mm Microstrip
Z10	1.16 x 4.3 mm Microstrip
PCB	Etched Circuit Board
Raw PCB Material	Rogers RO4350, 0.020″, 2.5″, x 2.5″, ε_r = 3.5
Bedstead	Copper Heatsink

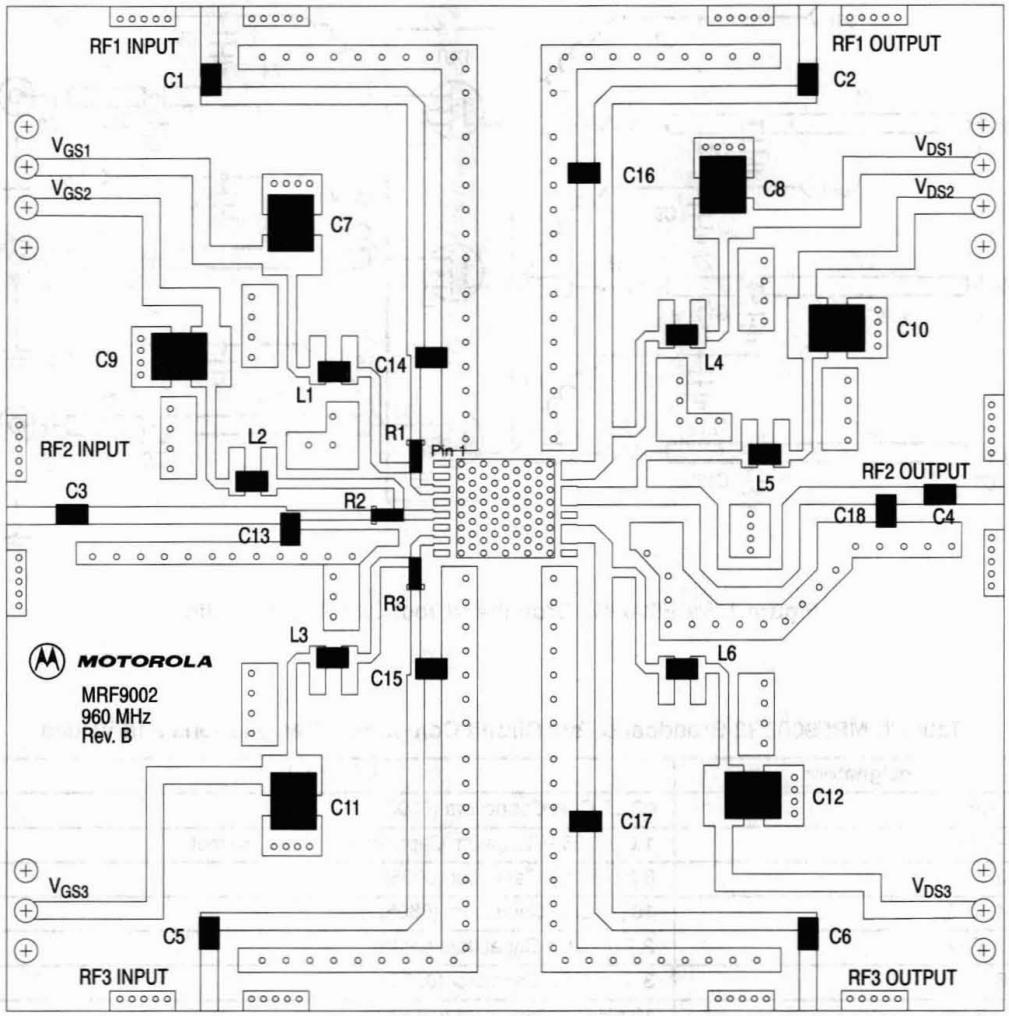


Figure 2. MRF9002R2 Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

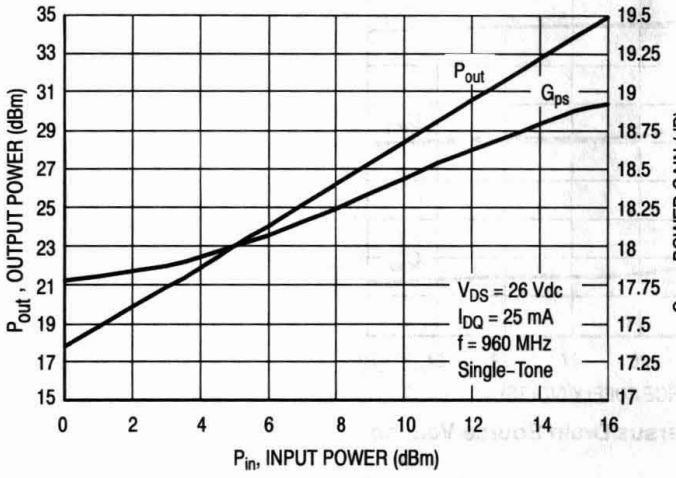


Figure 3. Output Power and Power Gain versus Input Power

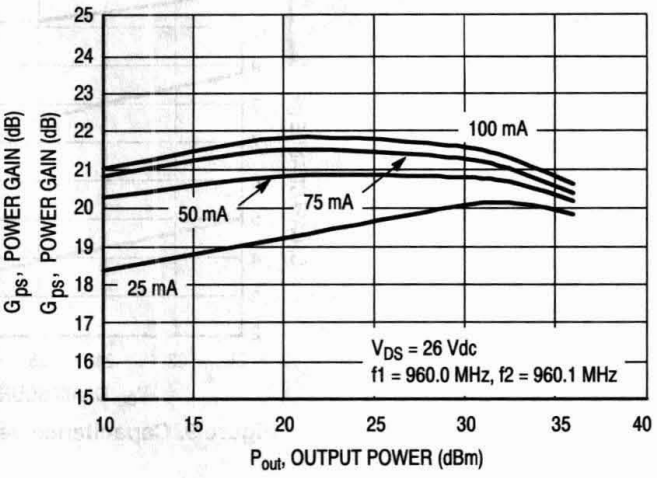


Figure 4. Power Gain versus Output Power

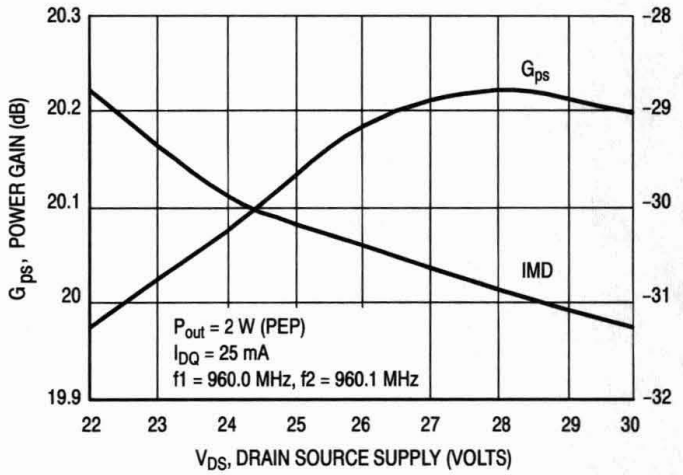


Figure 5. Power Gain and Intermodulation Distortion versus Supply Voltage

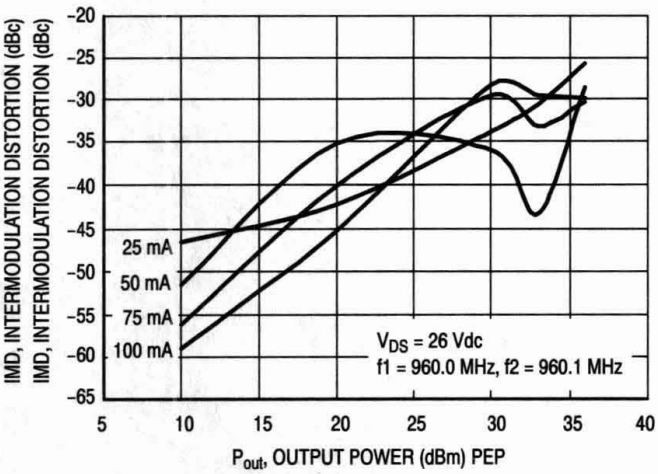


Figure 6. Intermodulation Distortion versus Output Power

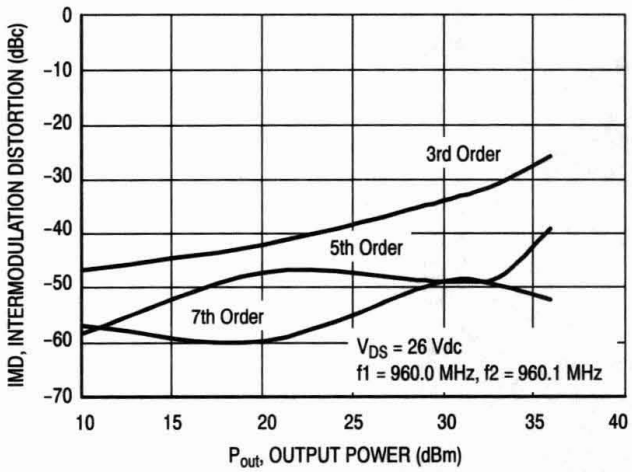


Figure 7. Intermodulation Distortion Products versus Output Power

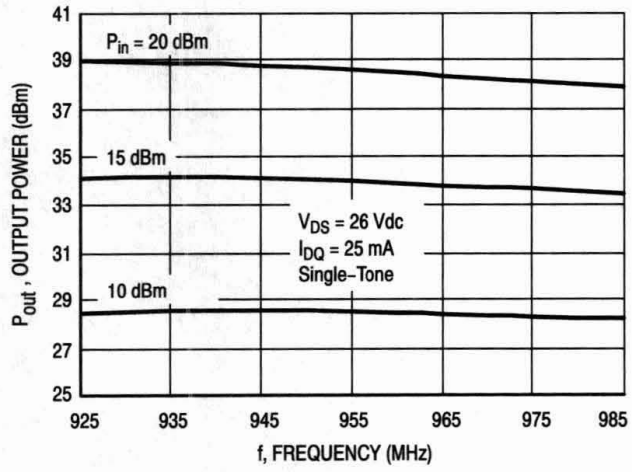


Figure 8. Output Power versus Frequency

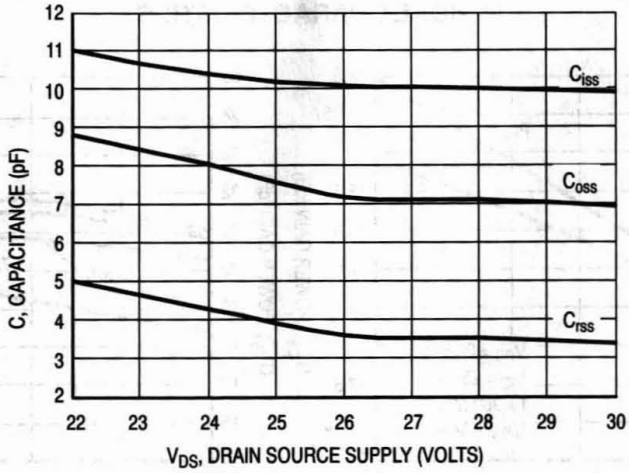
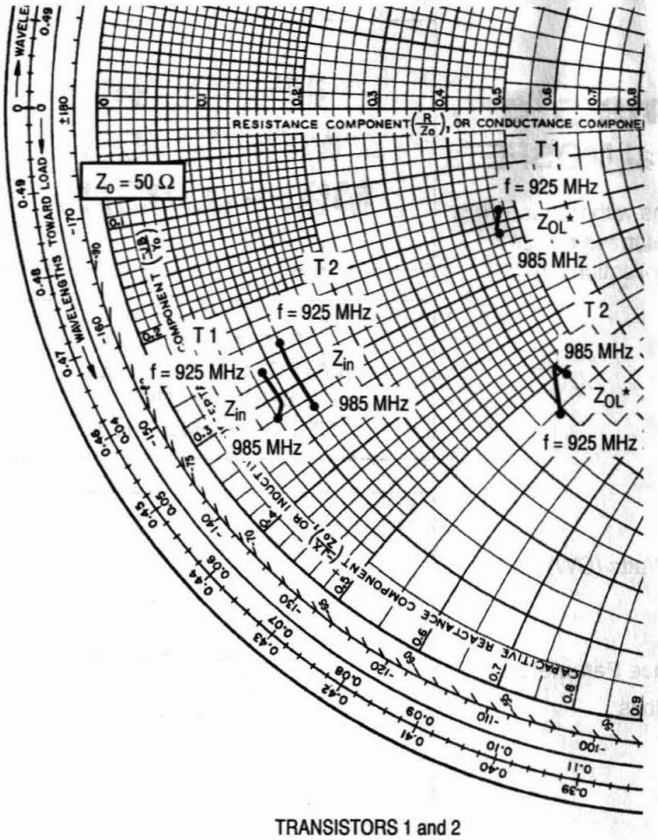
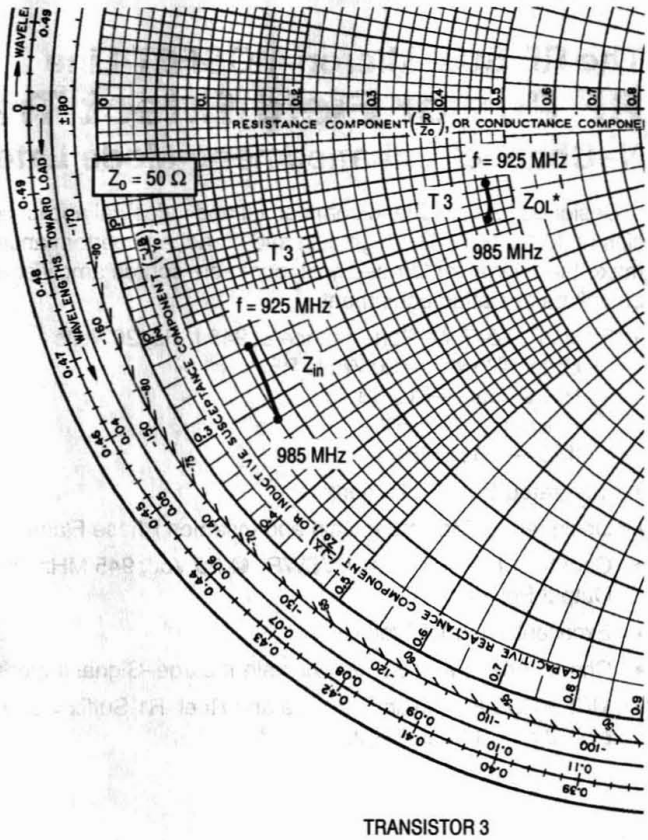


Figure 9. Capacitance versus Drain Source Voltage



TRANSISTORS 1 and 2



TRANSISTOR 3

V_{DD} = 26 V, I_{DQ} = 25 mA, P_{out} = 2 W PEP

f MHz	Z_{in} Ω	Z_{OL}^* Ω
925	4.5 – j13.3	23.4 – j9.2
960	4.3 – j15.3	23.2 – j10.4
985	4.1 – j15.8	23.0 – j11.1

Transistor 1

V_{DD} = 26 V, I_{DQ} = 25 mA, P_{out} = 2 W PEP

f MHz	Z_{in} Ω	Z_{OL}^* Ω
925	6.0 – j12.3	19.7 – j27.8
960	5.9 – j14.3	22.0 – j23.9
985	5.8 – j16.5	22.5 – j25.4

Transistor 2

V_{DD} = 26 V, I_{DQ} = 25 mA, P_{out} = 2 W PEP

f MHz	Z_{in} Ω	Z_{OL}^* Ω
925	4.3 – j12.2	23.1 – j6.5
960	4.3 – j14.0	22.8 – j8.4
985	3.9 – j15.9	22.6 – j9.3

Transistor 3

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

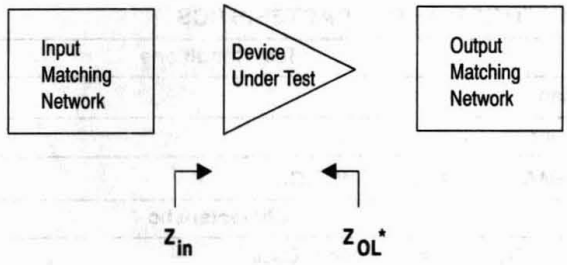


Figure 10. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

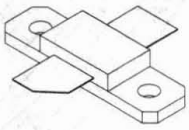
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9030
MRF9030S
MRF9030SR1

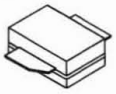
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical Two–Tone Performance at 945 MHz, 26 Volts
  Output Power — 30 Watts PEP
  Power Gain — 19 dB
  Efficiency — 41.5%
  IMD — –32.5 dBc
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 945 MHz, 30 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- MRF9030S Is Available in Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.

945 MHz, 30 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B–05, STYLE 1
(NI–360)
(MRF9030)



CASE 360C–05, STYLE 1
(NI–360S)
(MRF9030S)

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain–Source Voltage		V_{DSS}	68	Vdc
Gate–Source Voltage		V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	MRF9030	P_D	92 0.53	Watts W/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	MRF9030S	P_D	117 0.67	Watts W/°C
Storage Temperature Range		T_{stg}	–65 to +200	°C
Operating Junction Temperature		T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case	MRF9030 MRF9030S	$R_{\theta JC}$	1.9 1.5	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

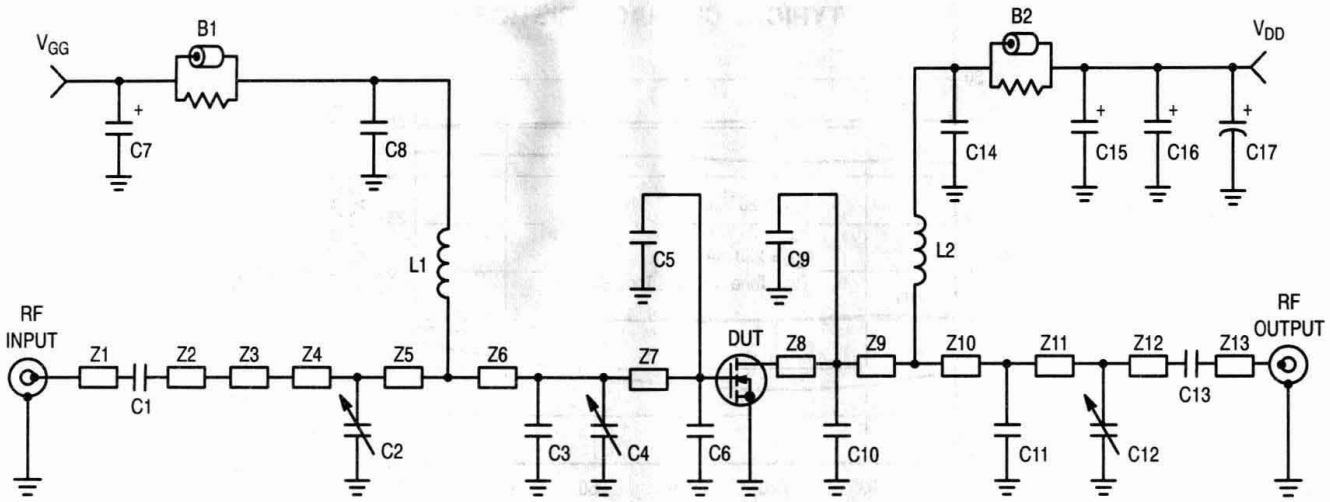
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 250 mAdc)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.7 Adc)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	3	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	49.5	—	pF
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	26.5	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1	—	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G_{ps}	18	19	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	37	41.5	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	–32.5	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	—	–15.5	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	G_{ps}	—	19	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	η	—	41.5	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	—	–33	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	—	–14	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 250 mA, f1 = 945.0 MHz)	P_{1dB}	—	30	—	W
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 250 mA, f1 = 945.0 MHz)	G_{ps}	—	19	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 250 mA, f1 = 945.0 MHz)	η	—	60	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 250 mA, f = 945.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			



B1	Short Ferrite Bead	Z3	0.500″ x 0.100″ Microstrip
B2	Long Ferrite Bead	Z4	0.215″ x 0.270″ Microstrip
C1, C8, C13, C14	47 pF Chip Capacitors, B Case	Z5	0.315″ x 0.270″ Microstrip
C2, C4	0.8 pF to 8.0 pF Trim Capacitors	Z6	0.160″ x 0.270″ x 0.520″, Taper
C3	3.9 pF Chip Capacitor, B Case	Z7	0.285″ x 0.520″ Microstrip
C5, C6	7.5 pF Chip Capacitors, B Case	Z8	0.140″ x 0.270″ Microstrip
C7, C15, C16	10 μF, 35 V Tantalum Capacitors	Z9	0.450″ x 0.270″ Microstrip
C9, C10	10 pF Chip Capacitors, B Case	Z10	0.250″ x 0.060″ Microstrip
C11	9.1 pF Chip Capacitor, B Case	Z11	0.720″ x 0.060″ Microstrip
C12	0.6 pF to 4.5 pF Trim Capacitor	Z12	0.490″ x 0.060″ Microstrip
C17	220 μF, 50 V Electrolytic Capacitor	Z13	0.290″ x 0.060″ Microstrip
L1, L2	12.5 nH Surface Mount Inductors	Board	Taconic RF–35–0300,
Z1	0.260″ x 0.060″ Microstrip		(ε_r = 3.5) CAX1/CAX1
Z2	0.240″ x 0.060″ Microstrip		

Figure 1. 945 MHz Broadband Test Circuit Schematic

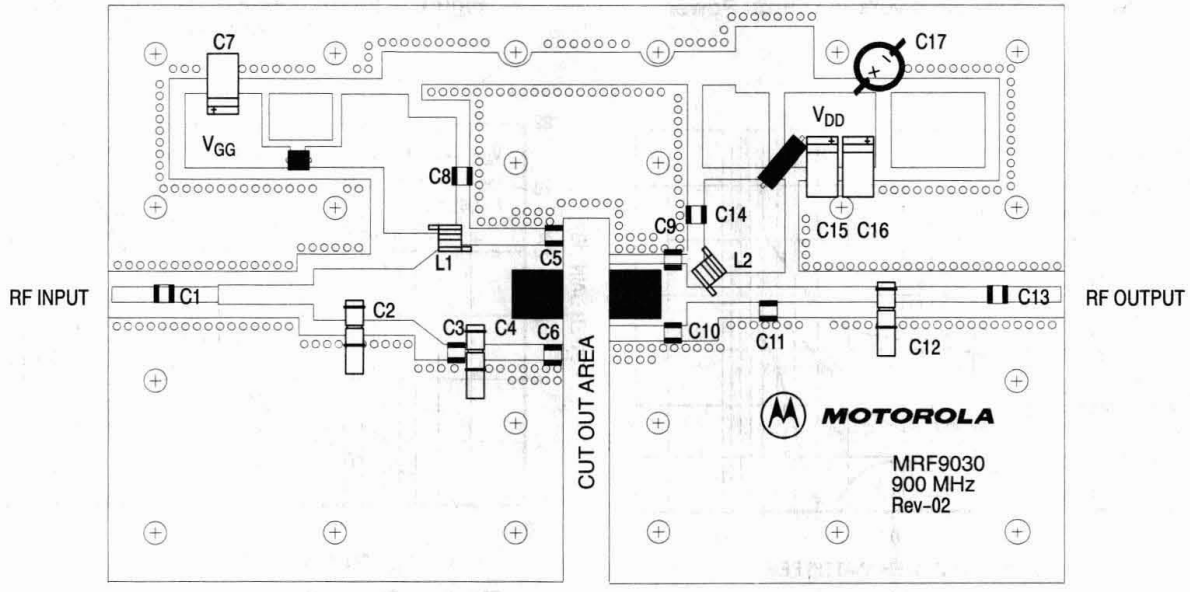


Figure 2. 945 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

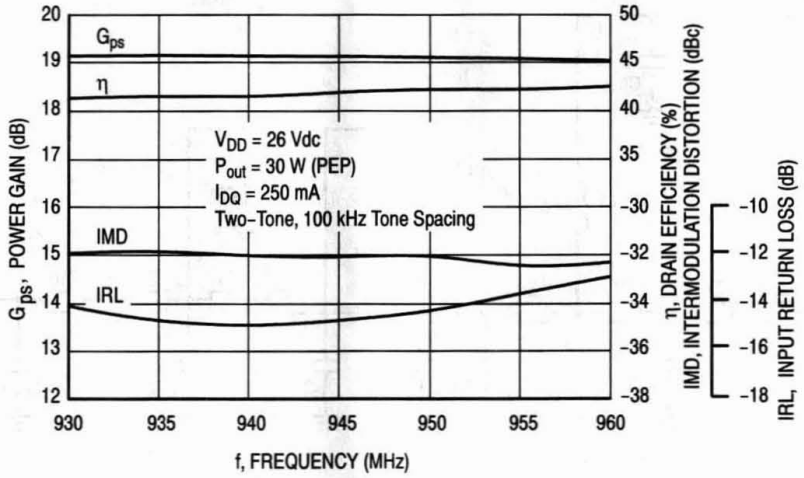


Figure 3. Class AB Broadband Circuit Performance

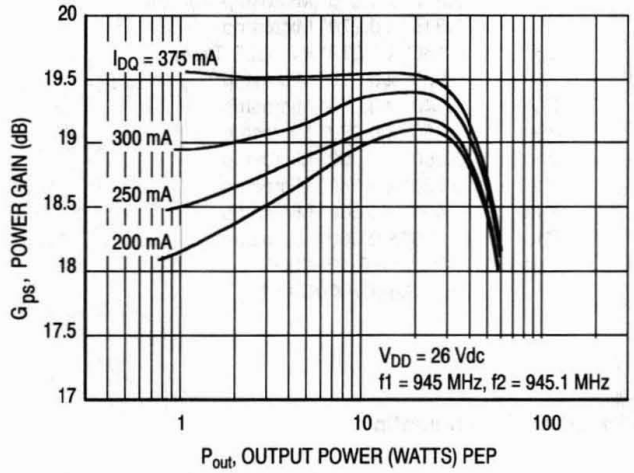


Figure 4. Power Gain versus Output Power

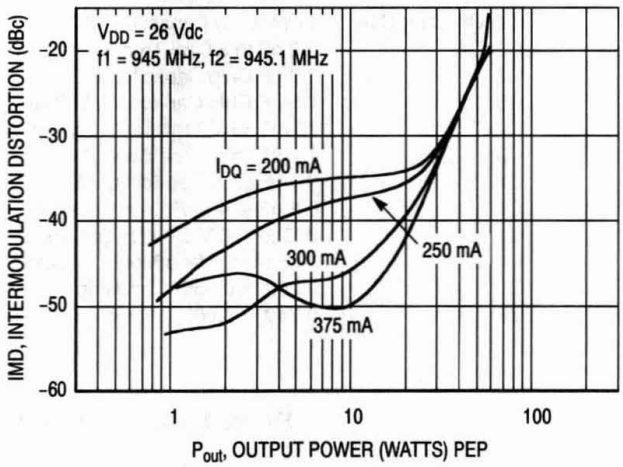


Figure 5. Intermodulation Distortion versus Output Power

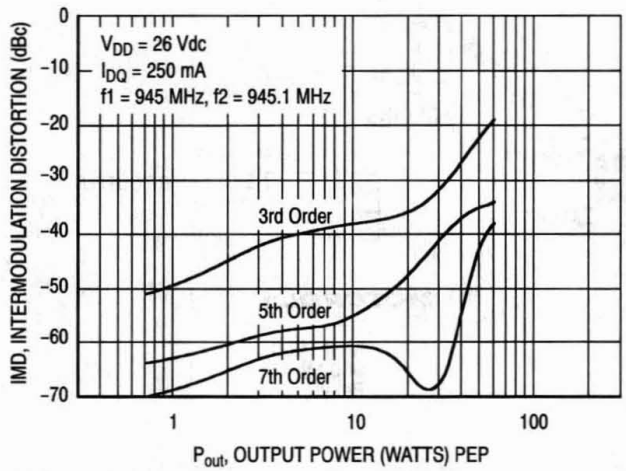


Figure 6. Intermodulation Distortion Products versus Output Power

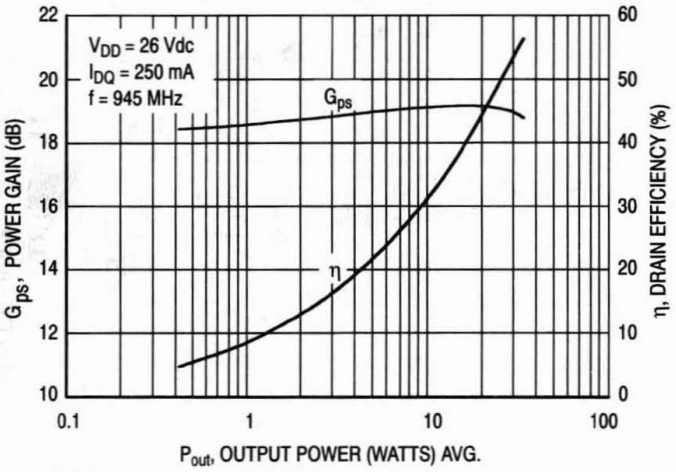


Figure 7. Power Gain and Efficiency versus Output Power

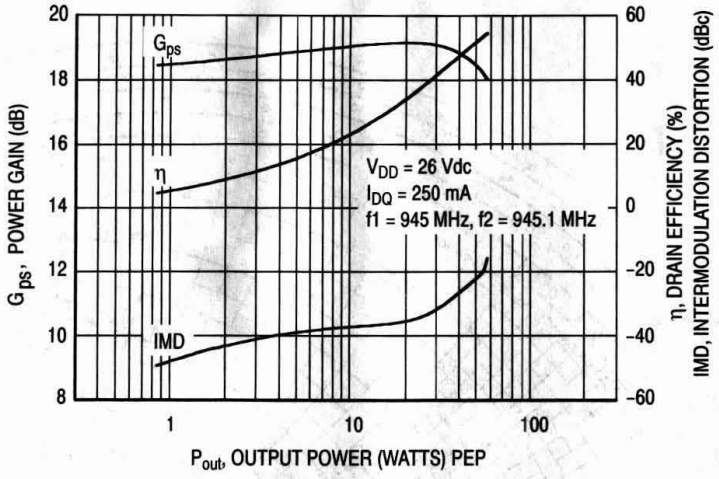
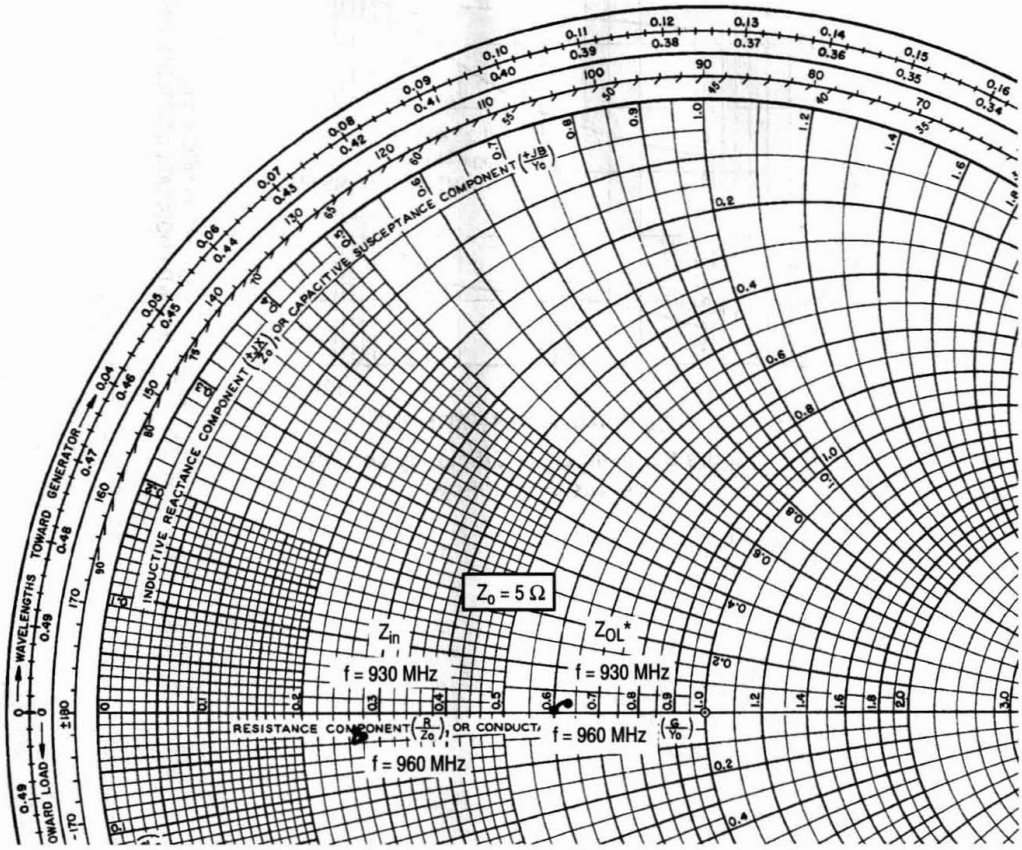


Figure 8. Power Gain, Efficiency and IMD versus Output Power



V_{DD} = 26 V, I_{DQ} = 250 mA, P_{out} = 30 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
930	1.34 – j0.1	3.175 + j0.09
945	1.36 – j0.2	3.1 + j0.08
960	1.4 – j0.14	3.0 + j0.05

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

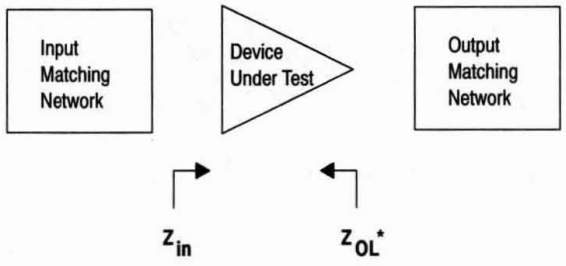


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistor

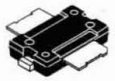
N–Channel Enhancement–Mode Lateral MOSFET

MRF9030MR1

Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of this device make it ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical Performance at 945 MHz, 26 Volts
  Output Power — 30 Watts PEP
  Power Gain — 19.2 dB
  Efficiency — 41% (Two Tone)
  IMD — –31.2 dBc
- Integrated ESD Protection
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 945 MHz, 30 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Moisture Sensitivity Level 3
- Available in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

945 MHz, 30 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET



CASE 1265–07, STYLE 1
(TO–270)
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	139 0.93	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	175	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

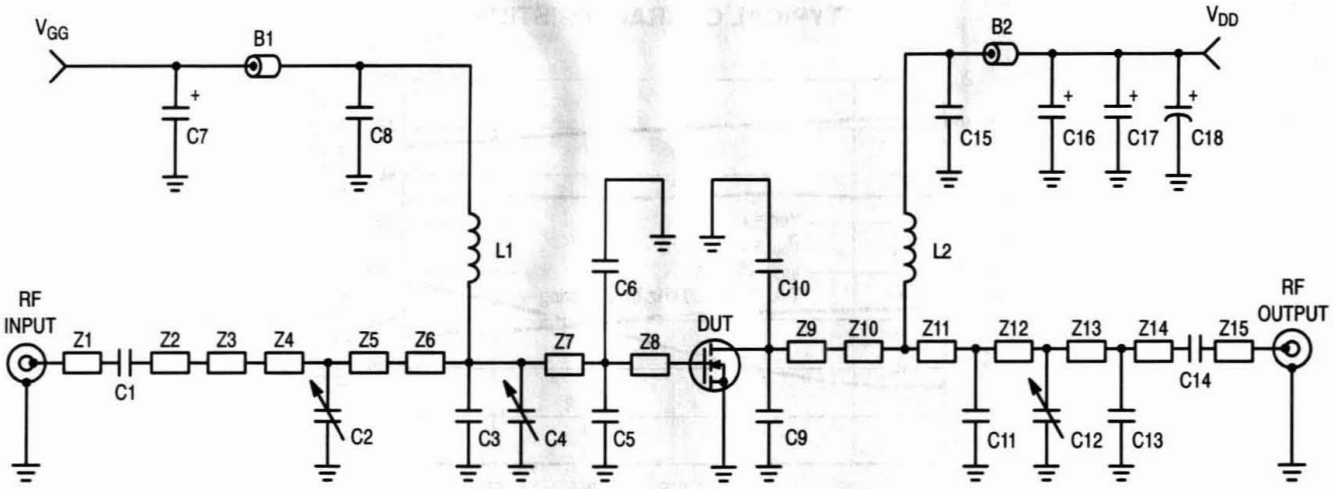
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.08	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 250 mAdc)	$V_{GS(Q)}$	3	3.8	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.7 Adc)	$V_{DS(on)}$	—	0.23	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	2.7	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	49	—	pF
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G_{ps}	18	19.2	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	37	41	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	–31.2	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	—	–13	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	G_{ps}	—	19.6	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	η	—	41	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	—	–13	—	dB



B1	Short Ferrite Bead	Z4	0.220″ x 0.270″ Microstrip
B2	Long Ferrite Bead	Z5	0.310″ x 0.270″ Microstrip
C1, C8, C14, C15	47 pF Chip Capacitors, B Case	Z6	0.270″ x 0.270″ x 0.300″, Taper
C2, C4, C12	0.8 – 8.0 pF Trim Capacitors	Z7	0.330″ x 0.530″ Microstrip
C5, C6	6.8 pF Chip Capacitors, B Case	Z8	0.110″ x 0.530″ Microstrip
C9, C10	10 pF Chip Capacitors, B Case	Z9	0.500″ x 0.270″ Microstrip
C3, C11	3.9 pF Chip Capacitor, B Case	Z10	0.240″ x 0.270″ x 0.060″ Microstrip
C7, C16, C17	10 μF, 35 V Tantalum Chip Capacitors	Z11	0.320″ x 0.060″ Microstrip
C13	1.8 pF Chip Capacitor, B Case	Z12	0.800″ x 0.060″ Microstrip
C18	220 μF, 50 V Electrolytic Capacitor	Z13	0.310″ x 0.060″ Microstrip
L1, L2	12.5 nH Surface Mount Inductors	Z14	0.400″ x 0.060″ Microstrip
Z1	0.320″ x 0.060″ Microstrip	Z15	0.380″ x 0.060″ Microstrip
Z2	0.290″ x 0.060″ Microstrip	Board	Taconic RF–35–0300, (ε_r = 2.55)
Z3	0.500″ x 0.100″ Microstrip		

Figure 1. 930–960 MHz Broadband Test Circuit Schematic

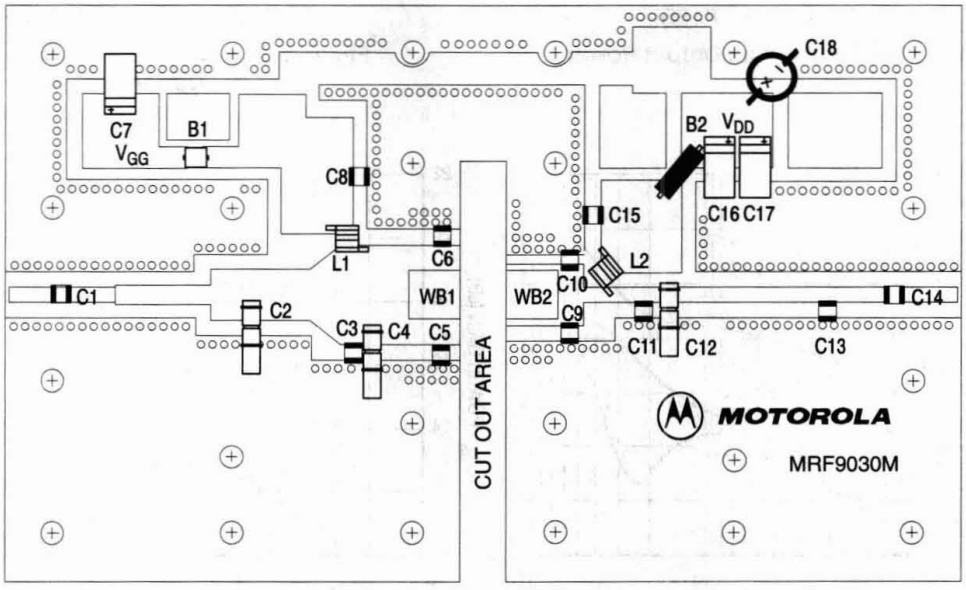


Figure 2. 930–960 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

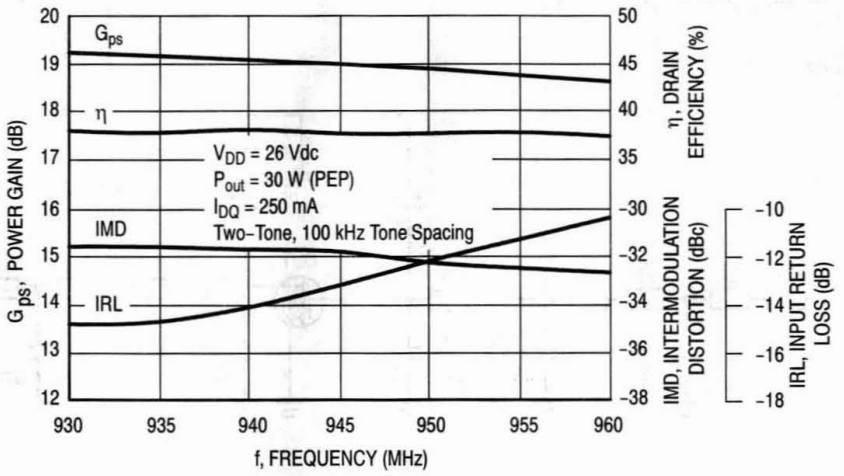


Figure 3. Class AB Broadband Circuit Performance

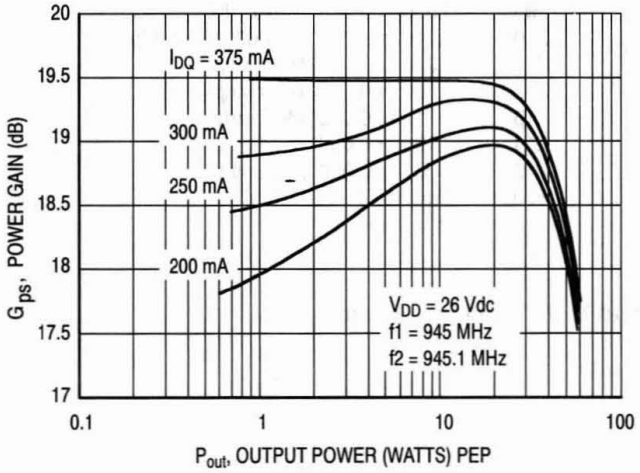


Figure 4. Power Gain versus Output Power

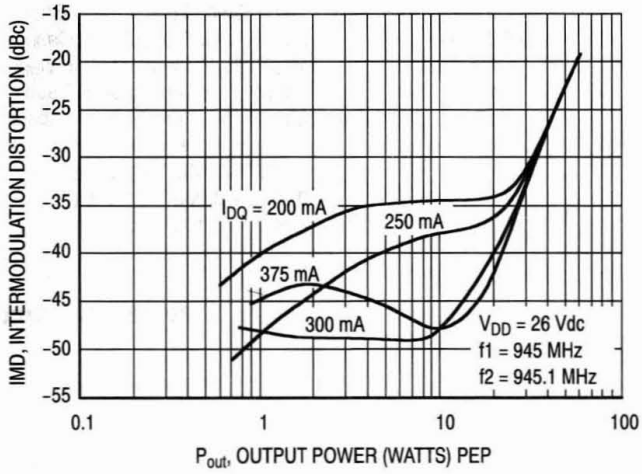


Figure 5. Intermodulation Distortion versus Output Power

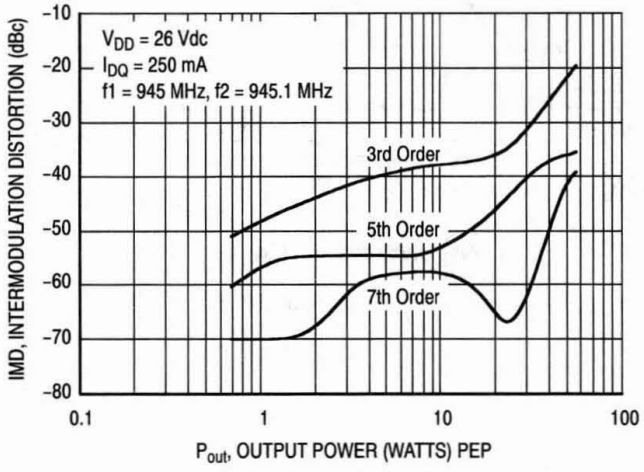


Figure 6. Intermodulation Distortion Products versus Output Power

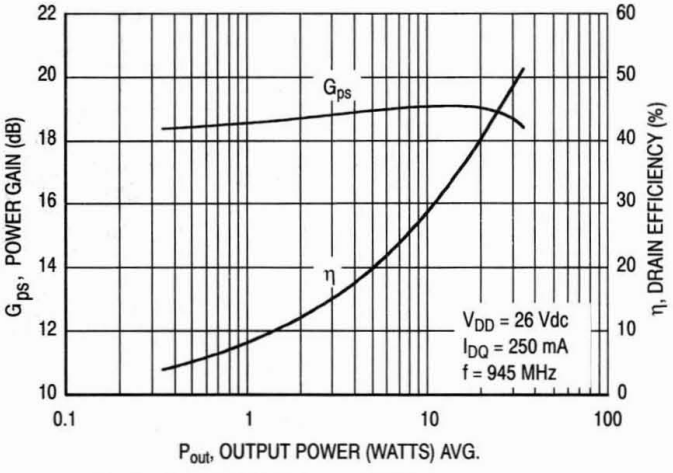


Figure 7. Power Gain and Efficiency versus Output Power

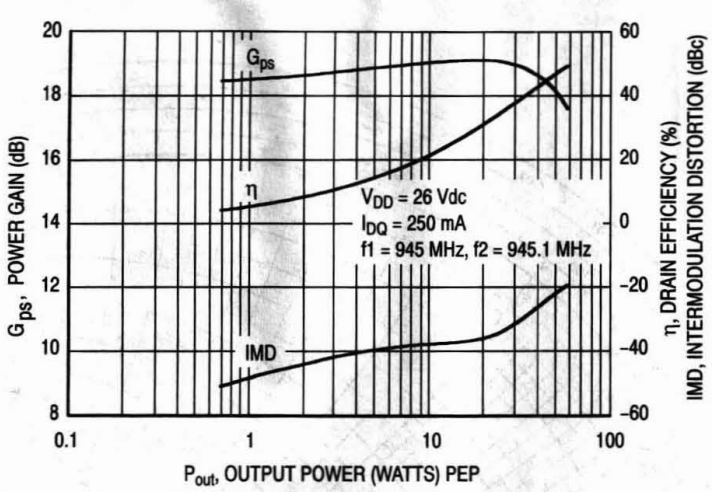
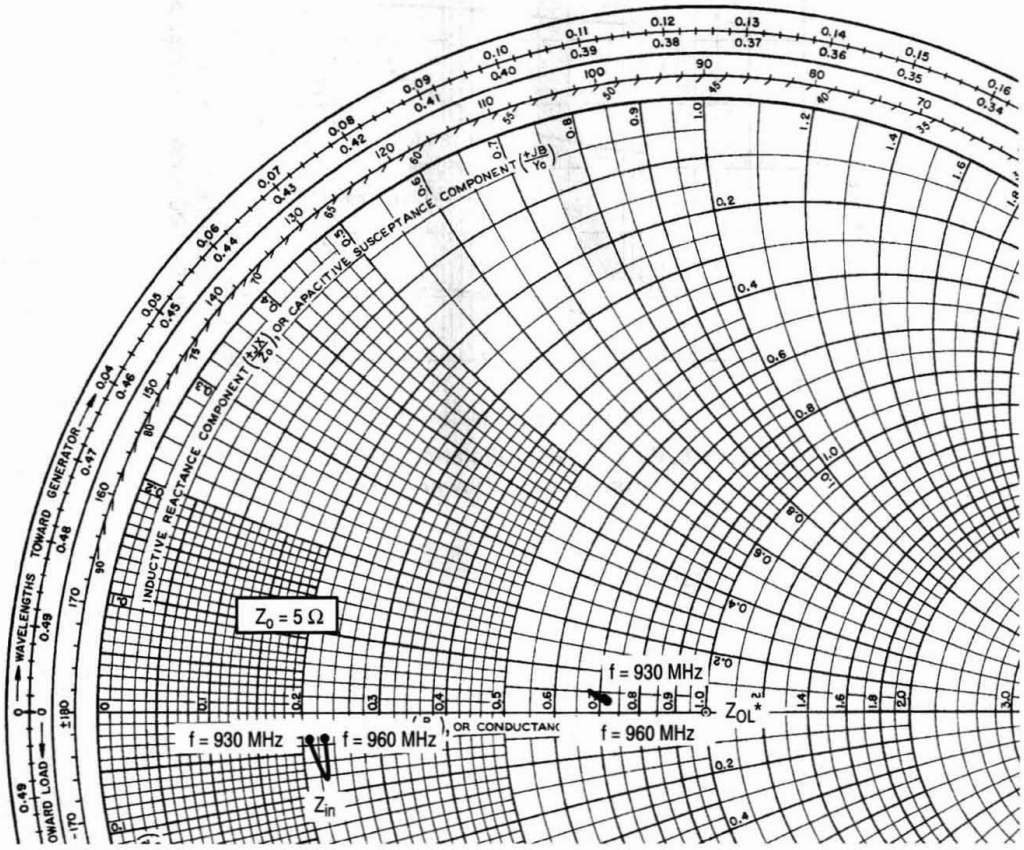


Figure 8. Power Gain, Efficiency and IMD versus Output Power



V_{DD} = 26 V, I_{DQ} = 250 mA, P_{out} = 30 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	1.07 – j0.160	3.53 + j0.20
945	1.14 – j0.385	3.41 + j0.24
960	1.17 – j0.170	3.60 + j0.17

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

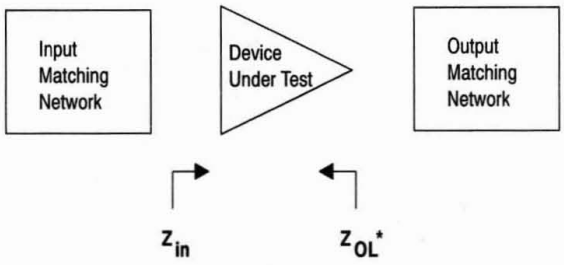


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

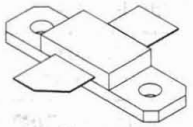
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9045
MRF9045S
MRF9045SR1

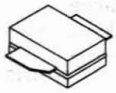
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 28 volt base station equipment.

- Typical Two–Tone Performance at 945 MHz, 28 Volts
  Output Power — 45 Watts PEP
  Power Gain — 18.8 dB
  Efficiency — 42%
  IMD — –32 dBc
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 945 MHz, 45 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- MRF9045S Is Available in Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.

945 MHz, 45 W, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B–05, STYLE 1
(NI–360)
(MRF9045)



CASE 360C–05, STYLE 1
(NI–360S)
(MRF9045S)

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain–Source Voltage		V_{DSS}	65	Vdc
Gate–Source Voltage		V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	MRF9045	P_D	125 0.71	Watts W/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	MRF9045S	P_D	175 1	Watts W/°C
Storage Temperature Range		T_{stg}	–65 to +200	°C
Operating Junction Temperature		T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case	MRF9045 MRF9045S	$R_{\theta JC}$	1.4 1.0	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

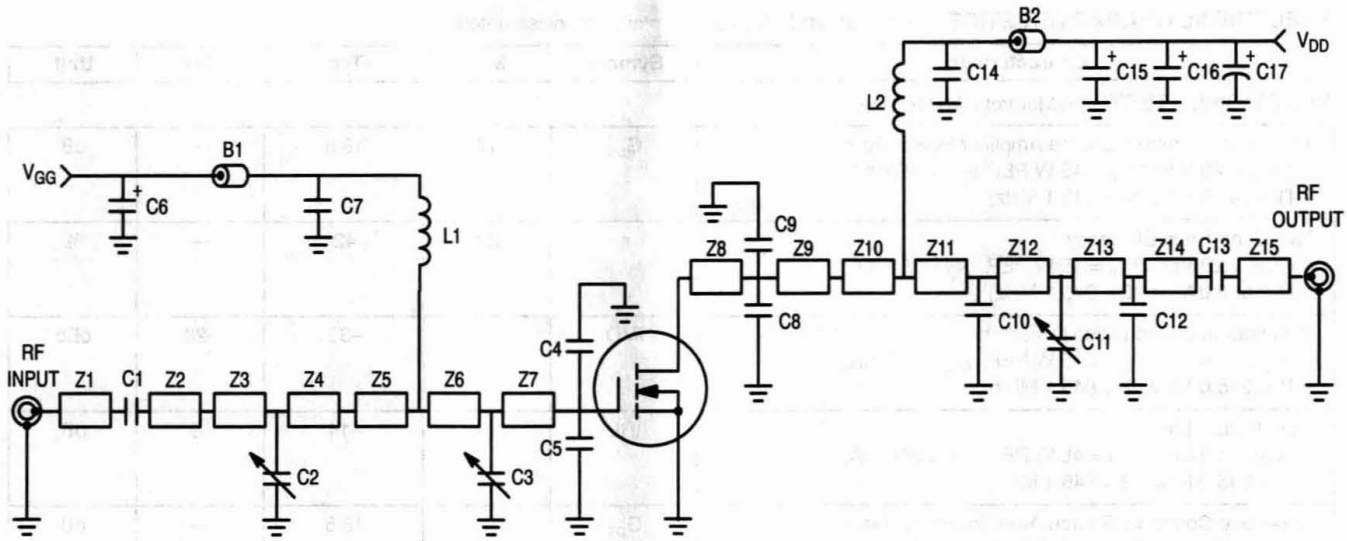
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 350 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	4	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	69	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.5	—	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G_{ps}	17	18.8	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	38	42	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	–32	–28	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	—	–14	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	G_{ps}	—	18.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	η	—	41	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	—	–33	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	—	13	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 28 Vdc, P_{out} = 45 W CW, I_{DQ} = 350 mA, f1 = 945.0 MHz)	P_{1dB}	—	55	—	W
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W CW, I_{DQ} = 350 mA, f1 = 945.0 MHz)	G_{ps}	—	18	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W CW, I_{DQ} = 350 mA, f1 = 945.0 MHz)	η	—	60	—	%
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 45 W CW, I_{DQ} = 350 mA, f = 945.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			



B1	Short Ferrite Bead Surface Mount	Z4	0.360″ x 0.320″ Microstrip
B2	Long Ferrite Bead Surface Mount	Z5	0.240″ x 0.320″ x 0.620″, Taper
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	Z6	0.140″ x 0.620″ Microstrip
C2, C3, C11	0.8–8.0 pF Gigatrim Variable Trim Capacitors	Z7	0.510″ x 0.620″ Microstrip
C4, C5, C8, C9	10 pF Chip Capacitors, B Case	Z8	0.330″ x 0.320″ Microstrip
C6, C15, C16	10 μF, 35 V Tantalum Surface Mount Chip Capacitors	Z9	0.140″ x 0.320″ Microstrip
C10	2.2 pF Chip Capacitor, B Case	Z10	0.070″ x 0.080″ Microstrip
C12	0.7 pF Chip Capacitor, B Case – MRF9045S	Z11	0.240″ x 0.080″ Microstrip
	1.3 pF Chip Capacitor, B Case – MRF9045	Z12	0.140″ x 0.080″ Microstrip
C17	220 μF, 50 V Electrolytic Capacitor	Z13	0.930″ x 0.080″ Microstrip
L1, L2	12.5 nH Surface Mount Inductors, Coilcraft	Z14	0.180″ x 0.080″ Microstrip
Z1	0.260″ x 0.080″ Microstrip	Z15	0.350″ x 0.080″ Microstrip
Z2	0.610″ x 0.120″ Microstrip	Printed Circuit Board	0.03″ Glass Teflon®, ε_r = 2.55 ARLON GX–0300–55–22
Z3	0.260″ x 0.320″ Microstrip		

Figure 1. 930 – 960 MHz Broadband Test Circuit Schematic

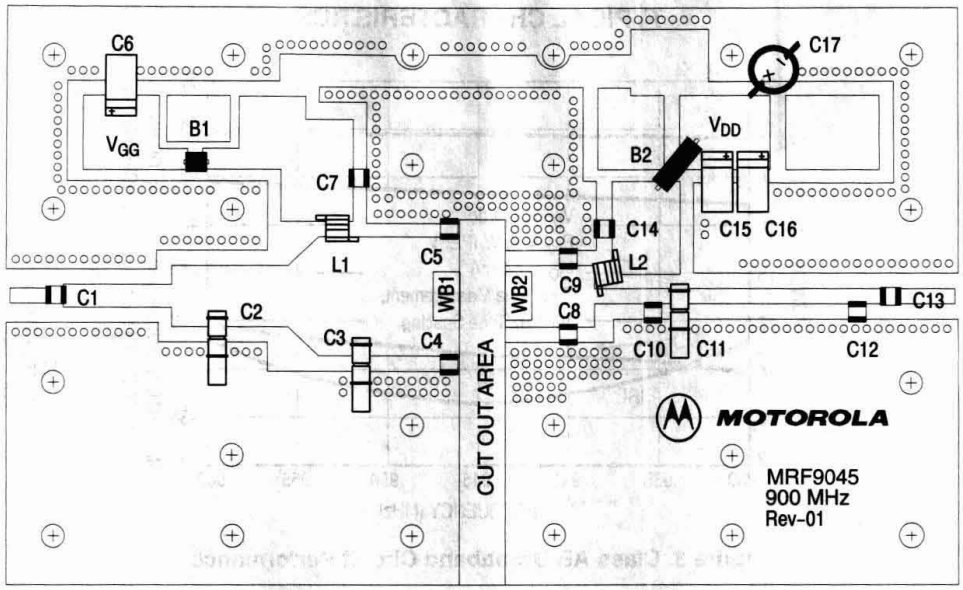


Figure 2. 930 – 960 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

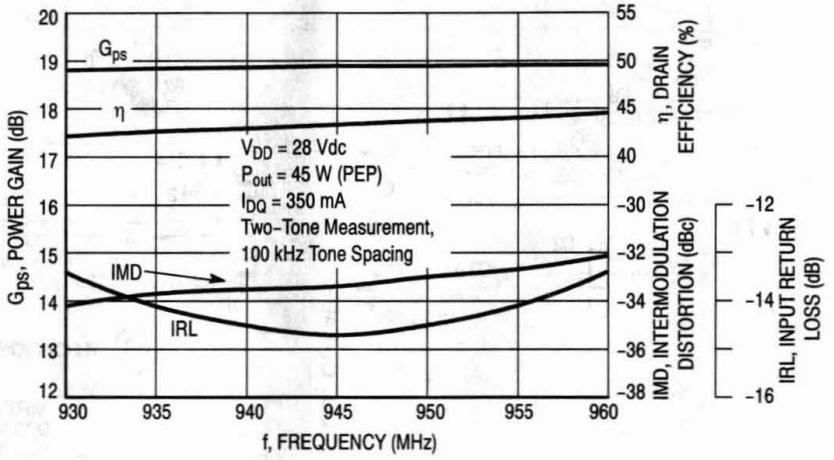


Figure 3. Class AB Broadband Circuit Performance

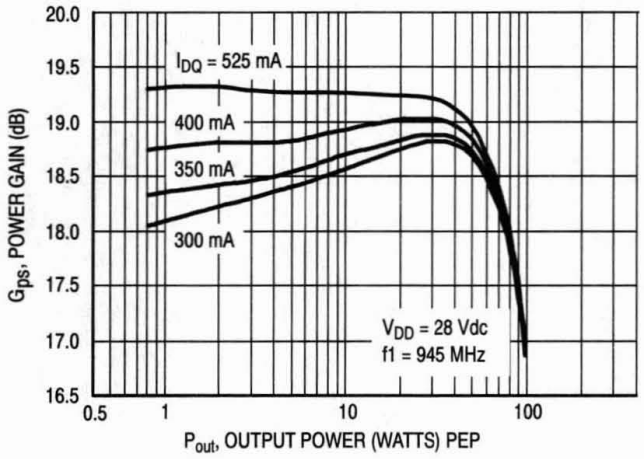


Figure 4. Power Gain versus Output Power

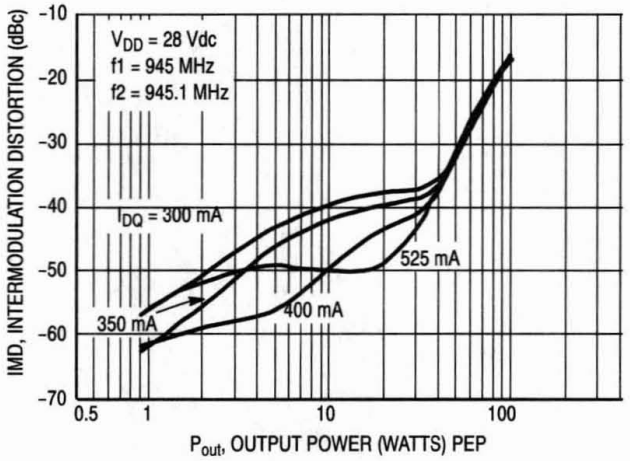


Figure 5. Intermodulation Distortion versus Output Power

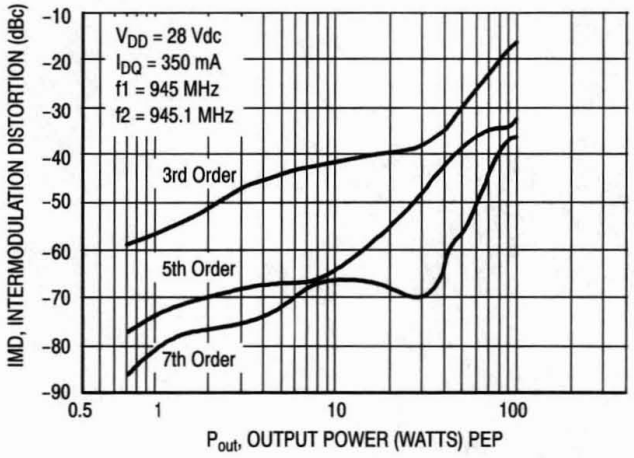


Figure 6. Intermodulation Distortion Products versus Output Power

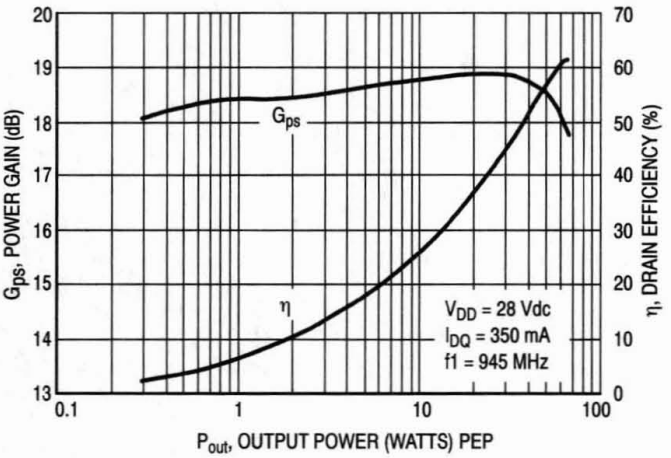
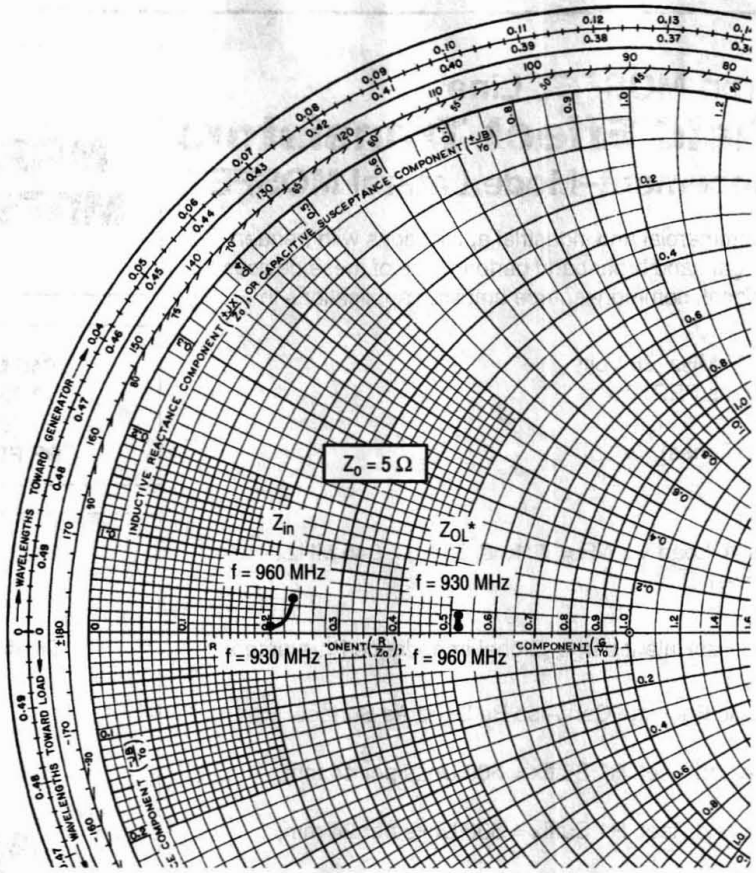


Figure 7. Power Gain, Efficiency versus Output Power



V_{DD} = 28 V, I_{DQ} = 350 mA, P_{out} = 45 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	1.02 + j0.06	2.6 + j0.20
945	1.10 + j0.11	2.6 + j0.16
960	1.15 + j0.25	2.6 + j0.10

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

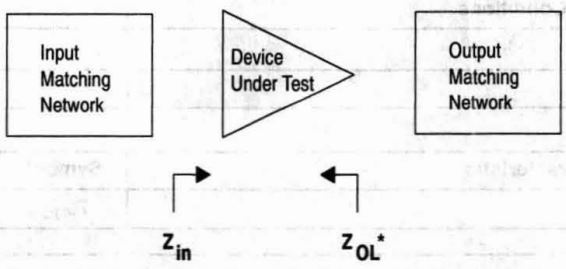


Figure 8. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

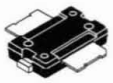
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9045MR1
MRF9045MBR1

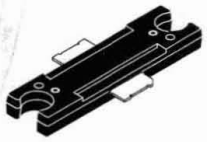
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 28 volt base station equipment.

- Typical Performance at 945 MHz, 28 Volts
  Output Power — 45 Watts PEP
  Power Gain — 19 dB
  Efficiency — 41% (Two Tones)
  IMD — –31 dBc
- Integrated ESD Protection
- Guaranteed Ruggedness @ Load VSWR = 5:1, @ 28 Vdc, 945 MHz, 45 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Moisture Sensitivity Level 3
- Dual–Lead Boltdown Plastic Package Can Also Be Used As Surface Mount.
- TO–272 Available in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.
- TO–270 Available in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

945 MHz, 45 W, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 1265–07, STYLE 1
(TO–270)
PLASTIC
(MRF9045MR1)



CASE 1337–01, STYLE 1
(TO–272 DUAL LEAD)
PLASTIC
(MRF9045MBR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	177 1.18	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	175	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

THERMAL CHARACTERISTICS

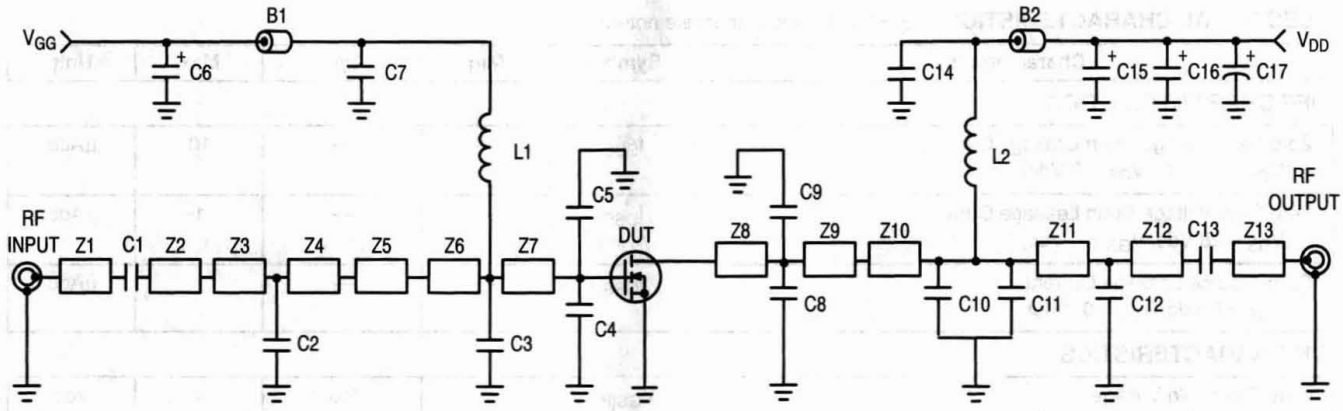
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.85	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	2	2.8	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 350 mAdc)	$V_{GS(Q)}$	3	3.7	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.22	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	4	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	70	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	38	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G_{ps}	17	19	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	38	41	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	—	–14	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	G_{ps}	—	19	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	η	—	41	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 350 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	—	–13	—	dB



B1, B2	Short Ferrite Beads, Surface Mount	Z3	0.14″ x 0.32″ Microstrip
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	Z4	0.47″ x 0.32″ Microstrip
C2, C8	2.7 pF Chip Capacitors, B Case	Z5	0.16″ x 0.32″ x 0.62″ Taper
C3	3.9 pF Chip Capacitor, B Case	Z6	0.18″ x 0.62″ Microstrip
C4, C5, C8, C9	10 pF Chip Capacitors, B Case	Z7	0.56″ x 0.62″ Microstrip
C6, C15, C16	10 μF, 35 V Tantalum Surface Mount Capacitors	Z8	0.33″ x 0.32″ Microstrip
C10	2.2 pF Chip Capacitor, B Case	Z9	0.14″ x 0.32″ Microstrip
C11	4.7 pF Chip Capacitor, B Case	Z10	0.36″ x 0.08″ Microstrip
C12	1.2 pF Chip Capacitor, B Case	Z11	1.01″ x 0.08″ Microstrip
C17	220 μF, 50 V Electrolytic Capacitor	Z12	0.15″ x 0.08″ Microstrip
L1, L2	12.5 nH Inductors	Z13	0.29″ x 0.08″ Microstrip
Z1	0.20″ x 0.08″ Microstrip		
Z2	0.57″ x 0.12″ Microstrip		

Figure 1. MRF9045MR1 930–960 MHz Broadband Test Circuit Schematic

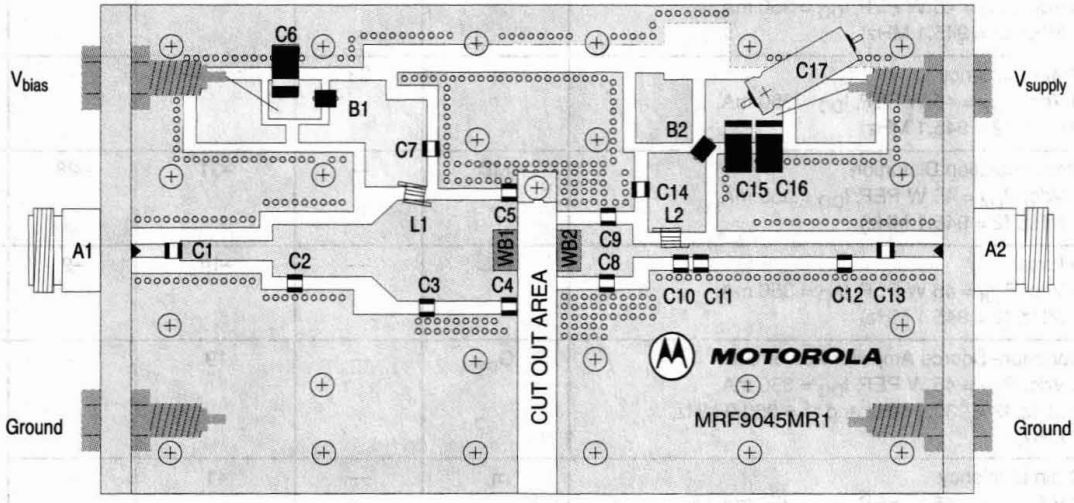
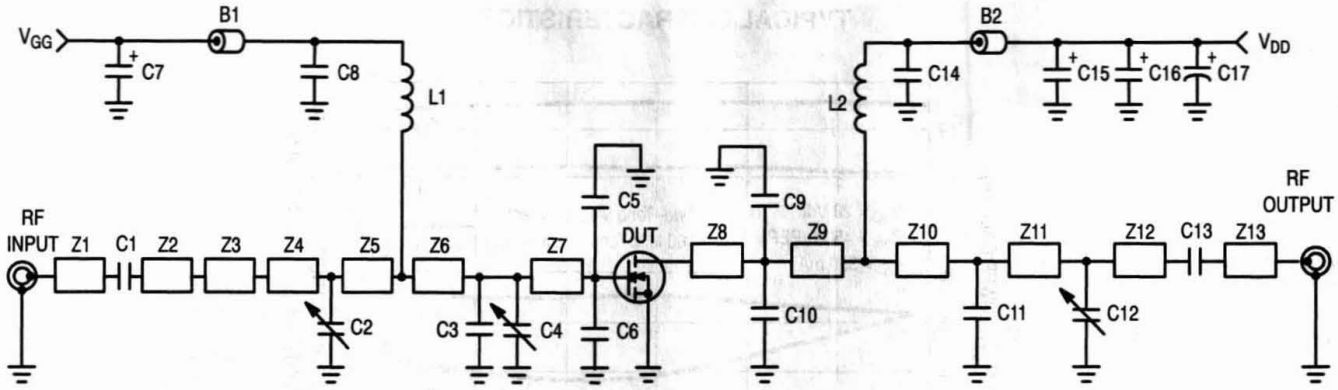


Figure 2. MRF9045MR1 930–960 MHz Broadband Test Circuit Component Layout



B1	Short Ferrite Bead	Z1	0.260″ x 0.060″ Microstrip
B2	Long Ferrite Bead	Z2	0.240″ x 0.060″ Microstrip
C1, C8, C13, C14	47 pF Chip Capacitors, B Case	Z3	0.500″ x 0.100″ Microstrip
C2	0.4–2.5 pF Variable Capacitor, Johanson Gigatrim	Z4	0.215″ x 0.270″ Microstrip
C3	3.6 pF Chip Capacitor, B Case	Z5	0.315″ x 0.270″ Microstrip
C4	0.8–8.0 pF Variable Capacitor, Johanson Gigatrim	Z6	0.160″ x 0.270″ x 0.520″ Taper
C5, C6, C9, C10	10 pF Chip Capacitors, B Case	Z7	0.285″ x 0.520″ Microstrip
C7, C15, C16	10 μF, 35 V Tantalum Chip Capacitors	Z8	0.140″ x 0.270″ Microstrip
C11	7.5 pF Chip Capacitor, B Case	Z9	0.450″ x 0.270″ Microstrip
C12	0.6–4.5 pF Variable Capacitor, Johanson Gigatrim	Z10	0.250″ x 0.060″ Microstrip
C17	220 μF Electrolytic Chip Capacitor	Z11	0.720″ x 0.060″ Microstrip
L1, L2	12.5 nH Surface Mount Inductors	Z12	0.490″ x 0.060″ Microstrip
WB1, WB2	10 mil Brass Wear Blocks	Z13	0.290″ x 0.060″ Microstrip
		Board	Taconic RF–35–0300, ε_r = 3.5

Figure 3. MRF9045MBR1 930–960 MHz Broadband Test Circuit Schematic

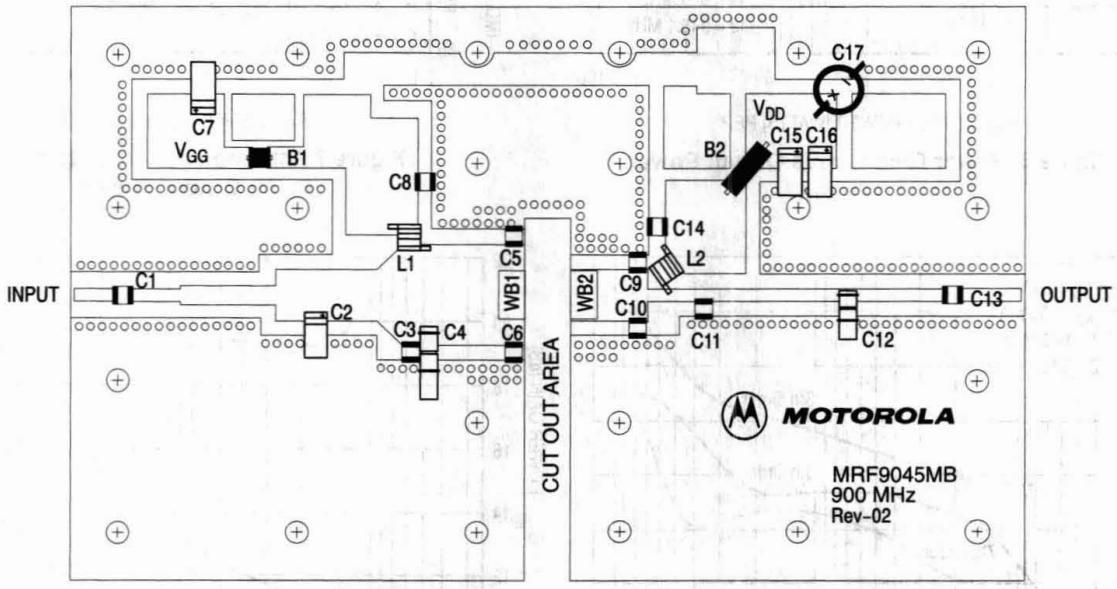


Figure 4. MRF9045MBR1 930–960 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

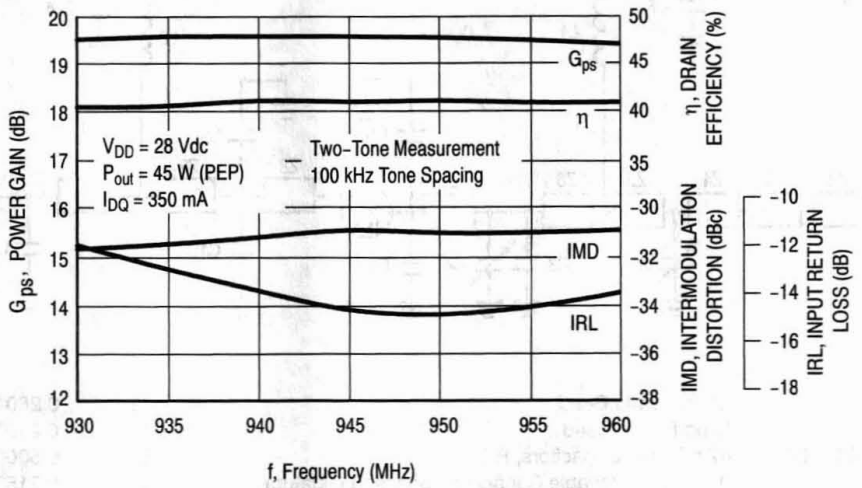


Figure 5. Class AB Broadband Circuit Performance

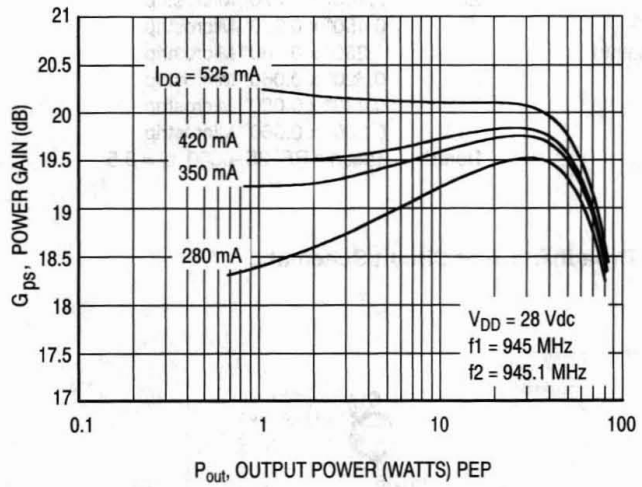


Figure 6. Power Gain versus Output Power

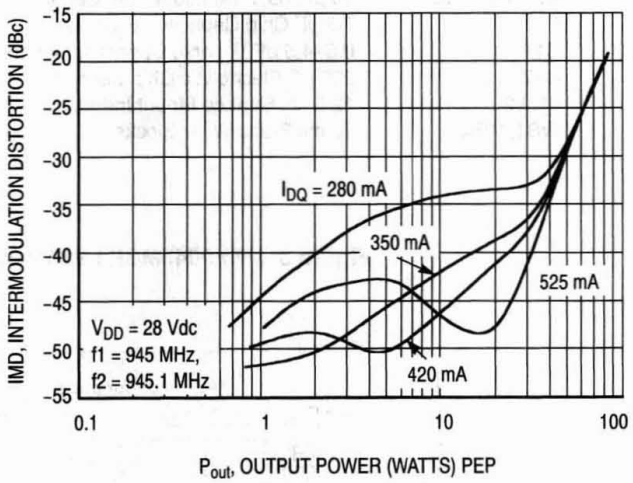


Figure 7. Intermodulation Distortion versus Output Power

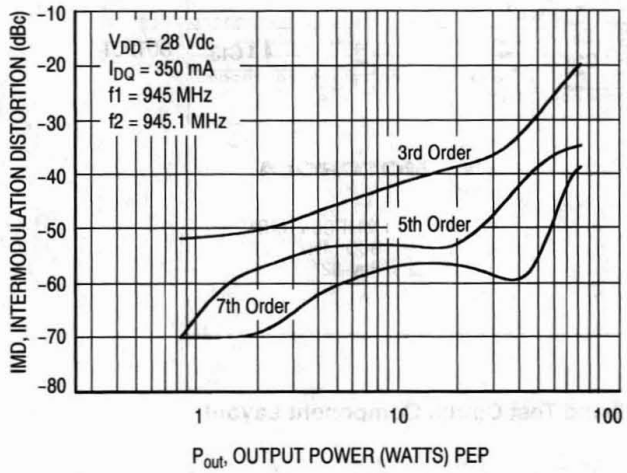


Figure 8. Intermodulation Distortion Products versus Output Power

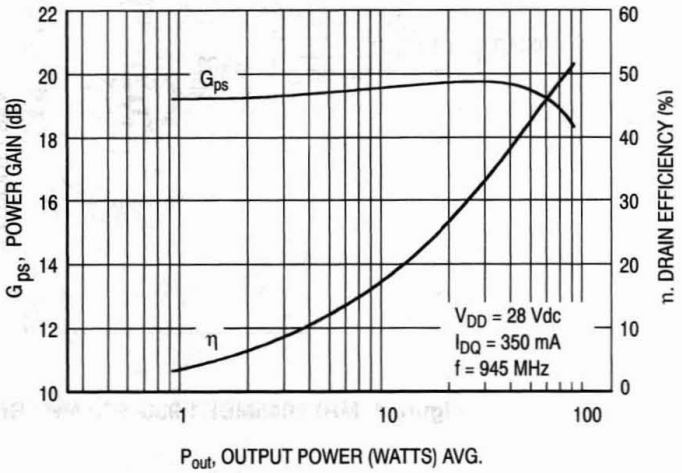


Figure 9. Power Gain and Efficiency versus Output Power

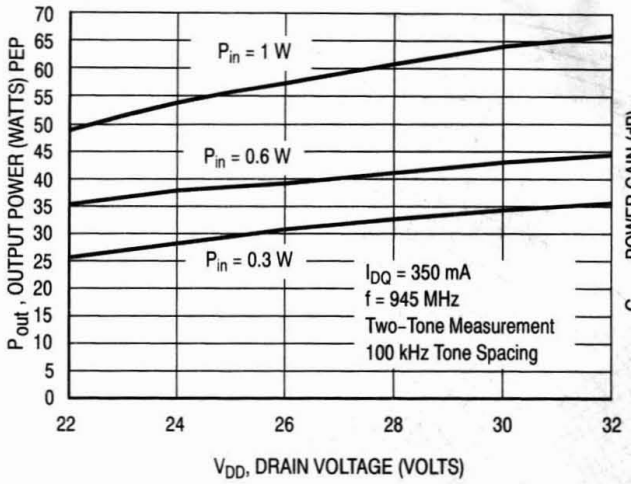


Figure 10. Output Voltage versus Supply Voltage (MRF9045MR1)

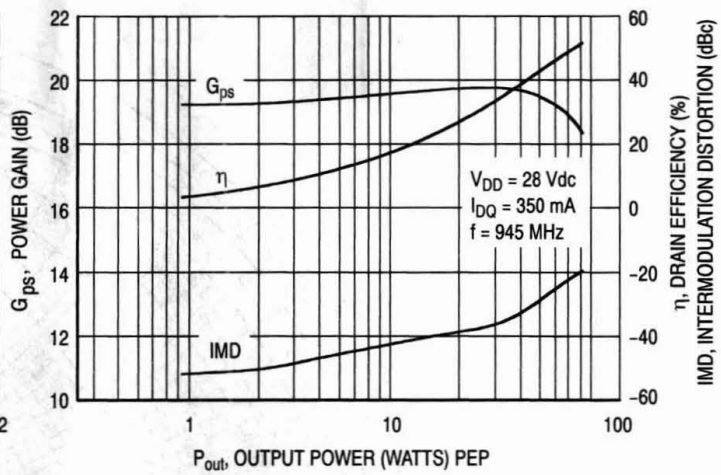
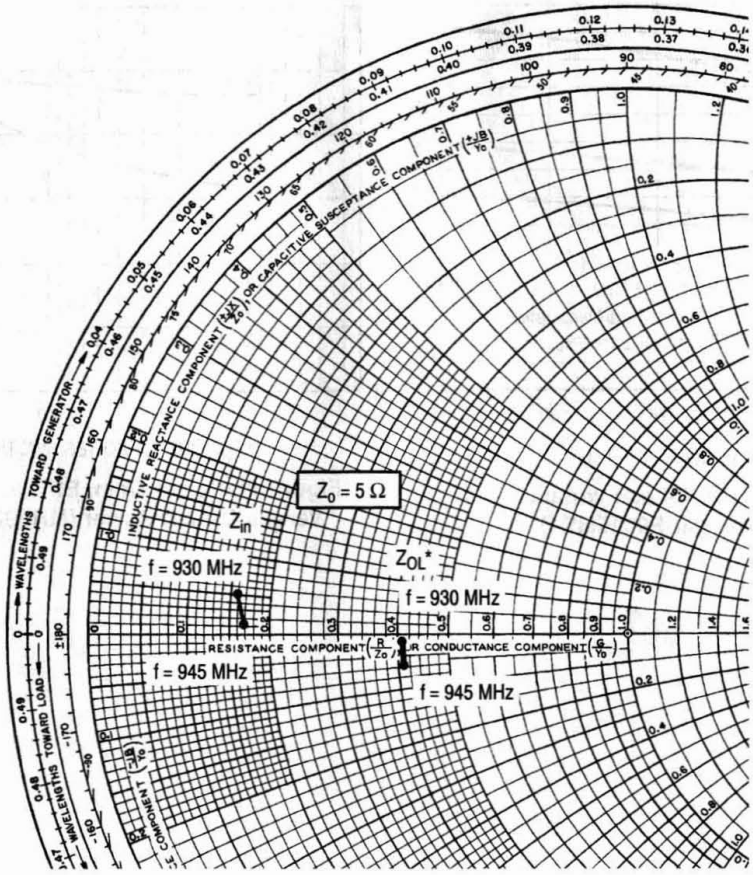


Figure 11. Power Gain, Efficiency and IMD versus Output Power (MRF9045MBR1)



V_{DD} = 28 V, I_{DQ} = 350 mA, P_{out} = 45 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	0.81 + j0.25	2.03 – j0.09
945	0.85 + j0.05	2.03 – j0.28

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

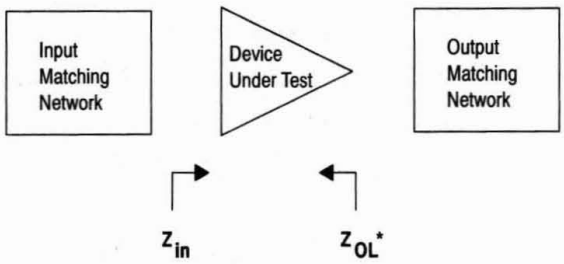
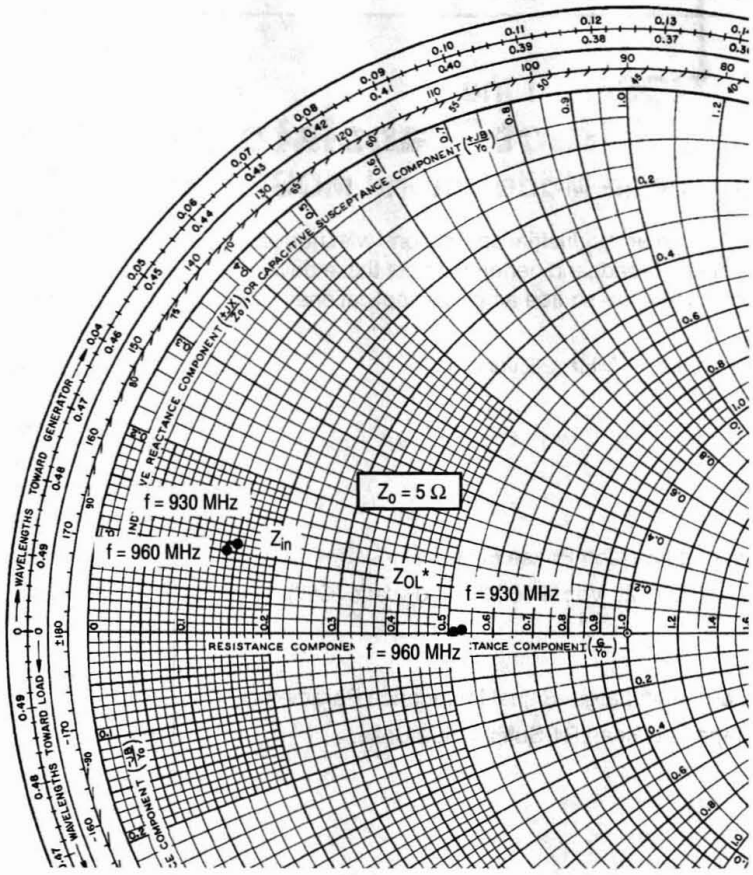


Figure 12. Series Equivalent Input and Output Impedance (MRF9045MR1)



V_{DD} = 28 V, I_{DQ} = 350 mA, P_{out} = 45 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	0.75 + j0.6	2.65 + j0.05
945	0.72 + j0.6	2.60 + j0.05
960	0.70 + j0.5	2.55 + j0.02

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

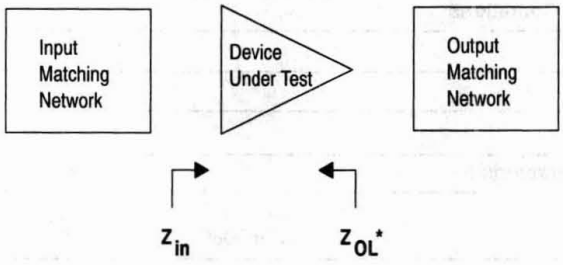


Figure 13. Series Equivalent Input and Output Impedance (MRF9045MBR1)

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

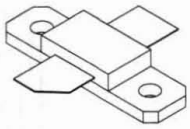
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9060
MRF9060S
MRF9060SR1

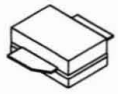
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical Two–Tone Performance at 945 MHz, 26 Volts
  Output Power — 60 Watts PEP
  Power Gain — 17 dB
  Efficiency — 40%
  IMD — –31 dBc
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 945 MHz, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- MRF9060S Is Available in Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.

945 MHz, 60 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B–05, STYLE 1
(NI–360)
(MRF9060)



CASE 360C–05, STYLE 1
(NI–360S)
(MRF9060S)

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain–Source Voltage		V_{DSS}	65	Vdc
Gate–Source Voltage		V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	MRF9060 MRF9060S	P_D	159 0.91 219 1.25	Watts W/°C Watts W/°C
Storage Temperature Range		T_{stg}	–65 to +200	°C
Operating Junction Temperature		T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case	MRF9060 MRF9060S	$R_{\theta JC}$	1.1 0.8	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

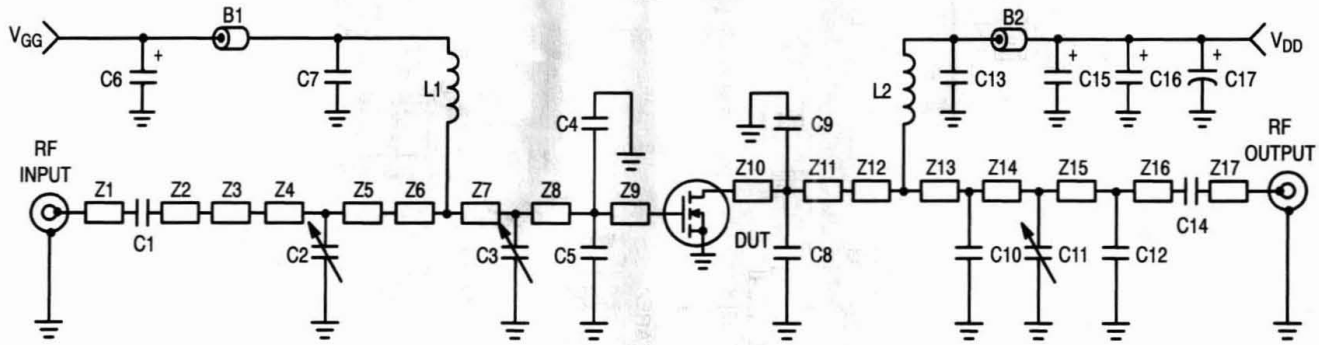
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 450 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.3 Adc)	$V_{DS(on)}$	—	0.17	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	g_{fs}	—	5.3	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	98	—	pF
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	50	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2	—	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G_{ps}	16	17	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	36	40	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	—	–16	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	G_{ps}	—	17	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	η	—	39	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	—	–16	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 450 mA, f1 = 945.0 MHz)	P_{1dB}	—	70	—	W
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 450 mA, f1 = 945.0 MHz)	G_{ps}	—	17	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 450 mA, f1 = 945.0 MHz)	η	—	51	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 450 mA, f = 945.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			



Z1	0.240″ x 0.060″ Microstrip	Z10	0.360″ x 0.270″ Microstrip
Z2	0.240″ x 0.060″ Microstrip	Z11	0.060″ x 0.270″ Microstrip
Z3	0.500″ x 0.100″ Microstrip	Z12	0.110″ x 0.060″ Microstrip
Z4	0.180″ x 0.270″ Microstrip	Z13	0.330″ x 0.060″ Microstrip
Z5	0.350″ x 0.270″ Microstrip	Z14	0.230″ x 0.060″ Microstrip
Z6	0.270″ x 0.520 x 0.140″ Taper	Z15	0.740″ x 0.060″ Microstrip
Z7	0.170″ x 0.520″ Microstrip	Z16	0.130″ x 0.060″ Microstrip
Z8	0.410″ x 0.520″ Microstrip	Z17	0.340″ x 0.060″ Microstrip
Z9	0.060″ x 0.520″ Microstrip		

Figure 1. 945 MHz Broadband Test Circuit Schematic

Table 1. 945 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1	Short Ferrite Bead	95F786	Newark
B2	Long Ferrite Bead	95F787	Newark
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	100B470JP 500X	ATC
C2, C3, C11	0.8–8.0 Gigatrim Variable Capacitors	44F3360	Newark
C4, C5, C8, C9	10 pF Chip Capacitors, B Case	100B100JP 500X	ATC
C6, C15, C16	10 μF, 35 V Tantalum Chip Capacitor	93F2975	Newark
C10	3.0 pF Chip Capacitor, B Case	100B3R0JP 500X	ATC
C12	0.5 pF Chip Capacitor, B Case (MRF9060) 0.7 pF Chip Capacitor, B Case (MRF9060S)	100B0R5BP 500X 100B0R7BP 500X	ATC ATC
C17	220 μF Electrolytic Chip Capacitor	14F185	Newark
L1, L2	12.5 nH Inductors	A04T–5	Coilcraft
N1, N2	N–Type Panel Mount, Stripline	3052–1648–10	Avnet
WB1, WB2	10 mil Brass Wear Blocks		
Board Material	30 mil Glass Teflon®, ε_r = 3.55 Copper Clad, 1 oz Cu	RF–35–0300	Taconic
PCB	Etched Circuit Board	MRF9060 900 MHz, Rev. 2	

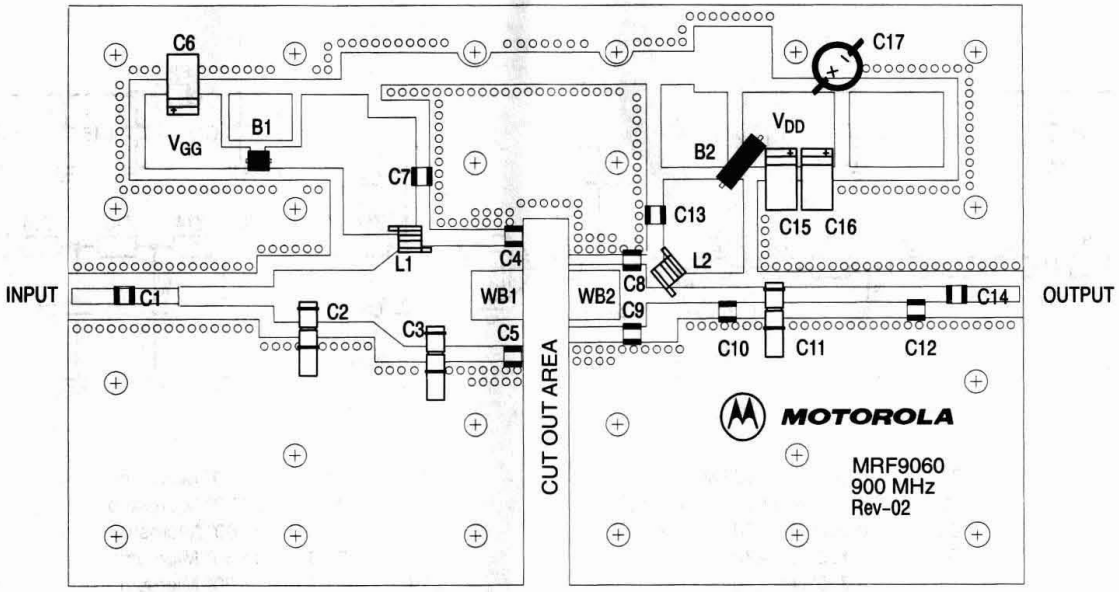


Figure 2. 930 – 960 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

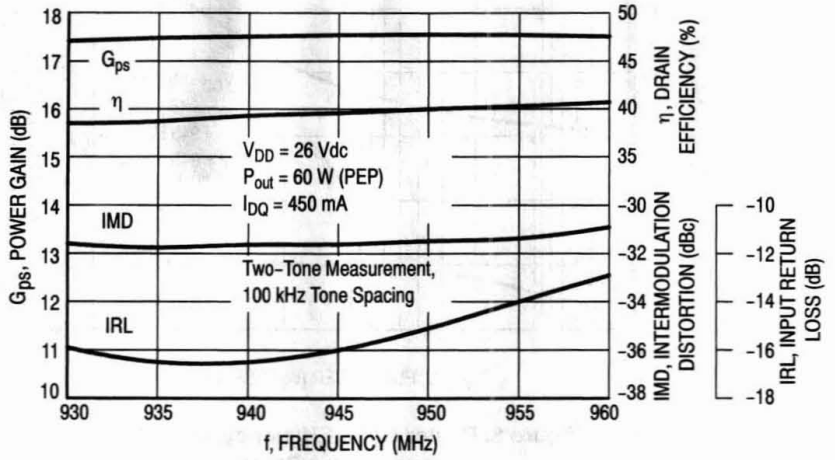


Figure 3. Class AB Broadband Circuit Performance

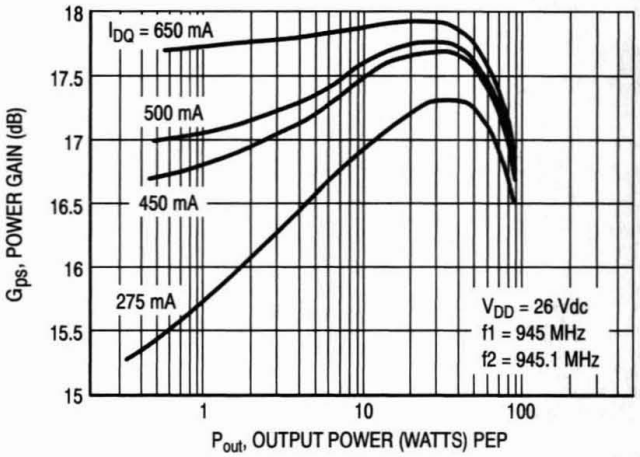


Figure 4. Power Gain versus Output Power

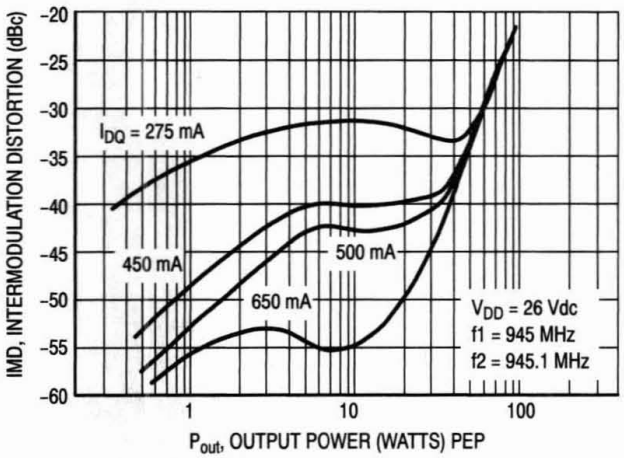


Figure 5. Intermodulation Distortion versus Output Power

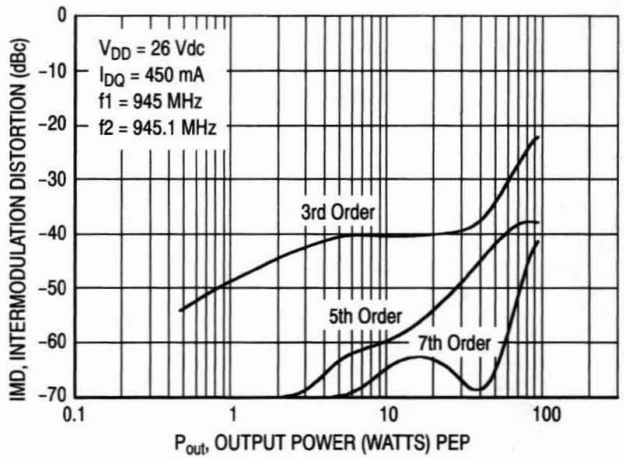


Figure 6. Intermodulation Distortion Products versus Output Power

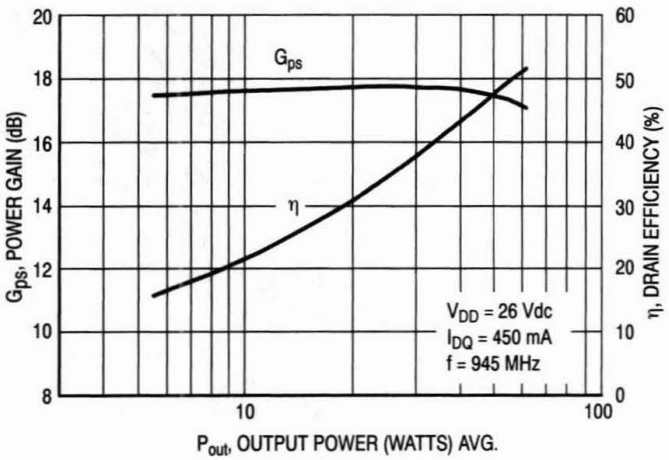


Figure 7. Power Gain and Efficiency versus Output Power

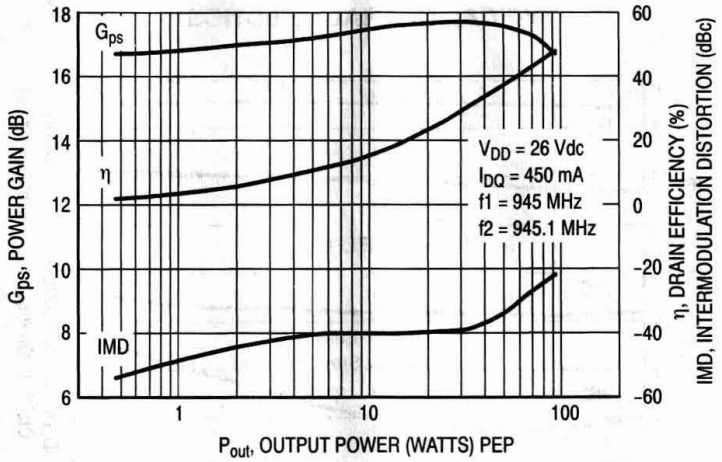
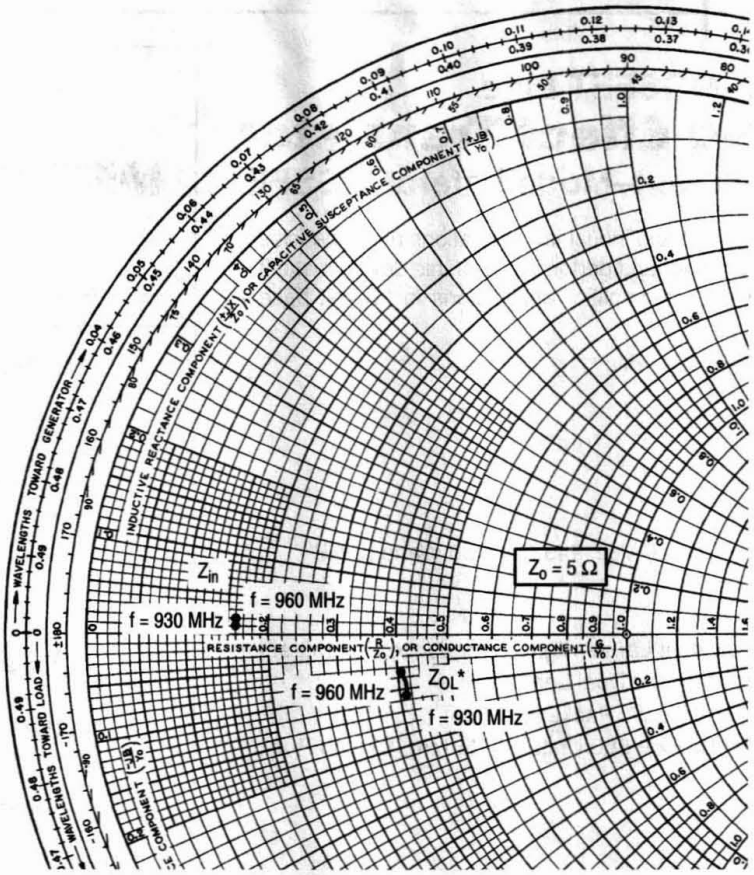


Figure 8. Power Gain, Efficiency, and IMD versus Output Power



V_{DD} = 26 V, I_{DQ} = 450 mA, P_{out} = 60 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	0.80 + j0.10	2.08 – j0.65
945	0.80 + j0.05	2.07 – j0.38
960	0.81 + j0.10	2.04 – j0.37

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

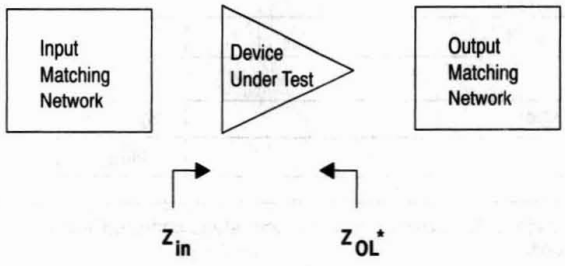


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistor

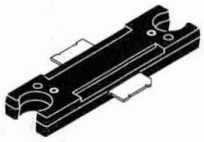
N–Channel Enhancement–Mode Lateral MOSFET

MRF9060MBR1

Designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz. The high gain and broadband performance of this device make it ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical Performance at 945 MHz, 26 Volts
  Output Power – 60 Watts PEP
  Power Gain – 18.0 dB
  Efficiency – 40% (Two Tones)
  IMD – –31.5 dBc
- Integrated ESD Protection
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 945 MHz, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Moisture Sensitivity Level 3 for TO–272 Dual Lead
- TO–272 Dual Lead Is a Boltdown Plastic Package.
- Available in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

945 MHz, 60 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET



CASE 1337–01, STYLE 1
(TO–272 DUAL LEAD)
PLASTIC
(MRF9060MBR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	223 1.79	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

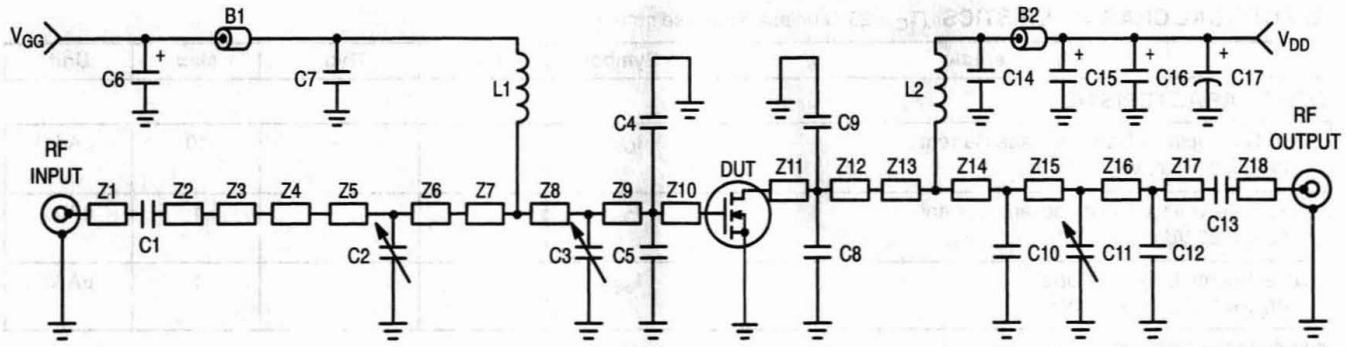
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.56	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	2.8	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 450 mAdc)	$V_{GS(Q)}$	3	3.7	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.3 Adc)	$V_{DS(on)}$	—	0.21	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	g_{fs}	—	5.3	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	101	—	pF
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	53	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.5	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G_{ps}	17	18	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	37	40	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	–31.5	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	–9	–14.5	—	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHZ)	G_{ps}	—	18	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHZ)	η	—	40	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHZ)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 450 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHZ)	IRL	—	–12.5	—	dB



Z1	0.240″ x 0.060″ Microstrip	Z10	0.060″ x 0.520″ Microstrip
Z2	0.240″ x 0.060″ Microstrip	Z11	0.360″ x 0.270″ Microstrip
Z3	0.500″ x 0.100″ Microstrip	Z12	0.060″ x 0.270″ Microstrip
Z4	0.100″ x 0.270″ x 0.080″, Taper	Z13	0.130″ x 0.060″ Microstrip
Z5	0.330″ x 0.270″ Microstrip	Z14	0.300″ x 0.060″ Microstrip
Z6	0.120″ x 0.270″ Microstrip	Z15	0.210″ x 0.060″ Microstrip
Z7	0.270″ x 0.520″ x 0.140″, Taper	Z16	0.600″ x 0.060″ Microstrip
Z8	0.240″ x 0.520″ Microstrip	Z17	0.290″ x 0.060″ Microstrip
Z9	0.340″ x 0.520″ Microstrip	Z18	0.340″ x 0.060″ Microstrip

Figure 1. 930–960 MHz Broadband Test Circuit Schematic

Table 1. 930–960 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1	Short Ferrite Bead	95F786	Newark
B2	Long Ferrite Bead	95F787	Newark
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	100B470JP 500X	ATC
C2, C3, C11	0.8–8.0 Gigatrim Variable Capacitors	44F3360	Newark
C4, C5	11 pF Chip Capacitors, B Case (MRF9060MR1) 10 pF Chip Capacitors, B Case (MRF9060MBR1)	100B110JP 500X 100B100JP 500X	ATC
C6, C15, C16	10 μF, 35 V Tantalum Chip Capacitors	93F2975	Newark
C8, C9	10 pF Chip Capacitors, B Case	100B100JP 500X	Newark
C10	3.9 pF Chip Capacitor, B Case	100B3R9CP 500X	ATC
C12	1.7 pF Chip Capacitor, B Case	100B1R7BP 500X	ATC
C17	220 μF Electrolytic Chip Capacitor	14F185	Newark
L1, L2	12.5 nH Inductors	A04T–5	Coilcraft
N1, N2	N–Type Panel Mount, Stripline	3052–1648–10	Avnet
WB1, WB2	15 mil Brass Wear Blocks		
Board Material	30 mil Glass Teflon®, ε_r = 2.55 Copper Clad, 2 oz Cu	RF–35–0300	Taconic
PCB	Etched Circuit Board	TO–270/TO–272 Surface/Bolt	DSelectronics

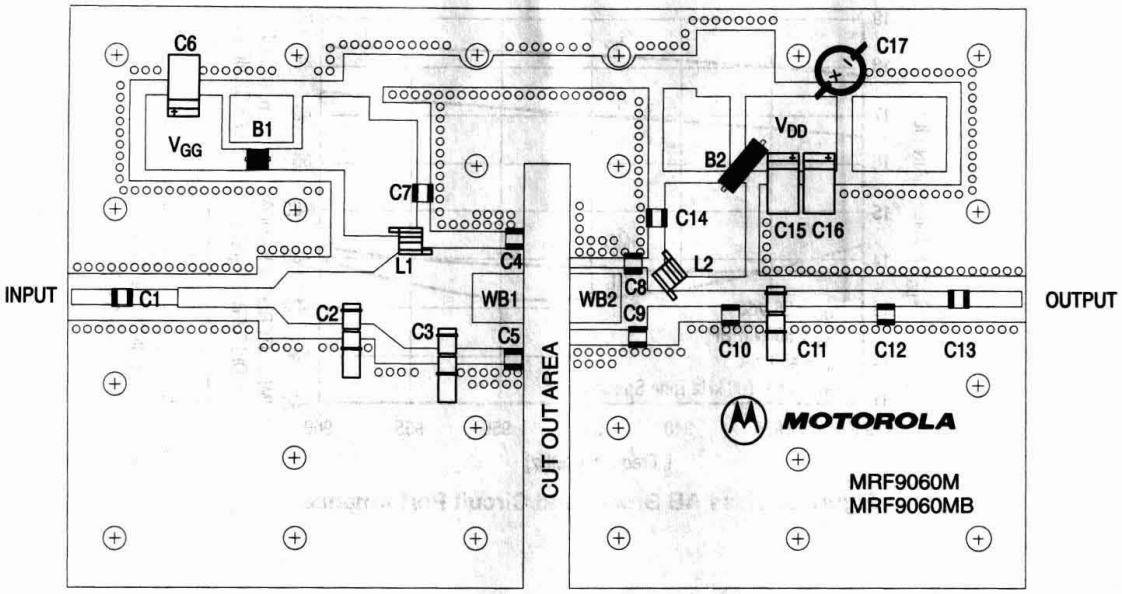


Figure 2. 930–960 MHz Broadband Test Circuit Component Layout

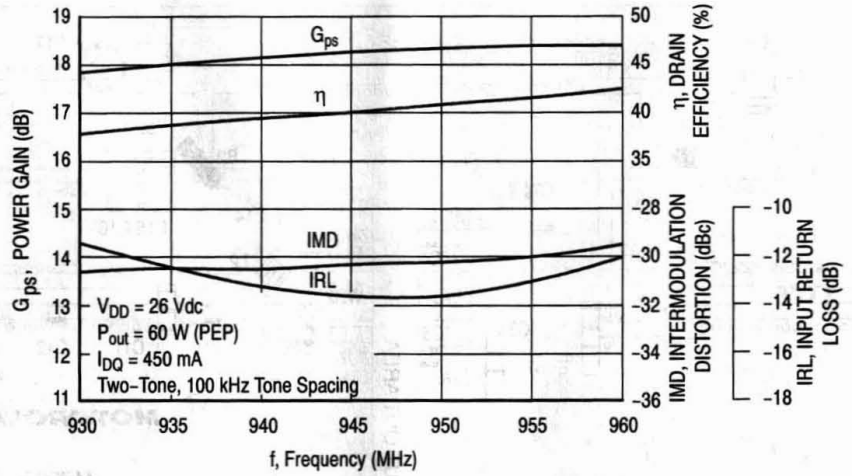


Figure 3. Class AB Broadband Circuit Performance

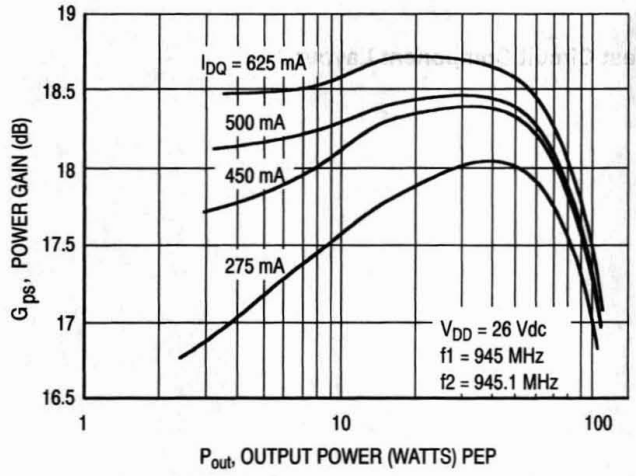


Figure 4. Power Gain versus Output Power

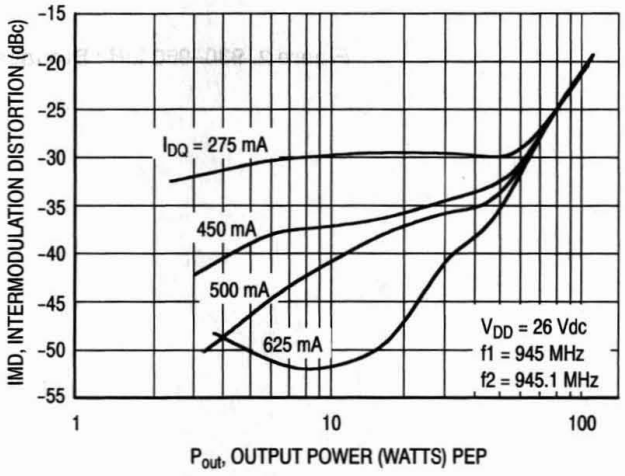


Figure 5. Intermodulation Distortion versus Output Power

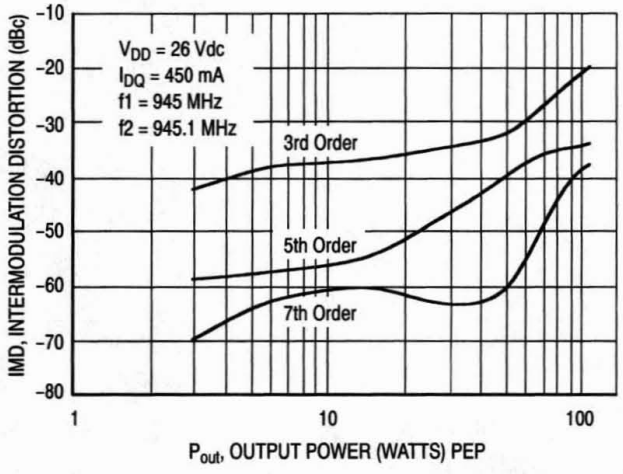


Figure 6. Intermodulation Distortion Products versus Output Power

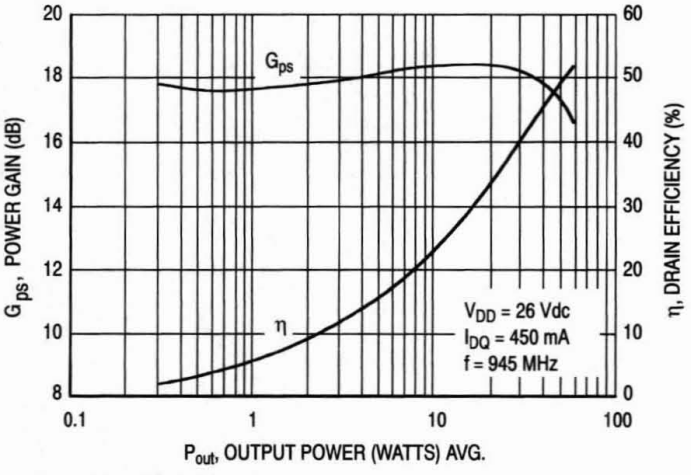


Figure 7. Power Gain and Efficiency versus Output Power

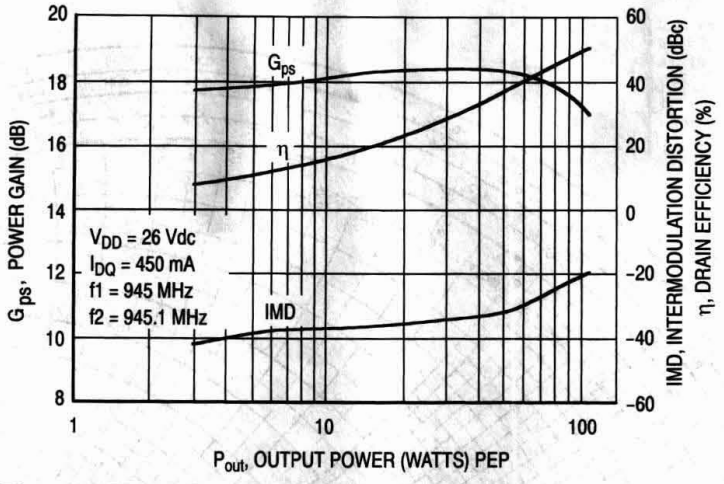
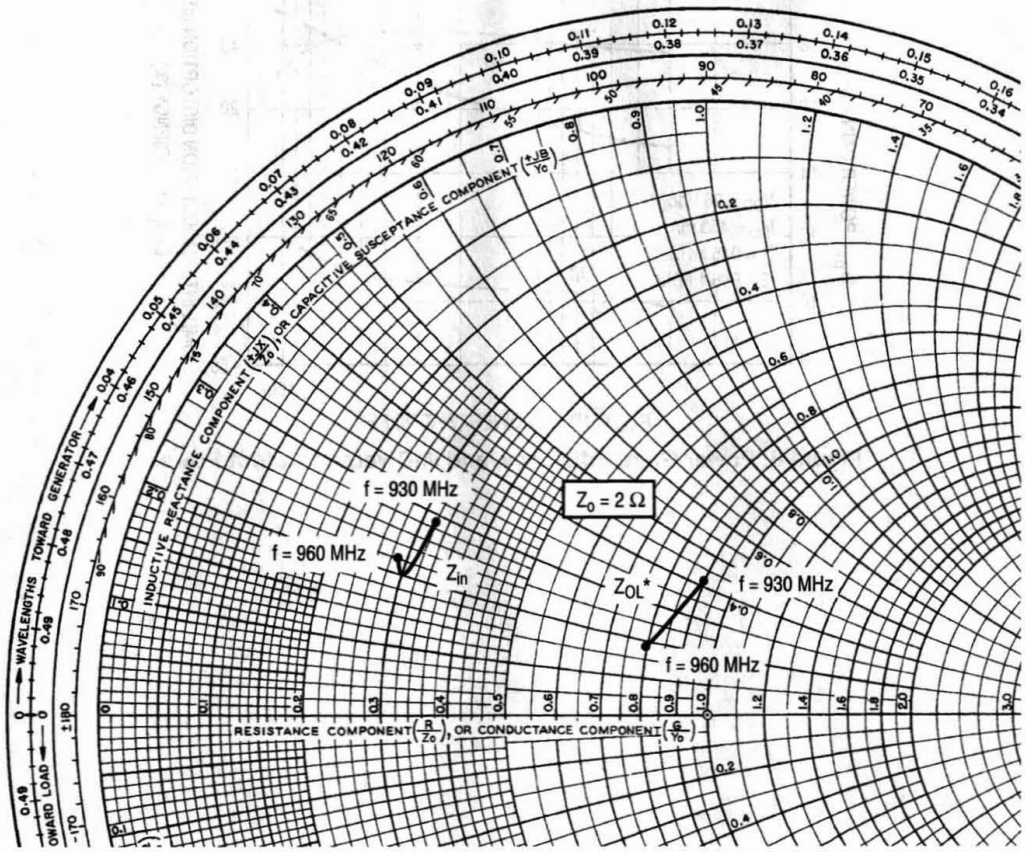


Figure 8. Power Gain, Efficiency, and IMD versus Output Power



V_{DD} = 26 V, I_{DQ} = 450 mA, P_{out} = 60 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	0.63 + j0.57	1.8 + j0.84
945	0.60 + j0.41	1.7 + j0.55
960	0.57 + j0.45	1.6 + j0.36

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

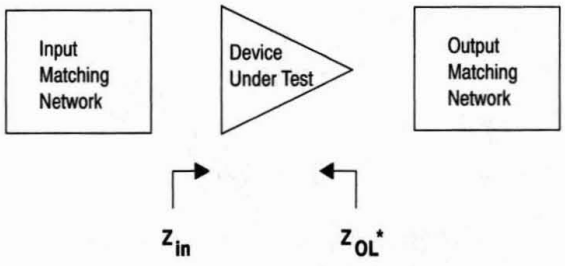


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

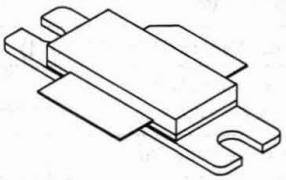
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9080
MRF9080R3
MRF9080S
MRF9080SR3
MRF9080LSR3

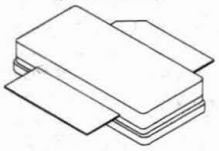
GSM 900 MHz FREQUENCY BAND, 75 W, 26 V LATERAL N–CHANNEL BROADBAND RF POWER MOSFETs

Designed for GSM 900 MHz frequency band, the high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical Performance for GSM Frequencies, 921 to 960 MHz, 26 Volts
  Output Power @ P1db: 75 Watts
  Power Gain @ P1db: 18.5 dB
  Efficiency @ P1db: 55%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 921 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ″ Nominal.



CASE 465–06, STYLE 1
(NI–780)
(MRF9080)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF9080S, MRF9080LSR3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vds, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 700 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6 Adc)	g_{fs}	—	8.0	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	73	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.9	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)					
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 921 and 960 MHz)	P_{1dB}	68	75	—	W
Common–Source Amplifier Power Gain @ 70 W (Min) (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 921 and 960 MHz)	G_{ps}	17	18.5	20	dB
Drain Efficiency @ P_{out} = 70 W (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 921 and 960 MHz)	η1	47	52	—	%
Drain Efficiency @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 600 mA, f = 921 and 960 MHz)	η2	—	55	—	%
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 70 W, I_{DQ} = 600 mA, f = 921 and 960 MHz)	IRL	9.5	12.5	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 600 mA, f = 921 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally input matched.
(2) To meet application requirements, Motorola test fixtures are designed to cover full GSM 900 band ensuring batch to batch consistency

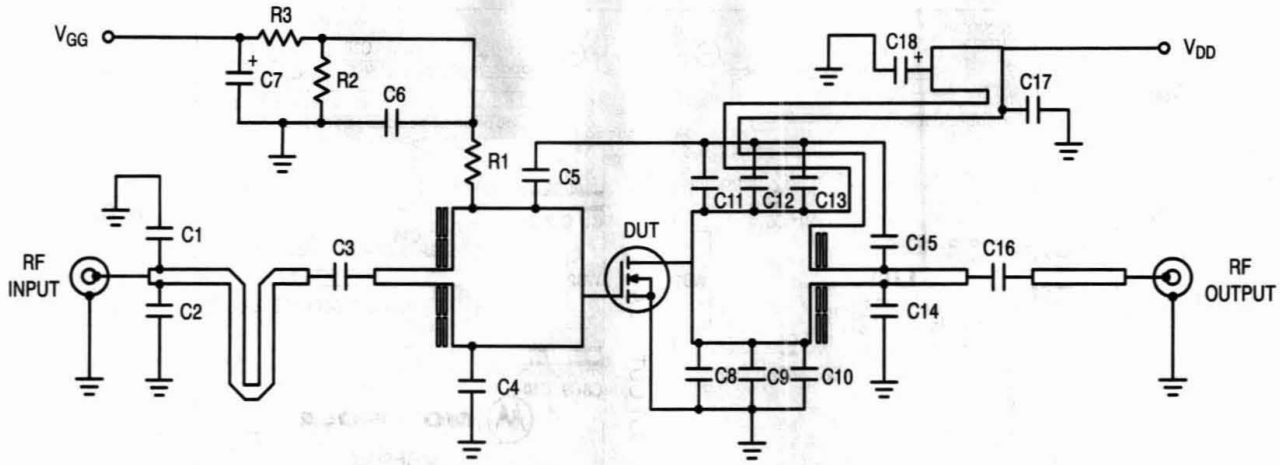


Figure 1. Broadband GSM 900 Test Circuit Schematic

Table 1. Broadband GSM 900 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	4.7 pF Chip Capacitor, B Case	100B4R7BW	ATC
C2	2.7 pF Chip Capacitor, B Case	100B2R7BW	ATC
C3	1.5 pF Chip Capacitor, B Case	100B1R5BW	ATC
C4, C5, C9, C10, C12, C13	5.6 pF Chip Capacitors, B Case	100B5R6CW	ATC
C6, C16, C17	22 pF Chip Capacitors, B Case	100B220GW	ATC
C7, C18	10 μF, 35 V Tantalum Chip Capacitors	293D106X9035D2T	Sprague–Vishay
C8, C11	10 pF Chip Capacitors, B Case	100B100JW	ATC
C14	0.8 pF Chip Capacitor, B Case	100B0R8BW	ATC
C15	8.2 pF Chip Capacitor, B Case	100B8R2GW	ATC
R1, R2, R3	1.0 kΩ, ??? W Chip Resistors (0805)		
WB1, WB2	Beryllium Copper Wear Blocks	0.004″ x 0.210″ x 0.520″	
Raw PCB Material	30 mil Glass Teflon®, ε_r = 2.55	TLX8–0300	Taconic
PCB	Etched Circuit Board	C–GY–00–001–02	Cibel

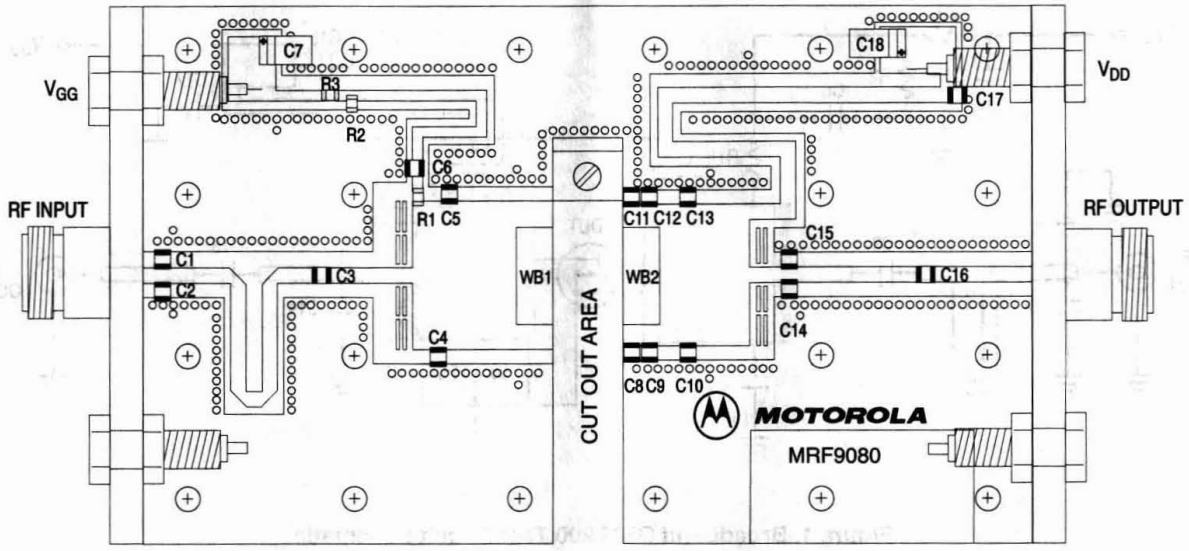


Figure 2. Broadband GSM 900 Test Circuit Component Layout

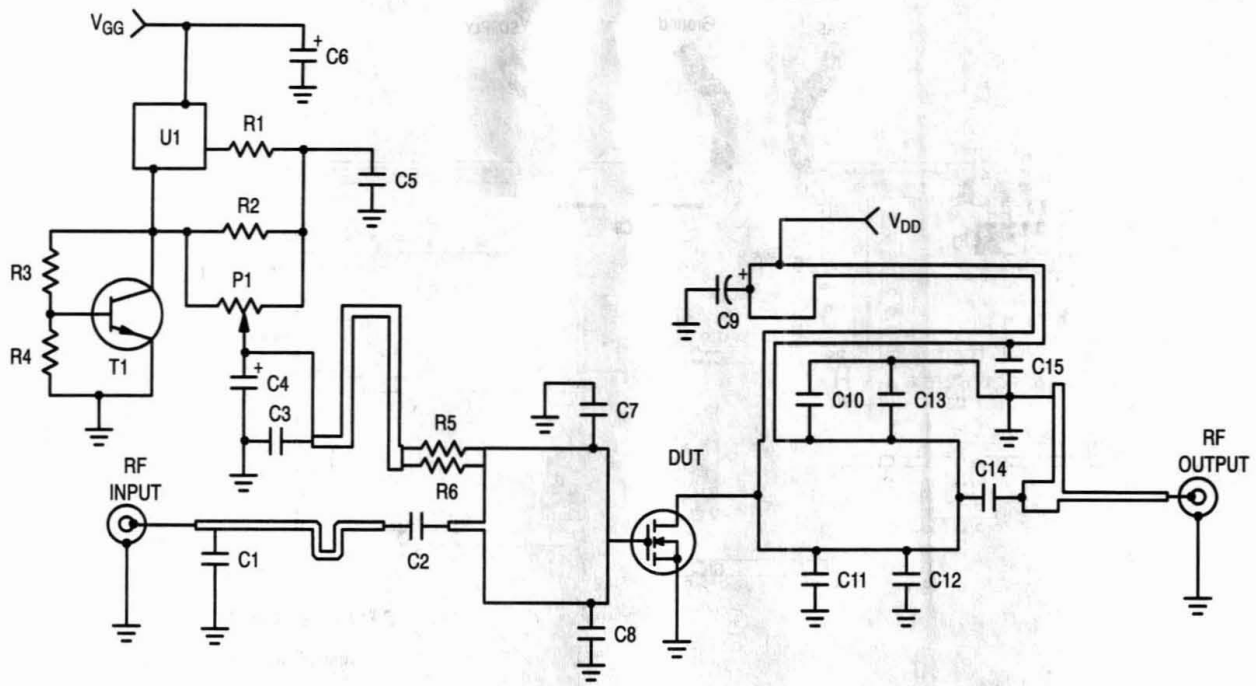


Figure 3. Broadband GSM 900 Optimized Demo Board Schematic

Table 2. Broadband GSM 900 Optimized Demo Board Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	4.7 pF Chip Capacitor, ACCU–P (0805)	#08051J3R9CBT	AVX
C2	3.9 pF Chip Capacitor, ACCU–P (0805)	#08051J3R9CBT	AVX
C3, C15	22 pF Chip Capacitors, ACCU–P (0805)	#08051J221	AVX
C4, C6	22 μF, 35 V Tantalum Chip Capacitors	#T491X226K035AS4394	Kemet
C5	1.0 μF Chip Capacitor, ACCU–P (0805)	#08053G105ZATEA	AVX
C7, C8	5.6 pF Chip Capacitors, ACCU–P (0805)	#08051J5R18CBT	AVX
C9	220 μF, 63 V Electrolytic Capacitor		
C10, C11	3.3 pF Chip Capacitors, ACCU–P (0805)	#08051J8R2CBT	AVX
C12, C13	2.2 pF Chip Capacitors, ACCU–P (0805)	#08051J2R2CBT	AVX
C14	4.7 pF Chip Capacitor	#100B	ATC
P1	5.0 kΩ Potentiometer CMS Cermet Multi–turn	#3224W	Bourns
R1	10 Ω, 1/8 W Chip Resistor (0805)		
R2	1.0 kΩ, 1/8 W Chip Resistor (0805)		
R3	1.2 kΩ, 1/8 W Chip Resistor (0805)		
R4	2.2 kΩ, 1/8 W Chip Resistor (0805)		
R5, R6	1.0 kΩ, 1/8 W Chip Resistors (0805)		
T1	Bipolar NPN Transistor, SOT–23	#BC847ALT1	ON Semiconductor
U1	Voltage Regulator, Micro–8	#LP2951ACDM–5.0R2	ON Semiconductor
	RF Connectors, Type SMA	#R125510001	Radial
	Substrate = Taconic RF35, Thickness 0.5 mm		

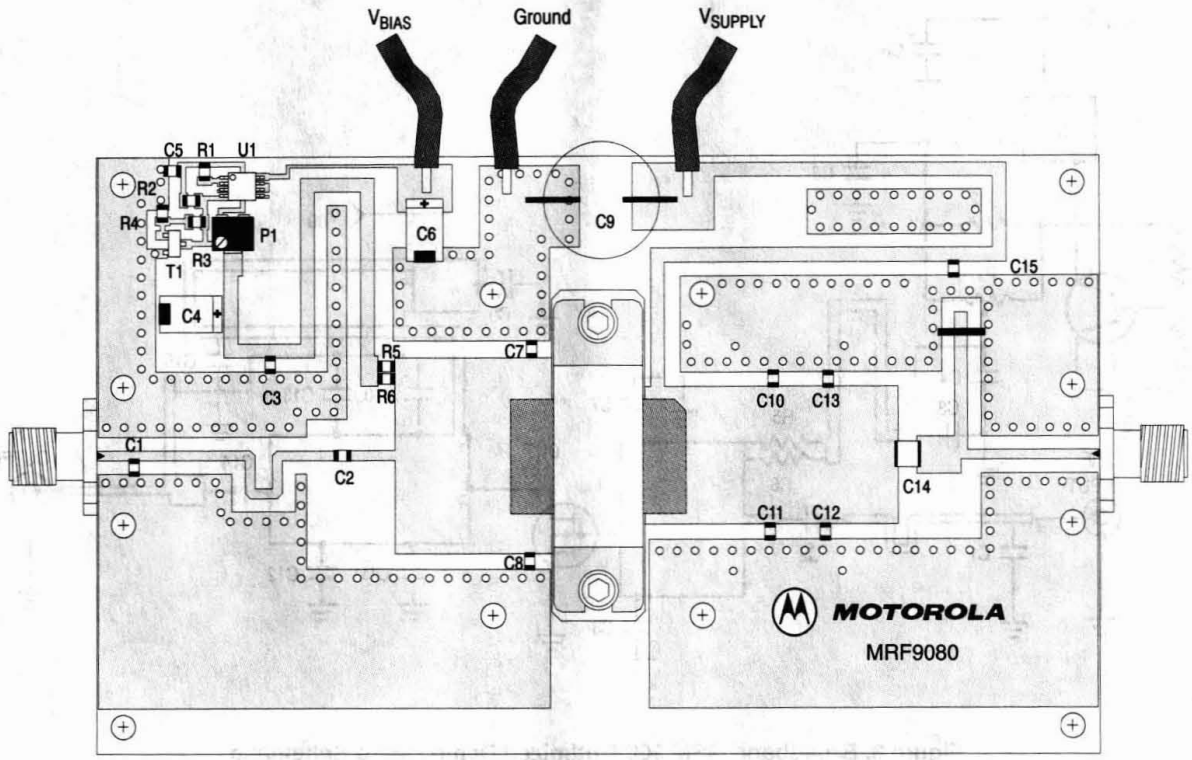


Figure 4. Broadband GSM 900 Optimized Demo Board Component Layout

TYPICAL CHARACTERISTICS
(IN MOTOROLA BROADBAND GSM 900 OPTIMIZED DEMO BOARD)

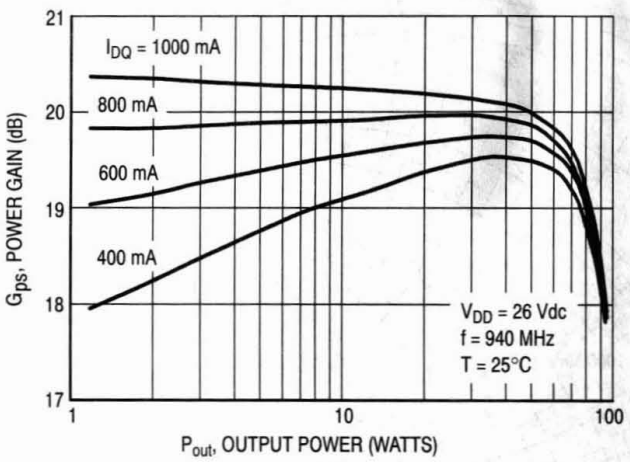


Figure 5. Power Gain versus Output Power

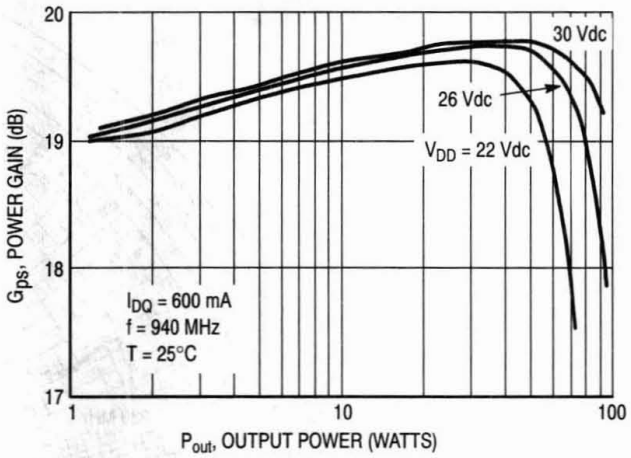


Figure 6. Power Gain versus Output Power

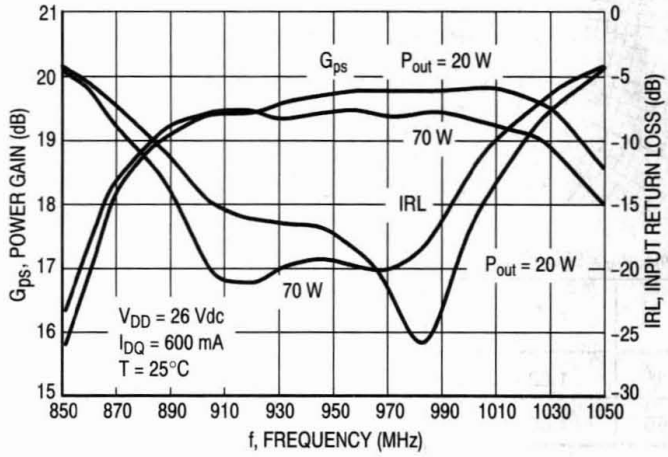


Figure 7. Power Gain and Input Return Loss versus Frequency

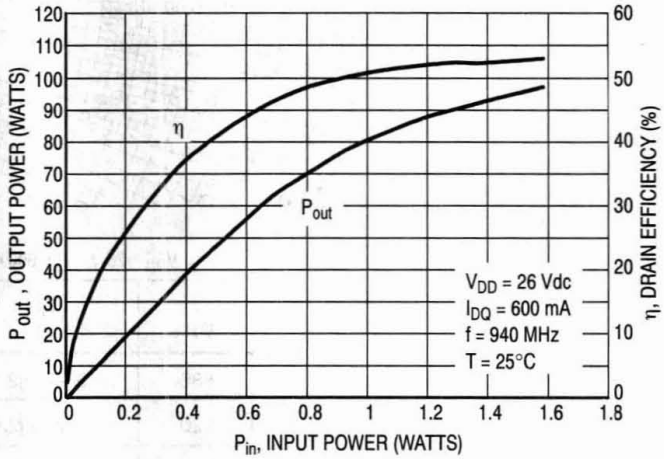


Figure 8. Output Power and Efficiency versus Input Power

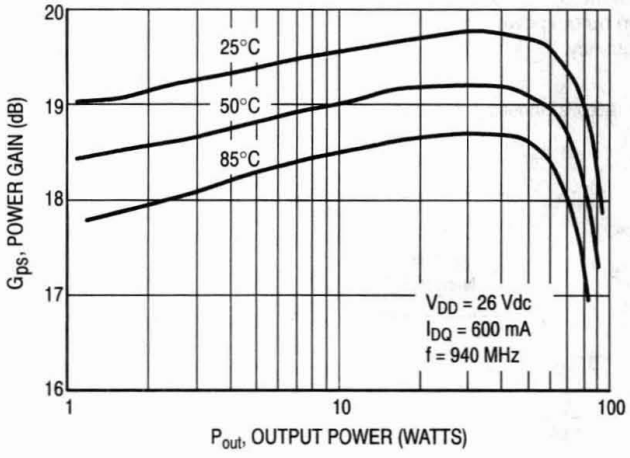


Figure 9. Power Gain versus Output Power

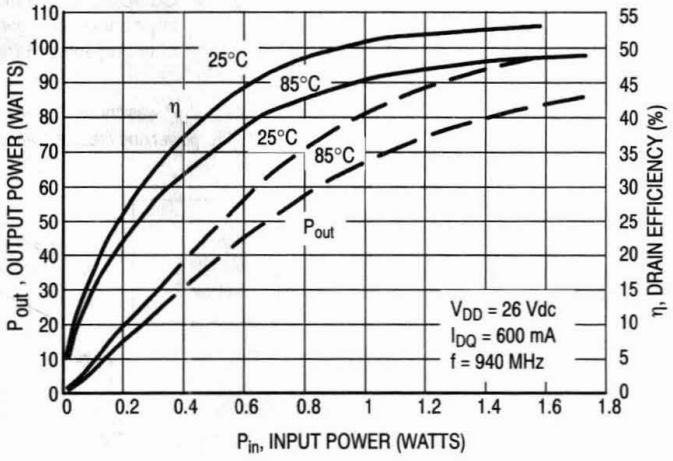
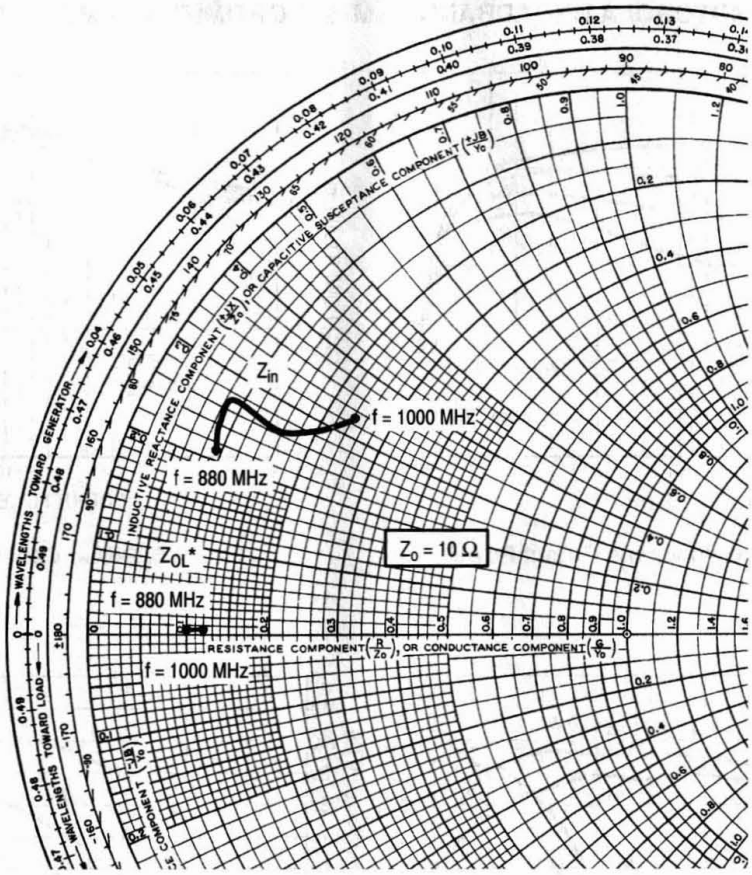


Figure 10. Output Power and Efficiency versus Input Power



V_{DD} = 26 V, I_{DQ} = 600 mA, P_{out} = 90 W (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
880	0.91 + j2.11	1.22 + j0.12
920	0.88 + j2.65	1.00 + j0.16
960	1.6 + j2.61	1.22 + j0.22
1000	2.45 + j3.38	1.14 + j0.41

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power and drain efficiency.

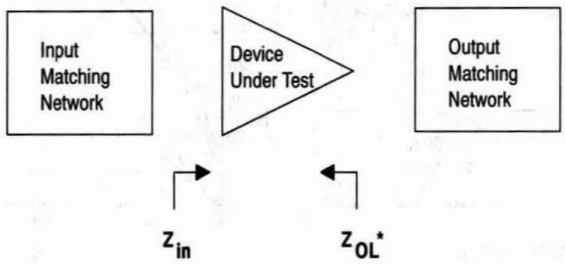


Figure 11. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

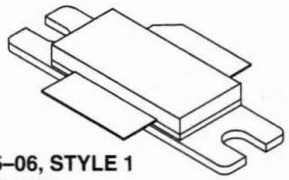
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9085
MRF9085R3
MRF9085S
MRF9085SR3
MRF9085LS
MRF9085LSR3

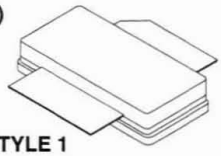
880 MHz, 90 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical CDMA Performance @ 880 MHz, 26 Volts, I_{DQ} = 700 mA
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 20 Watts
  Power Gain — 17.9 dB
  Efficiency — 28%
  Adjacent Channel Power —
  750 kHz: –45.0 dBc @ 30 kHz BW
  1.98 MHz: –60.0 dBc @ 30 kHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.



CASE 465–06, STYLE 1
(NI–780)
(MRF9085)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF9085S, MRF9085LS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions		Class
Human Body Model		1 (Minimum)
Machine Model	MRF9085	M2 (Minimum)
	MRF9085S/MRF9085LSR3	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

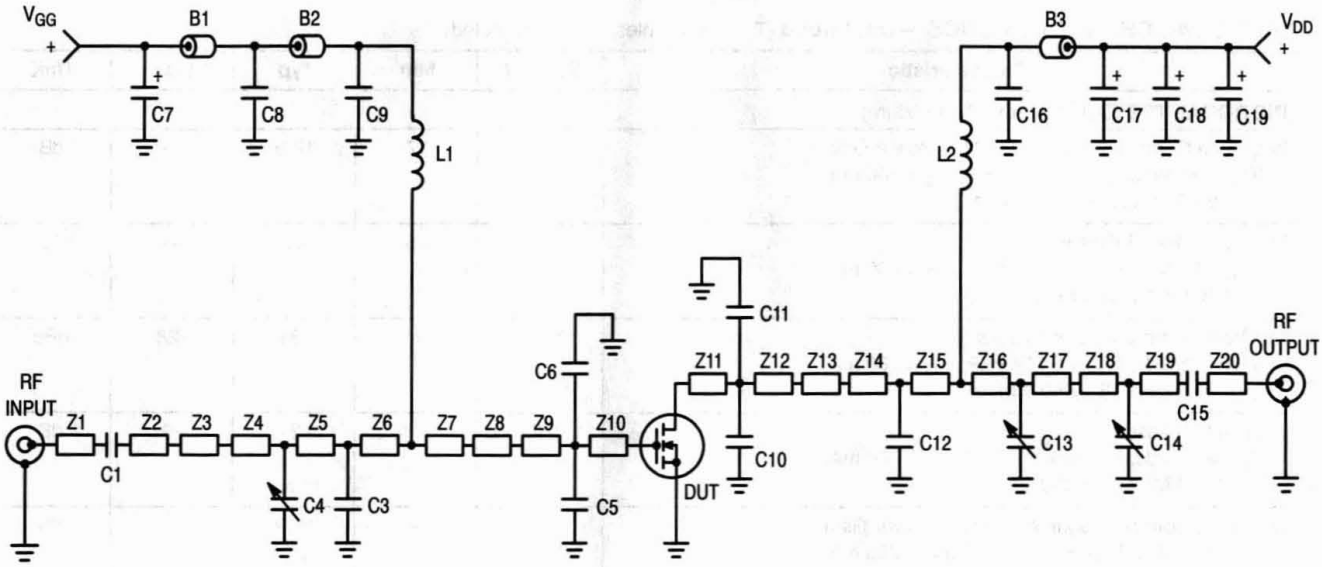
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vds, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 700 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6 Adc)	g_{fs}	—	8.0	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	73	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.9	—	pF

(1) Part is internally input matched.

(continued)

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	G_{ps}	17	17.9	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	η	36	40	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IRL	—	–21	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	G_{ps}	—	17.9	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	η	—	40.0	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	IRL	—	–16	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, CW, I_{DQ} = 700 mA, f1 = 880.0 MHz)	P_{1dB}	—	105	—	W
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 700 mA, f1 = 880.0 MHz)	G_{ps}	—	17.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 700 mA, f1 = 880.0 MHz)	η	—	51	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 700 mA, f = 880.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			



B1, B2, B3	Short Ferrite Beads, Surface Mount
C1, C9, C15, C16	47 pF Chip Capacitors, B Case , ATC
C3	5.6 pF Chip Capacitor, B Case, ATC
C4, C13	0.8 – 8.0 Variable Capacitors, Gigatrim
C5, C6, C12	10 pF Chip Capacitors, B Case, ATC
C7, C17, C18, C19	10 μF, 35 V Tantalum Surface Mount Capacitors, Kemet
C8	20 K pF Chip Capacitor, B Case, ATC
C10, C11	16 pF Chip Capacitors, B Case, ATC
C14	0.6 – 4.5 Variable Capacitor, Gigatrim
L1	7.15 nH Inductor, Coilcraft
L2	18.5 nH Inductor, Coilcraft
N1, N2	N–Type Panel Mount, Stripline, M/A–Com
WB1, WB2	5 Mil BeCu Shim (0.225 x 0.525)
Z1	0.219″ x 0.080″ Microstrip
Z2	0.150″ x 0.080″ Microstrip
Z3	0.851″ x 0.080″ Microstrip
Z4	0.125″ x 0.220″ Microstrip
Z5	0.123″ x 0.220″ Microstrip
Z6	0.076″ x 0.220″ Microstrip
Z7	0.261″ x 0.220″ Microstrip
Z8	0.220″ x 0.630″ x 0.200″ Taper
Z9	0.240″ x 0.630″ Microstrip
Z10	0.060″ x 0.630″ Microstrip
Z11	0.067″ x 0.630″ Microstrip
Z12	0.233″ x 0.630″ Microstrip
Z13	0.630″ x 0.220″ x 0.200″ Taper
Z14	0.200″ x 0.220″ Microstrip
Z15	0.055″ x 0.220″ Microstrip
Z16	0.088″ x 0.220″ Microstrip
Z17	0.226″ x 0.220″ Microstrip
Z18	0.868″ x 0.080″ Microstrip
Z19	0.129″ x 0.080″ Microstrip
Z20	0.223″ x 0.080″ Microstrip
PCB	Etched Circuit Board, Glass, Teflon® $\varepsilon_r = 2.55$, 30 Mils

Figure 1. 865–895 MHz Broadband Test Circuit Schematic

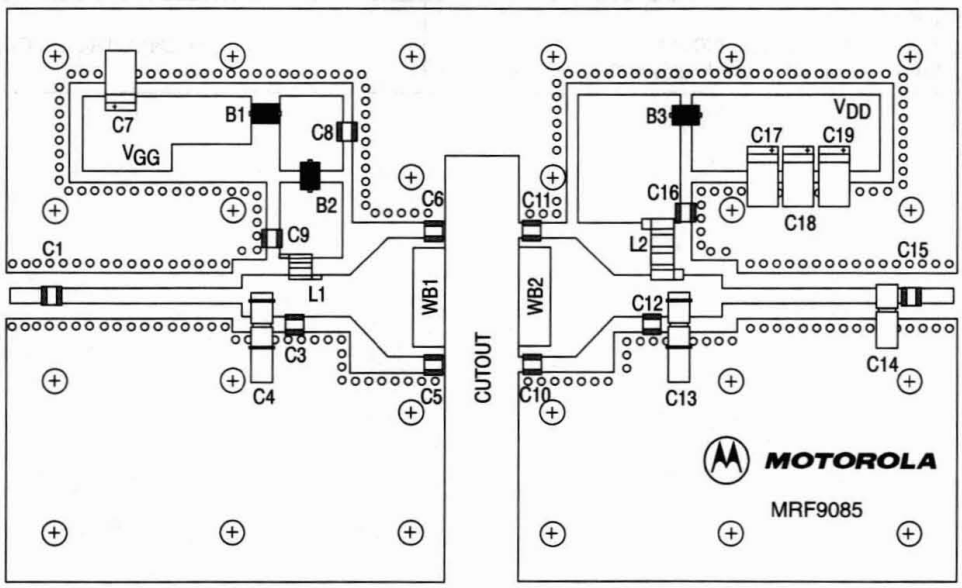


Figure 2. 865–895 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

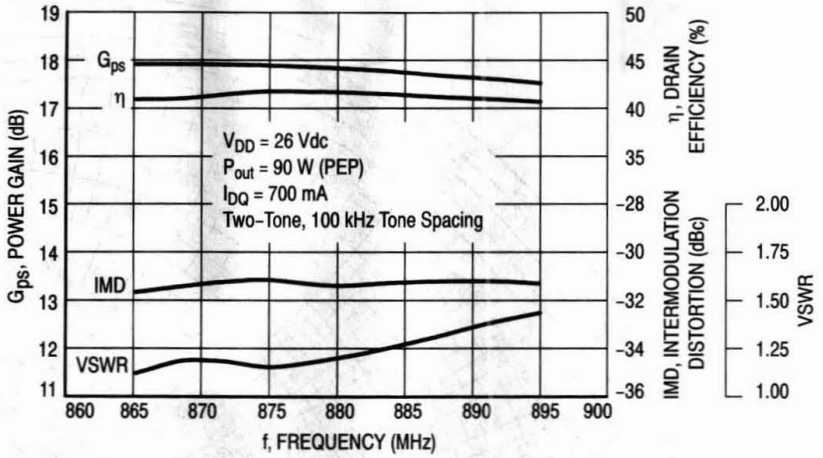


Figure 3. Class AB Broadband Circuit Performance

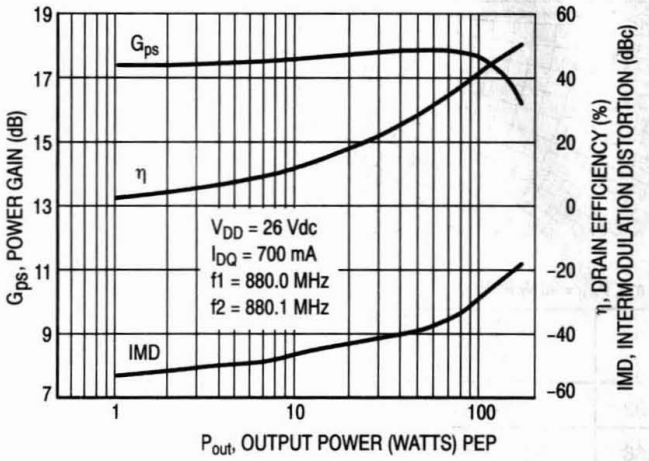


Figure 4. Power Gain, Efficiency, IMD versus Output Power

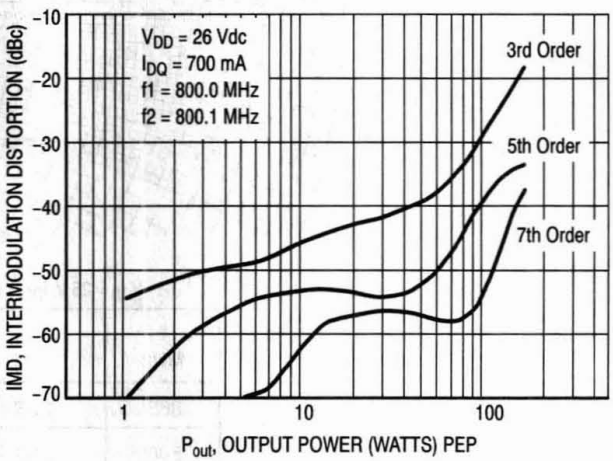


Figure 5. Intermodulation Distortion Products versus Output Power

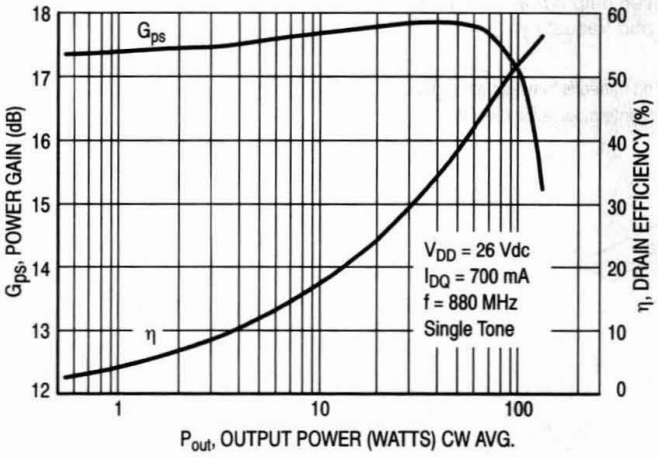


Figure 6. Power Gain, Efficiency versus Output Power

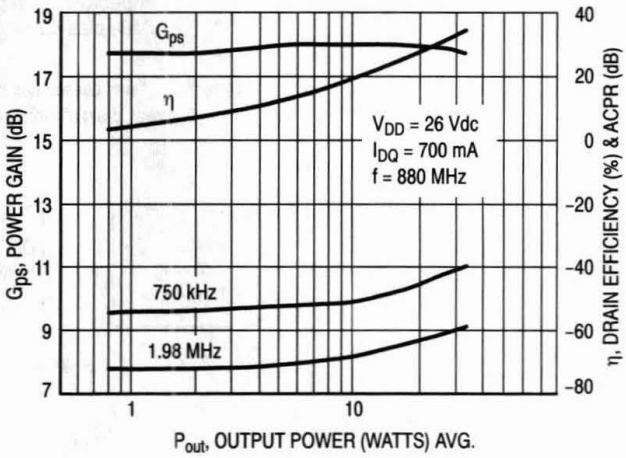
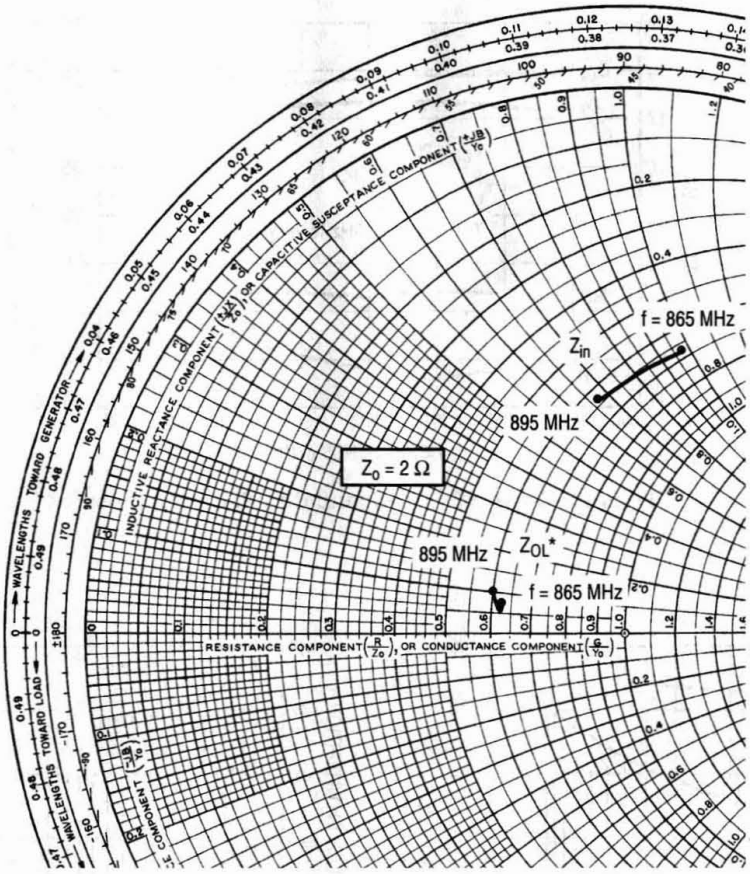


Figure 7. Power Gain, Efficiency, ACPR versus Output Power



V_{DD} = 26 V, I_{DQ} = 700 mA, P_{out} = 90 W PEP

f MHz	Z_{in} Ω	Z_{OL}* Ω
865	1.35 + j1.92	1.26 + j0.15
880	1.33 + j1.66	1.26 + j0.10
895	1.28 + j1.30	1.21 + j0.20

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

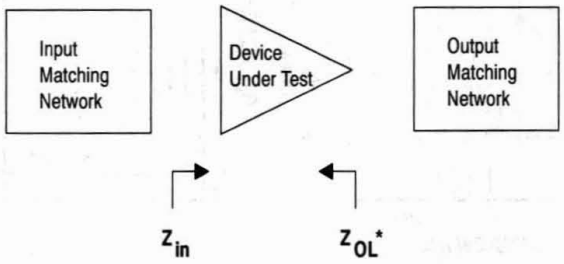


Figure 8. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

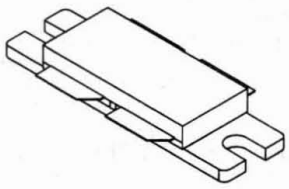
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9120
MRF9120S

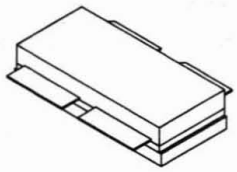
880 MHz, 120 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large–signal, common source amplifier applications in 26 volt base station equipment.

- Typical CDMA Performance @ 880 MHz, 26 Volts, I_{DQ} = 2 x 500 mA
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 26 Watts
  Power Gain — 16 dB
  Efficiency — 26%
  Adjacent Channel Power —
  750 kHz: –45 dBc @ 30 kHz BW
  1.98 MHz: –60 dBc @ 30 kHz BW
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 120 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 375B–04, STYLE 1
(NI–860)
(MRF9120)



CASE 375H–03, STYLE 1
(NI–860S)
(MRF9120S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, – 0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 450 mAdc)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.3 Adc)	$V_{DS(on)}$	—	0.17	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	g_{fs}	—	5.3	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	50	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2	—	pF

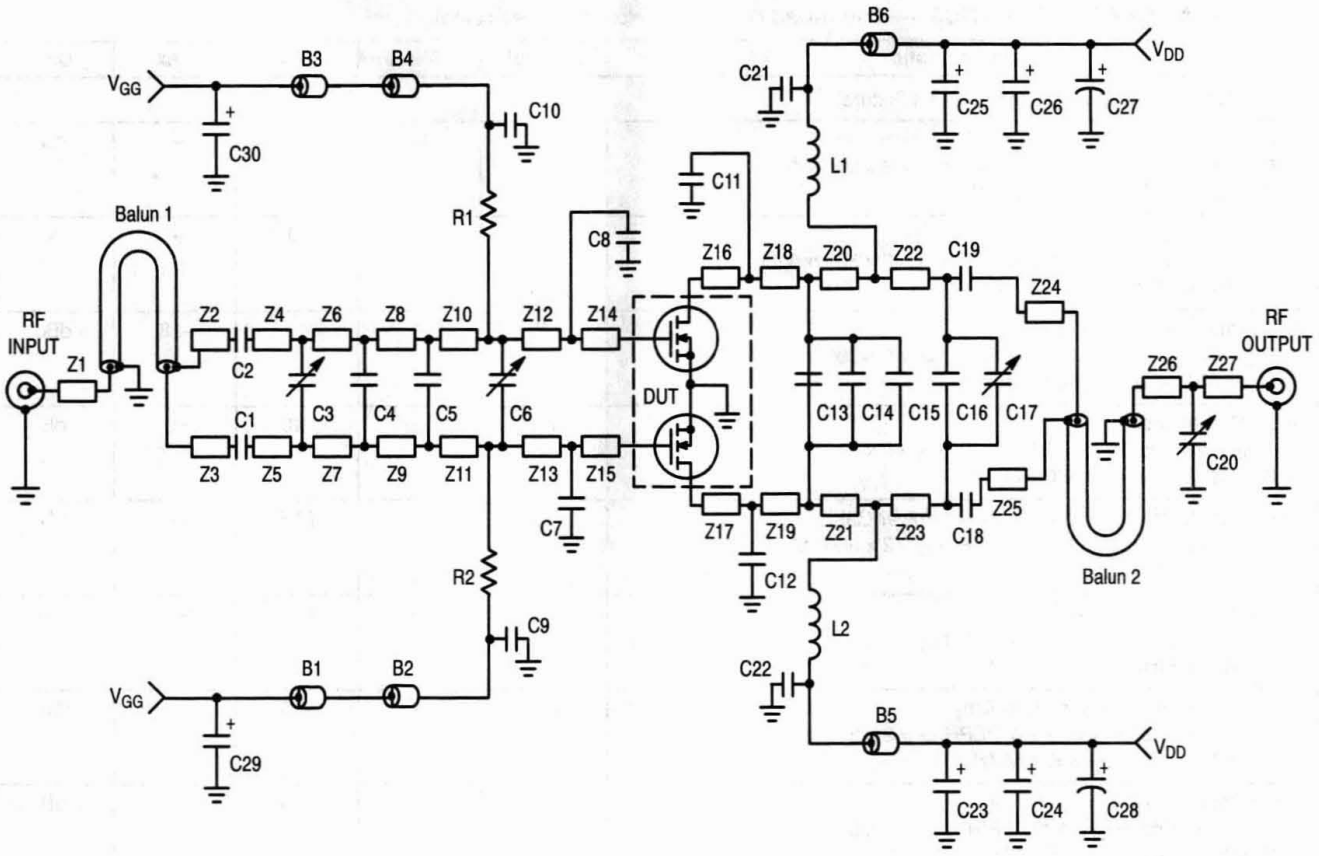
(1) Each side of device measured separately.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	G_{ps}	15	16.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	η	36	39	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IRL	—	–16	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 895.0 MHz, f2 = 895.1 MHz)	G_{ps}	—	16.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 895.0 MHz, f2 = 895.1 MHz)	η	—	40.5	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 895.0 MHz, f2 = 895.1 MHz)	IMD	—	–30	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 x 500 mA, f1 = 895.0 MHz, f2 = 895.1 MHz)	IRL	—	–13	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz)	P_{1dB}	—	120	—	W
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz)	G_{ps}	—	16	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 500 mA, f1 = 880.0 MHz)	η	—	51	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 x 500 mA, f = 880.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			

(2) Device measured in push–pull configuration.



Z1	0.420″ x 0.080″ Microstrip	Z14, Z15	0.040″ x 0.630″ Microstrip
Z2, Z3	0.090″ x 0.420″ Microstrip	Z16, Z17	0.040″ x 0.630″ Microstrip
Z4, Z5	0.125″ x 0.220″ Microstrip	Z18, Z19	0.330″ x 0.630″ Microstrip
Z6, Z7	0.095″ x 0.220″ Microstrip	Z20, Z21	0.450″ x 0.630″ Microstrip
Z8, Z9	0.600″ x 0.220″ Microstrip	Z22, Z23	0.750″ x 0.220″ Microstrip
Z10, Z11	0.200″ x 0.630″ Microstrip	Z24, Z25	0.115″ x 0.420″ Microstrip
Z12, Z13	0.500″ x 0.630″ Microstrip	Z26	0.130″ x 0.080″ Microstrip
		Z27	0.350″ x 0.080″ Microstrip

Figure 1. 880 MHz Broadband Test Circuit Schematic

Table 1. 880 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1, B3, B5, B6	Long Ferrite Beads, Surface Mount	95F787	Newark
B2, B4	Short Ferrite Beads, Surface Mount	95F786	Newark
C1, C2	68 pF Chip Capacitors, B Case	100B680JP500X	ATC
C3, C6	0.8 – 8.0 pF Variable Capacitors	44F3360	Newark
C4	7.5 pF Chip Capacitor, B Case	100B7R5JP150X	ATC
C5	3.3 pF Chip Capacitor, B Case	100B3R3CP150X	ATC
C7, C8	11 pF Chip Capacitors, B Case	100B110BCA500X	ATC
C9, C10, C21, C22	51 pF Chip Capacitors, B Case	100B510JP500X	ATC
C11, C12	6.2 pF Chip Capacitors, B Case	100B6R2BCA150X	ATC
C13	4.7 pF Chip Capacitor, B Case	100B4R7BCA150X	ATC
C14	5.1 pF Chip Capacitor, B Case	100B5R1BCA150X	ATC
C15	3.0 pF Chip Capacitor, B Case	100B2R7BCA150X	ATC
C16	2.7 pF Chip Capacitor, B Case	100B3R0BCA150X	ATC
C17	0.6 – 4.5 pF Variable Capacitor	44F3358	Newark
C18, C19	47 pF Chip Capacitors, B Case	100B470JP500X	ATC
C20	0.4 – 2.5 pF Variable Capacitor	44F3367	Newark
C29, C30	10 μF, 35 V Tantalum Chip Capacitors	93F2975	Newark
C23, C24, C25, C26	22 μF, 35 V Tantalum Chip Capacitors	92F1853	Newark
C27, C28	220 μF, 50 V Electrolytic Capacitors	14F185	Newark
Balun 1, Balun 2	Xinger Surface Mount Balun Transformers	3A412	Anaren
L1, L2	12.5 nH Mini Spring Inductors	A04T–5	Coilcraft
R1, R2	510 Ω, 1/4 W Chip Resistors		Garret
WB1, WB2, WB3, WB4	10 mil Brass Wear Blocks		
Board Material	30 mil Glass Teflon®, ε_r = 2.55 Copper Clad, 2 oz Cu	900 MHz Push–Pull Rev 01B	CMR
PCB	Etched Circuit Board	900 MHz Push–Pull Rev 01B	CMR

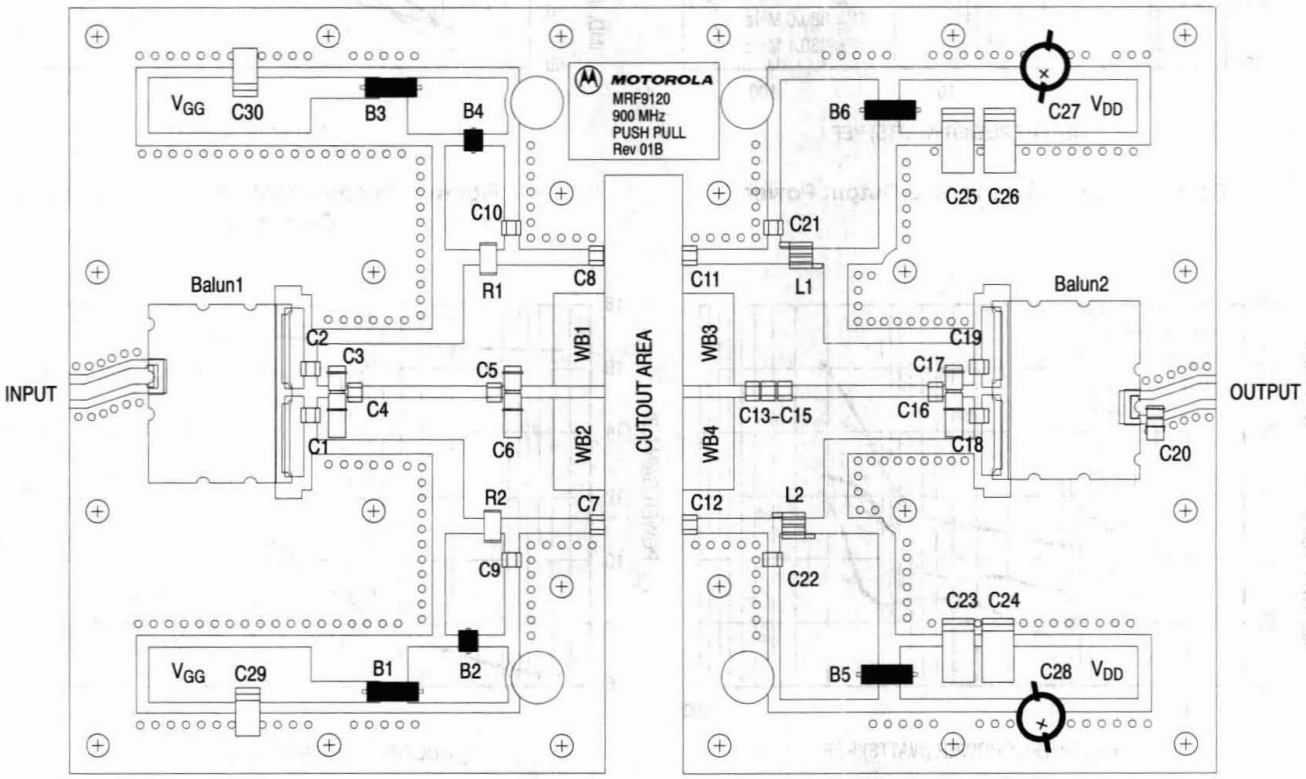


Figure 2. 865–895 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

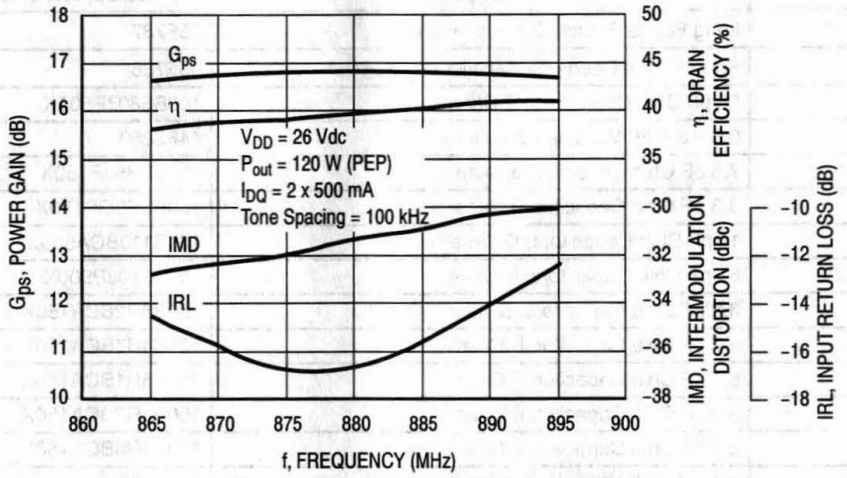


Figure 3. Class AB Broadband Circuit Performance

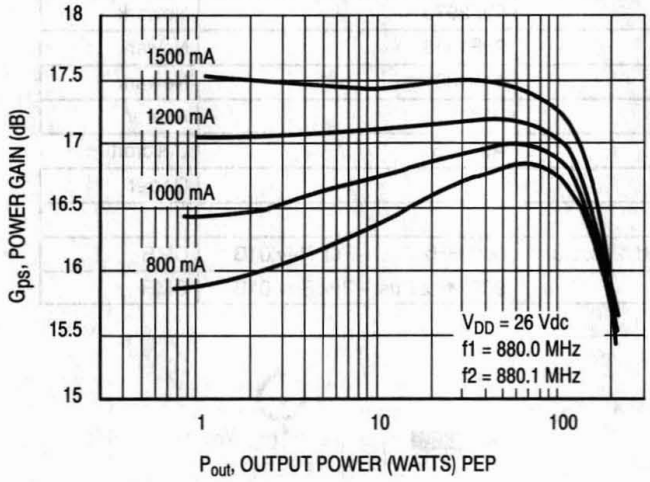


Figure 4. Power Gain versus Output Power

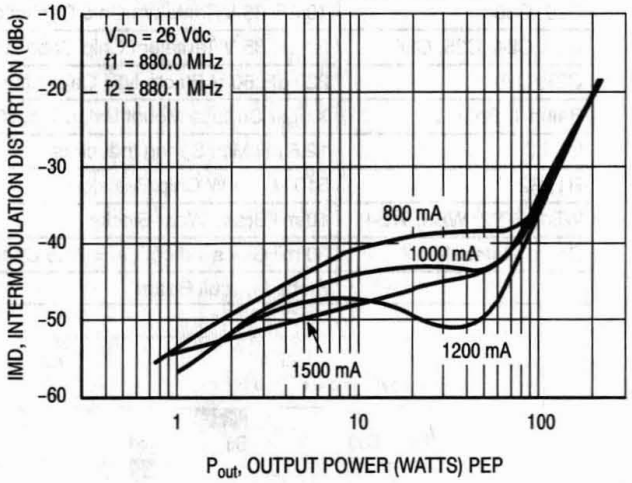


Figure 5. Intermodulation Distortion versus Output Power

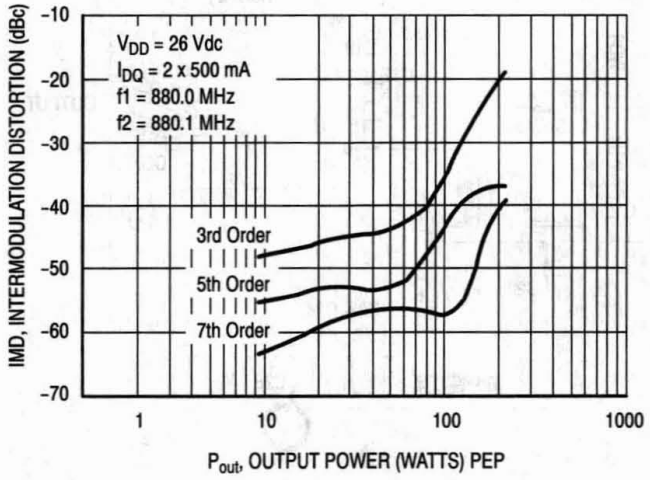


Figure 6. Intermodulation Distortion Products versus Output Power

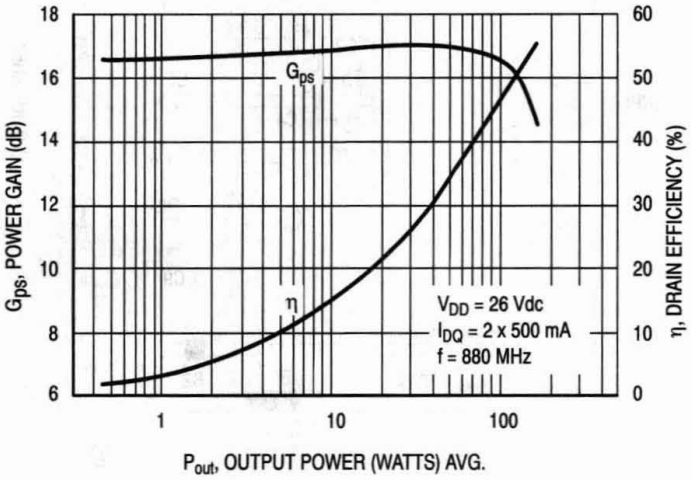


Figure 7. Power Gain and Efficiency versus Output Power

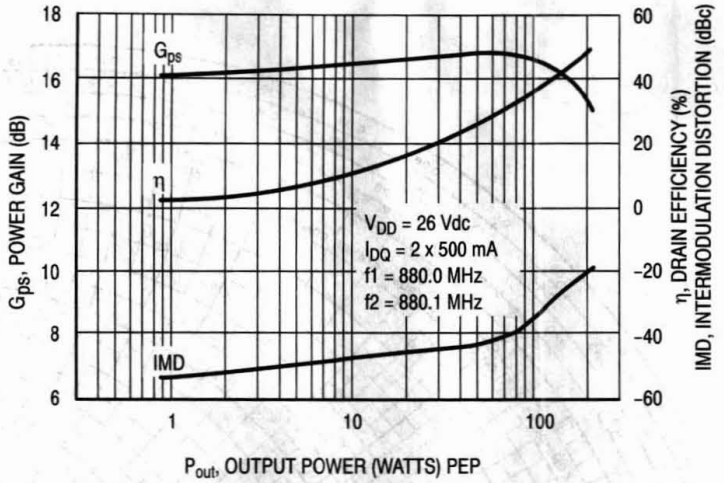


Figure 8. Power Gain, Efficiency and IMD versus Output Power

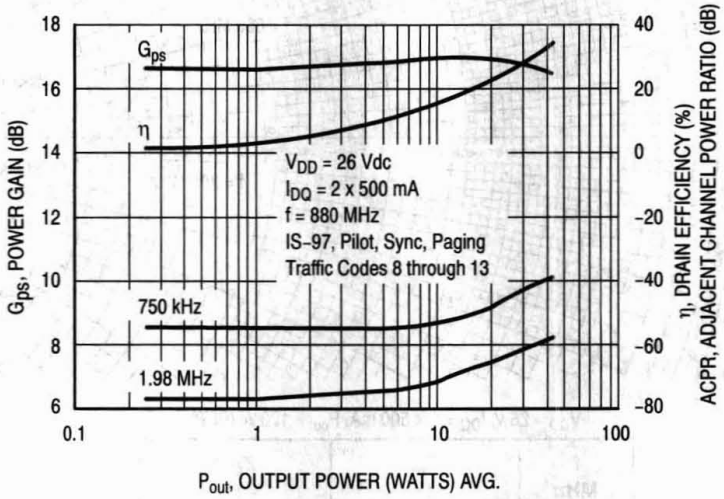
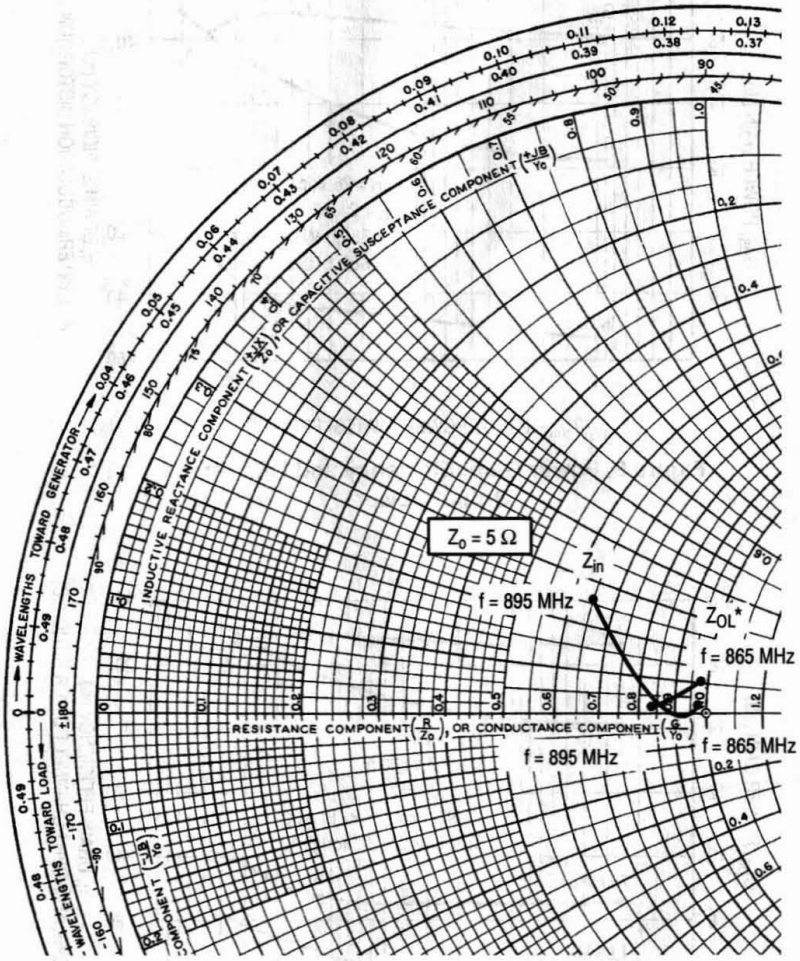


Figure 9. Power Gain, Efficiency and ACPR versus Output Power



V_{DD} = 26 V, I_{DQ} = 2 × 500 mA, P_{out} = 120 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
865	4.89 + j0.2	4.9 + j0.5
880	4.54 – j0.07	4.6 + j0.32
895	3.29 + j1.3	4.2 + j0.04

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

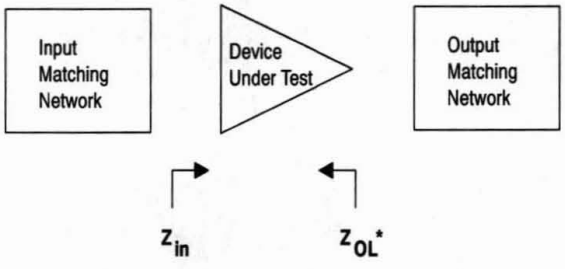


Figure 10. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

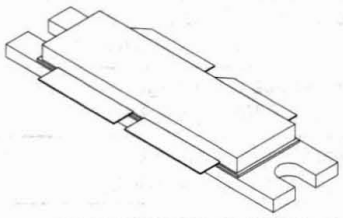
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9180
MRF9180S

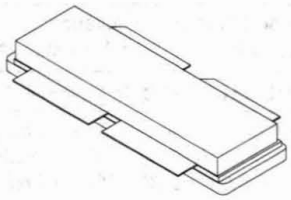
880 MHz, 170 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical CDMA Performance @ 880 MHz, 26 Volts, I_{DQ} = 2 × 700 mA
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 40 Watts
  Power Gain — 17 dB
  Efficiency — 26%
  Adjacent Channel Power –
  750 kHz: –45.0 dBc @ 30 kHz BW
  1.98 MHz: –60.0 dBc @ 30 kHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 170 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 375D–04, STYLE 1
(NI–1230)
(MRF9180)



CASE 375E–03, STYLE 1
(NI–1230S)
(MRF9180S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	388 2.22	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 5

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

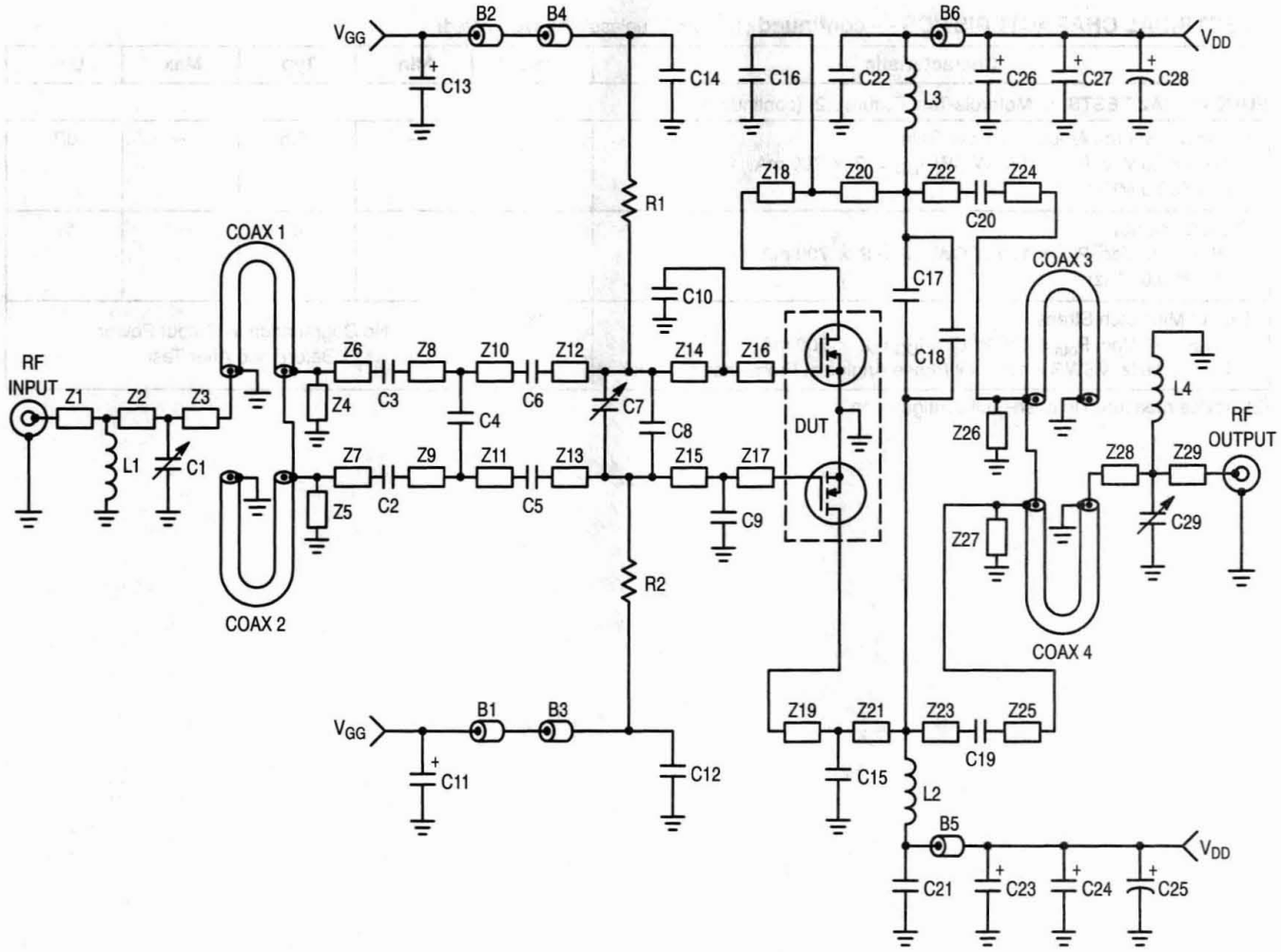
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 700 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.19	0.5	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6 Adc)	g_{fs}	—	6	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	77	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	3.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 170 W PEP, I_{DQ} = 2 × 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	G_{ps}	16	17.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 170 W PEP, I_{DQ} = 2 × 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	η	35	39	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 170 W PEP, I_{DQ} = 2 × 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 170 W PEP, I_{DQ} = 2 × 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IRL	—	–15	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 170 W PEP, I_{DQ} = 2 × 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	G_{ps}	—	17.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 170 W PEP, I_{DQ} = 2 × 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	η	—	38.5	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 170 W PEP, I_{DQ} = 2 × 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 170 W PEP, I_{DQ} = 2 × 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	IRL	—	–13	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, CW, I_{DQ} = 2 × 700 mA, f1 = 880.0 MHz)	P_{1dB}	—	170	—	W

(1) Each side of device measured separately.
(2) Device measured in push–pull configuration.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture) (2) (continued)					
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 170 W CW, I_{DQ} = 2 × 700 mA, f1 = 880.0 MHz)	G_{ps}	—	16.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 170 W CW, I_{DQ} = 2 × 700 mA, f1 = 880.0 MHz)	η	—	55	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 170 W CW, I_{DQ} = 2 × 700 mA, f = 880 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(2) Device measured in push–pull configuration.



B1, B2, B5, B6	Long Ferrite Beads, Surface Mount	Z1	0.420″ x 0.080″ Microstrip
B3, B4	Short Ferrite Beads, Surface Mount	Z2	0.190″ x 0.080″ Microstrip
C1	0.6–4.5 pF Variable Capacitor	Z3	0.097″ x 0.080″ Microstrip
C2, C3, C5, C6, C12, C14, C19, C20, C21, C22	47 pF Chip Capacitors, B Case	Z4, Z5, Z26, Z27	2.170″ x 0.080″ Microstrip
		Z6, Z7	0.075″ x 0.080″ Microstrip
C4, C9, C10, C15, C16	12 pF Chip Capacitors, B Case	Z8, Z9	0.088″ x 0.220″ Microstrip
C7	0.8–9.1 pF Variable Capacitor	Z10, Z11	0.088″ x 0.220″ Microstrip
C8	7.5 pF Chip Capacitor, B Case	Z12, Z13	0.460″ x 0.220″ Microstrip
C11, C13	10 μF, 35 V Tantalum Surface Mount Chip Capacitors	Z14, Z15	0.685″ x 0.625″ Microstrip
C17	3.6 pF Chip Capacitor, B Case	Z16, Z17	0.055″ x 0.625″ Microstrip
C18	5.1 pF Chip Capacitor, B Case	Z18, Z19	0.055″ x 0.632″ Microstrip
C23, C24, C26, C27	22 μF, 35 V Tantalum Surface Mount Chip Capacitors	Z20, Z21	0.685″ x 0.632″ Microstrip
C25, C28	220 μF, 50 V Electrolytic Capacitors	Z22, Z23	0.732″ x 0.080″ Microstrip
C29	0.4–2.5 pF Variable Capacitor	Z24, Z25	0.060″ x 0.080″ Microstrip
Coax1, Coax2	25 Ω, Semi Rigid Coax, 70 mil OD, 1.05″ Long	Z28	0.230″ x 0.080″ Microstrip
Coax3, Coax4	50 Ω, Semi Rigid Coax, 85 mil OD, 1.05″ Long	Z29	0.460″ x 0.080″ Microstrip
L1, L2, L3	18.5 nH Mini Spring Inductors, Coilcraft	Board Material	30 mil Teflon®, εr = 2.55, Copper Clad, 2 oz Cu
L4	12.5 nH Mini Spring Inductor, Coilcraft		
R1, R2	510 Ω, 1/10 W Chip Resistors		

Figure 1. 880 MHz Broadband Test Circuit Schematic

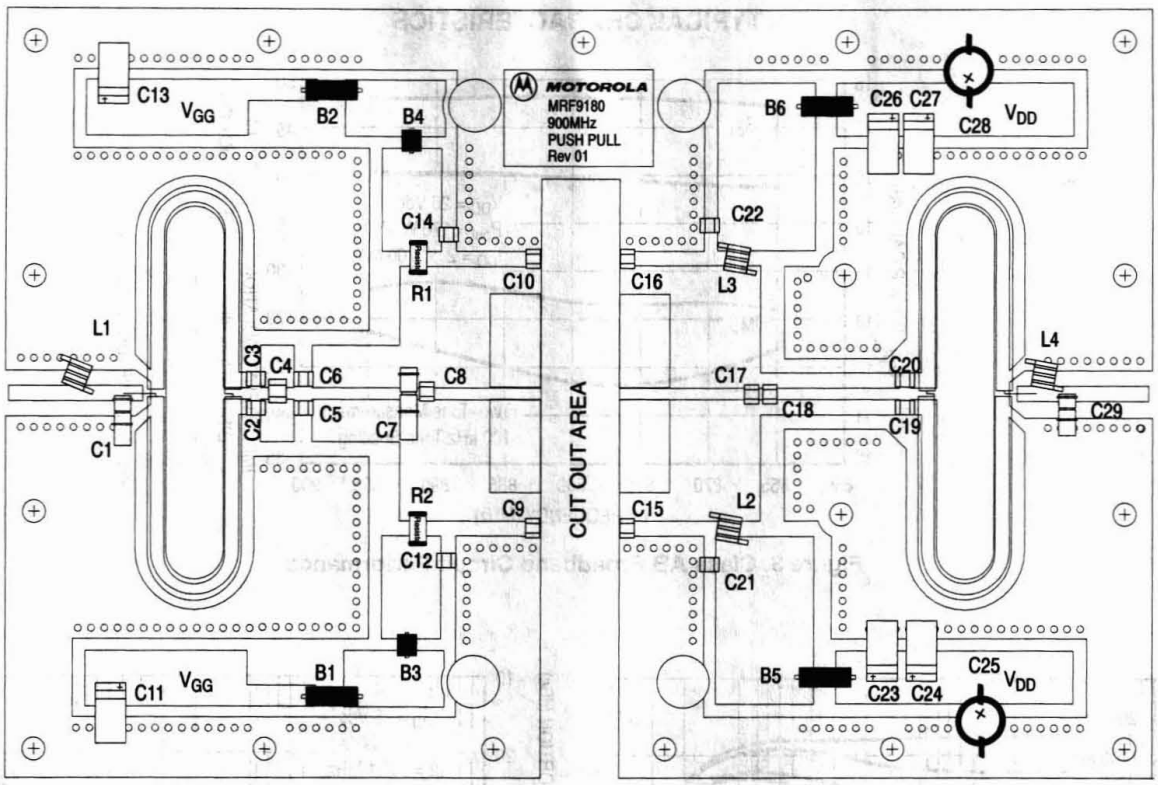


Figure 2. 880 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

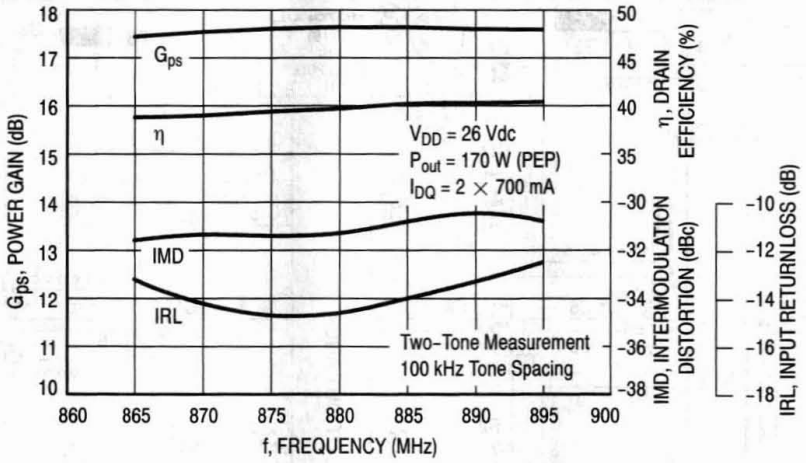


Figure 3. Class AB Broadband Circuit Performance

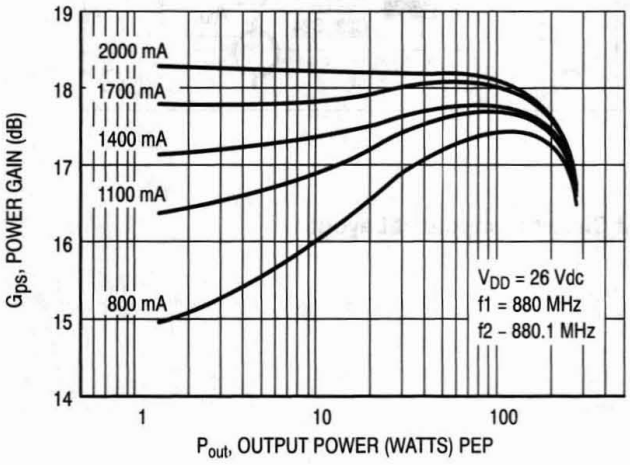


Figure 4. Power Gain versus Output Power

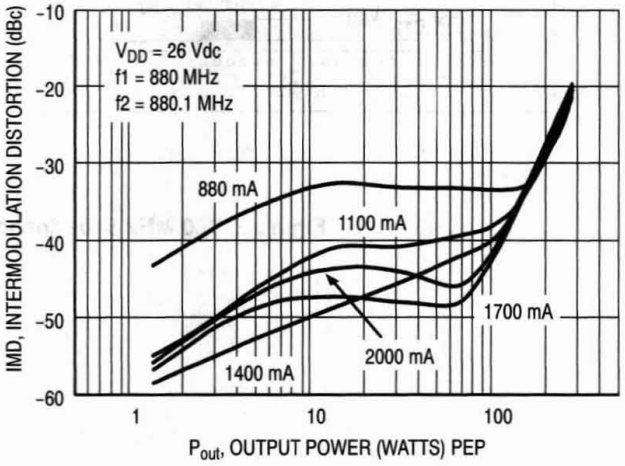


Figure 5. Intermodulation Distortion versus Output Power

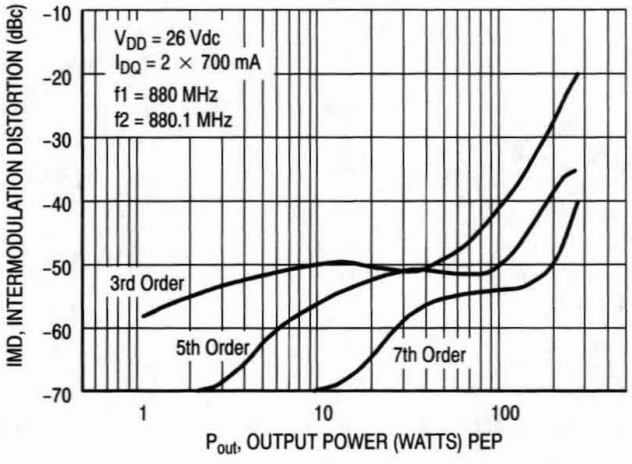


Figure 6. Intermodulation Distortion Products versus Output Power

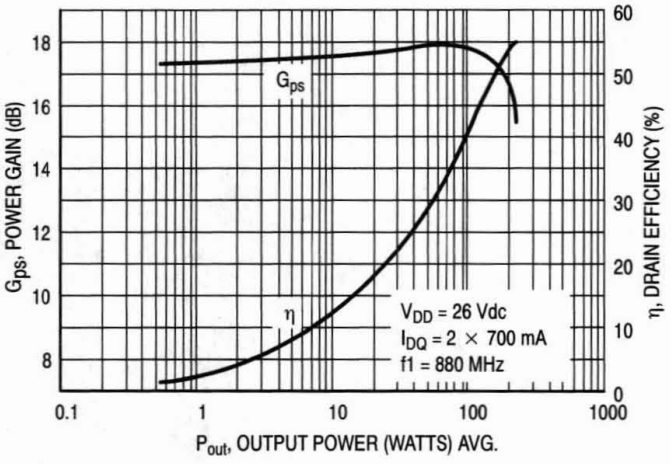


Figure 7. Power Gain and Efficiency versus Output Power

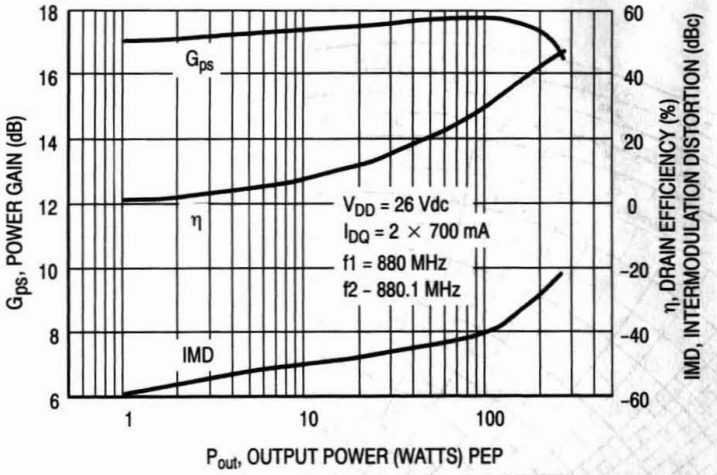


Figure 8. Power Gain, Efficiency and IMD versus Output Power

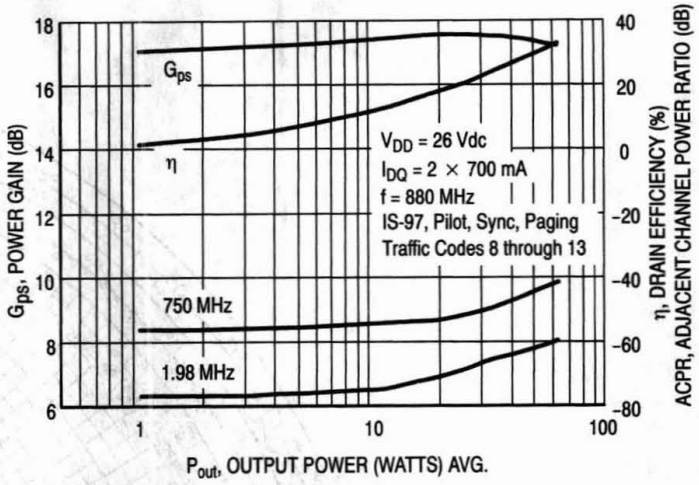
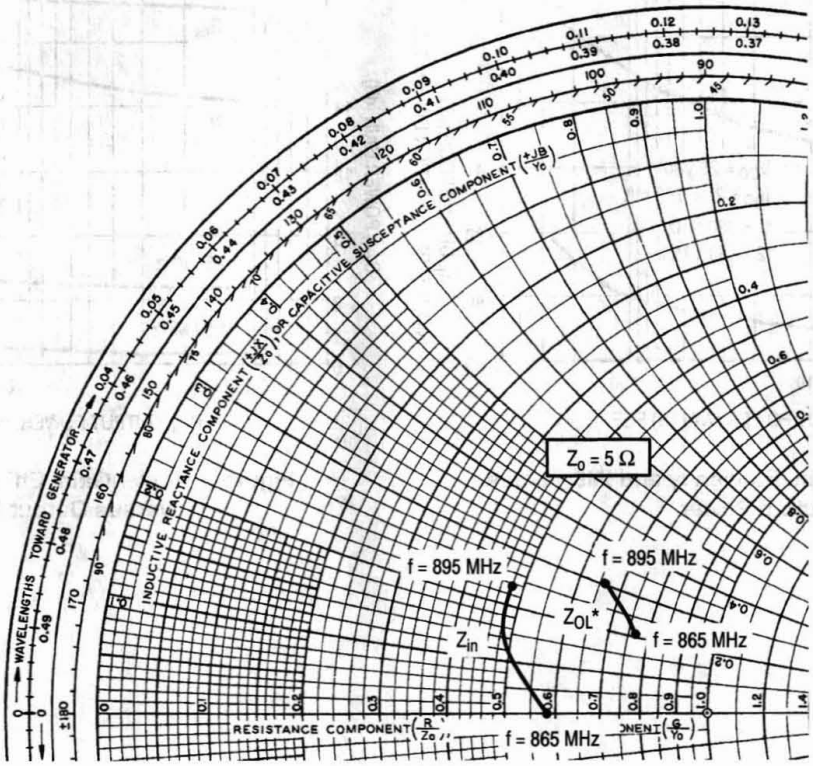


Figure 9. Power Gain, Efficiency and ACPR versus Output Power



V_{DD} = 26 V, I_{DQ} = 2 × 700 mA, P_{out} = 170 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
865	2.95 + j0.00	3.83 + j1.02
880	2.48 + j0.67	3.55 + j1.38
895	2.44 + j1.18	3.34+ j1.51

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

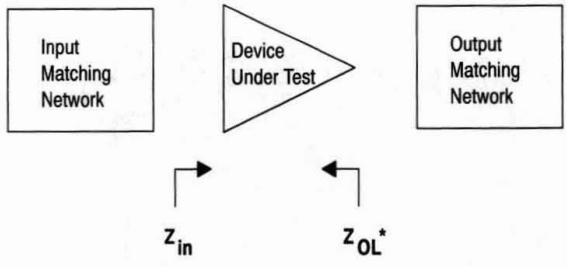


Figure 10. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

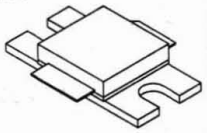
Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. Specified for GSM 1805 – 1880 MHz.

- Typical GSM Performance:
  Power Gain – 14 dB (Typ) @ 30 Watts
  Efficiency – 50% (Typ) @ 30 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 30 W Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

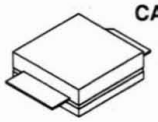
MRF18030A
MRF18030AR3
MRF18030AS
MRF18030ASR3

GSM/GSM EDGE 1.8 – 1.88 GHz, 30 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

CASE 465E–03, STYLE 1
(NI–400)
(MRF18030A)



CASE 465F–03, STYLE 1
(NI–400S)
(MRF18030AS)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83.3 0.48	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

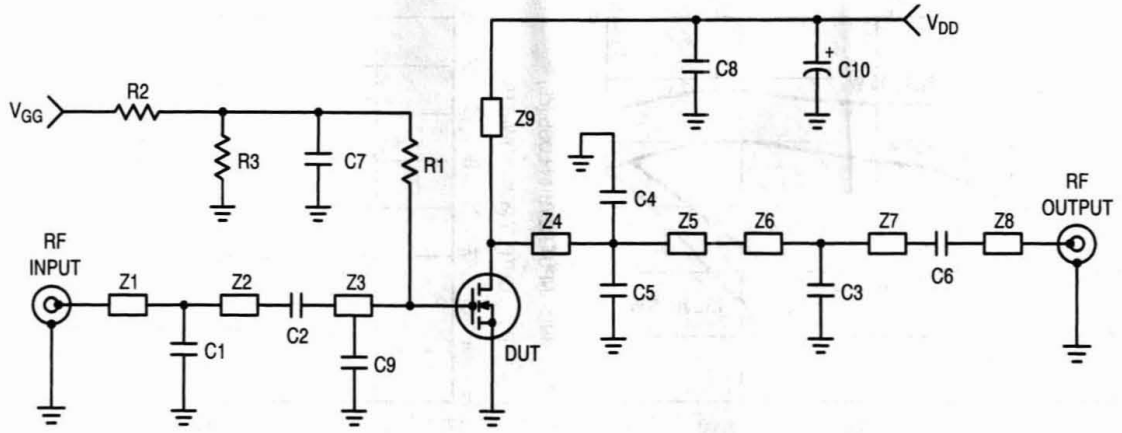
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 250 mAdc)	$V_{GS(Q)}$	2	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)					
Output Power, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1805 – 1880 MHz)	P1dB	27	30	—	Watts
Common–Source Amplifier Power Gain @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1805 – 1880 MHz)	G_{ps}	13	14	—	dB
Drain Efficiency @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1805 – 1880 MHz)	η	46.5	50	—	%
Input Return Loss @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1805 – 1880 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f1 = 1805 – 1880 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.
(2) Device specifications obtained on a Production Test Fixture.



C1	1.8 pF, 100B Chip Capacitor	Z1	0.874″ x 0.087″ Microstrip
C2	0.8 pF, 100B Chip Capacitor	Z2	1.094″ x 0.087″ Microstrip
C3	1.0 pF, 100B Chip Capacitor	Z3	0.257″ x 0.633″ Microstrip
C4, C5	1.2 pF, 100B Chip Capacitors	Z4	0.189″ x 0.394″ Microstrip
C6, C7, C8	8.2 pF, 100B Chip Capacitors	Z5	0.335″ x 0.394″ Microstrip
C9	0.3 pF, 100B Chip Capacitor	Z6	0.484″ x 0.087″ Microstrip
C10	220 μF, 63 V Electrolytic Capacitor	Z7	0.877″ x 0.087″ Microstrip
R1	1.0 kΩ, 1/8 W Chip Resistor (0805)	Z8	0.366″ x 0.087″ Microstrip
R2, R3	10 kΩ, 1/8 W Chip Resistors (0805)	Z9	≈0.600″ x 0.087″ Microstrip

Figure 1. 1805 – 1880 MHz Test Fixture Schematic

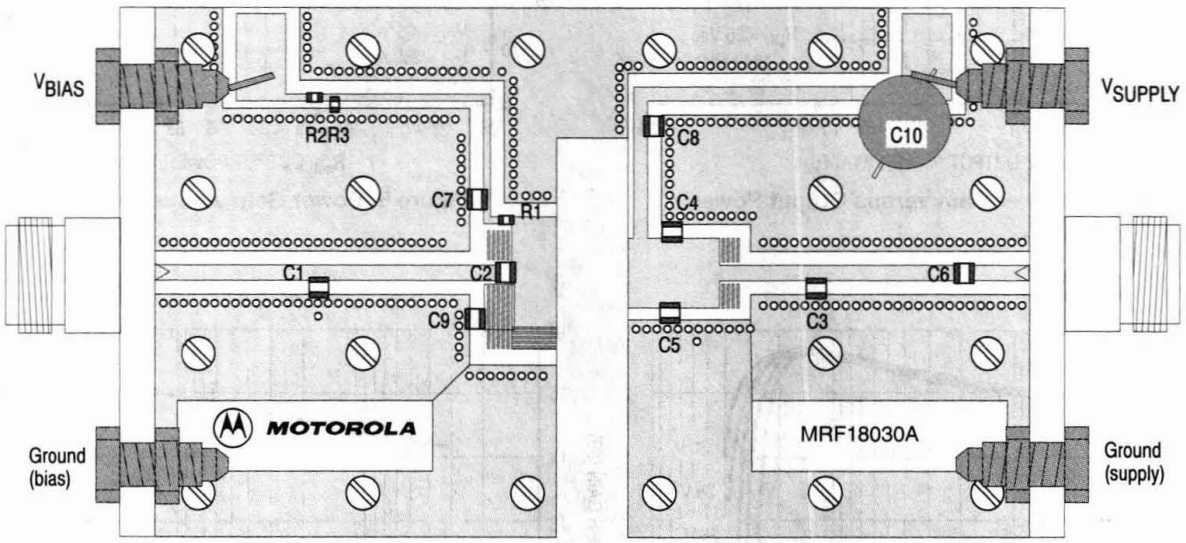


Figure 2. 1805 – 1880 MHz Test Fixture Component Layout

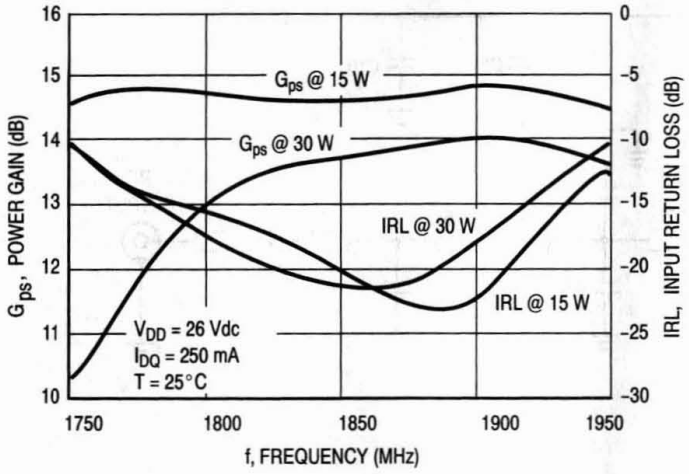


Figure 3. Wideband Gain and IRL at 30 W and 15 W Output Power

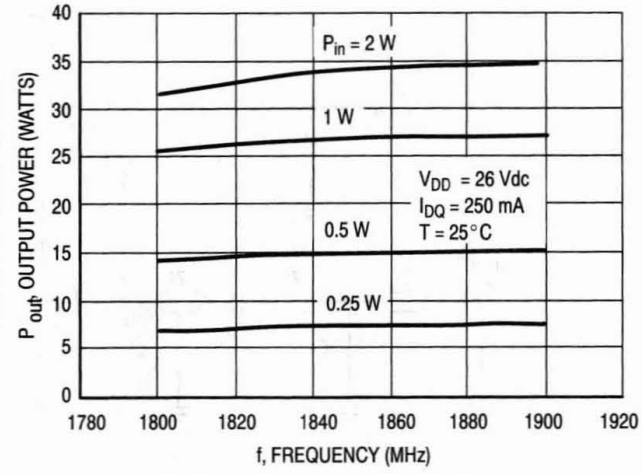


Figure 4. Output Power versus Frequency

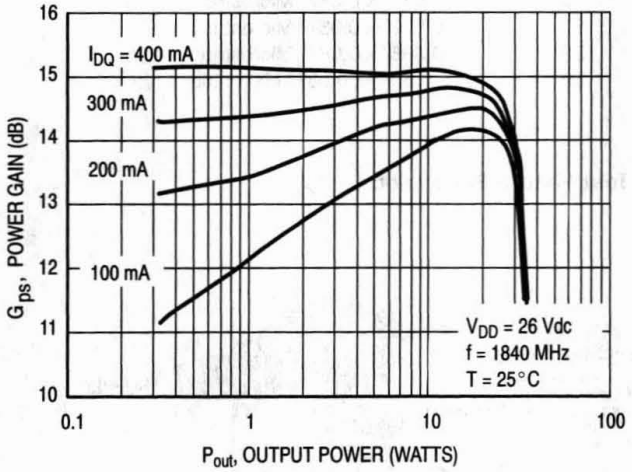


Figure 5. Power Gain versus Output Power

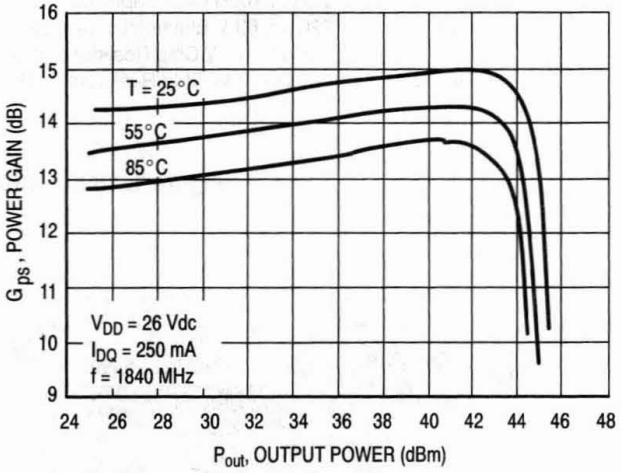


Figure 6. Power Gain versus Output Power

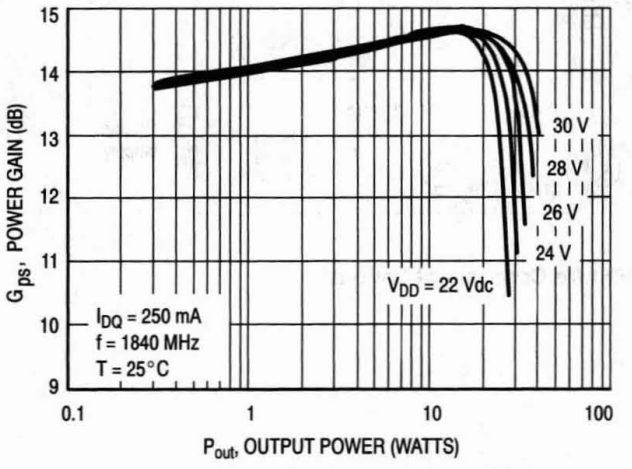


Figure 7. Power Gain versus Output Power

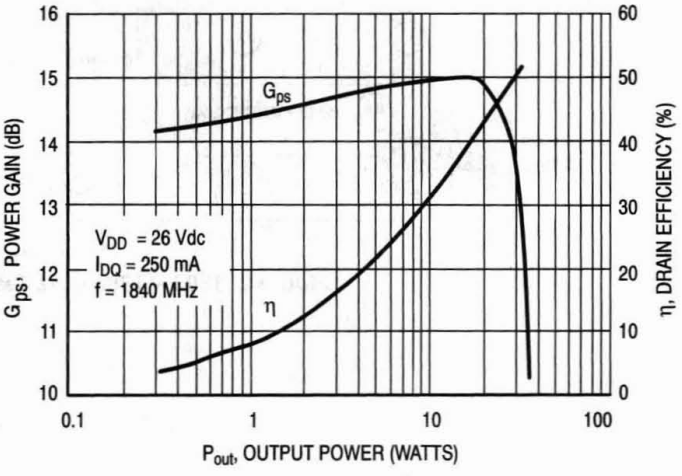
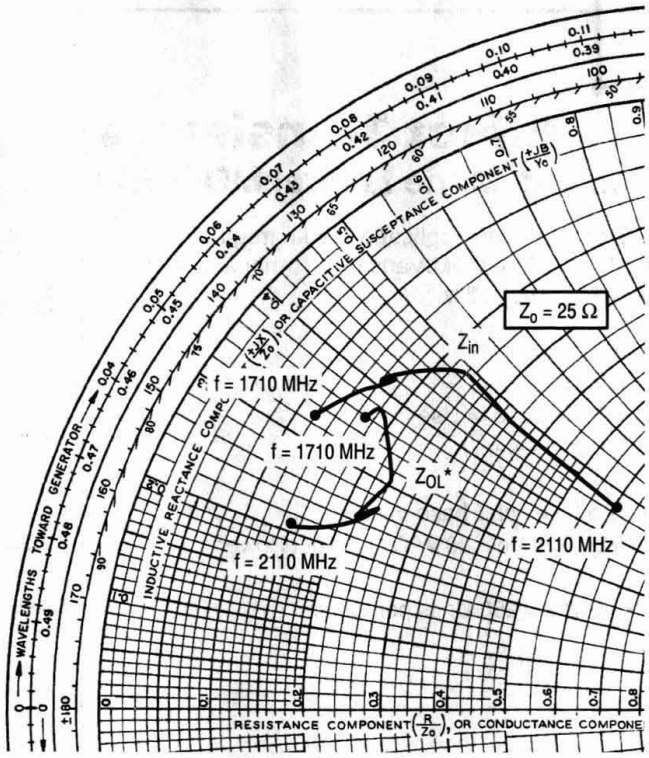


Figure 8. Power Gain and Efficiency versus Output Power



V_{DD} = 26 V, I_{DQ} = 250 mA, P_{out} = 30 W (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1710	2.92 + j8.24	4.18 + j9.06
1785	3.84 + j9.75	4.59 + j9.46
1805	4.15 + j10.38	4.98 + j9.06
1840	4.04 + j10.22	6.10 + j7.63
1880	6.12 + j12.29	5.83 + j6.89
1960	6.20 + j12.29	5.55 + j6.33
1990	8.61 + j12.10	5.93 + j6.66
2110	15.19 + j11.85	3.82 + j5.33

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given power, voltage, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, and drain efficiency.

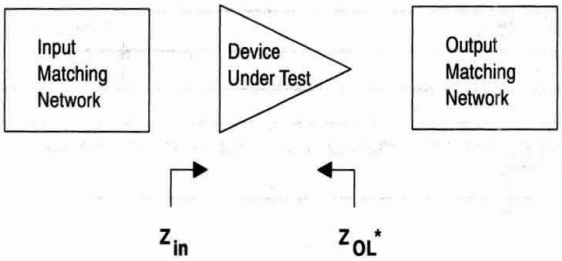


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

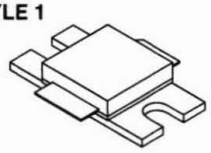
Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. Specified for GSM 1930 – 1990 MHz.

- Typical GSM Performance:
  Power Gain – 14 dB (Typ) @ 30 Watts
  Efficiency – 50% (Typ) @ 30 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 30 W CW Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

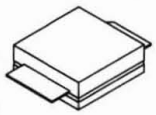
MRF18030B
MRF18030BR3
MRF18030BS
MRF18030BSR3

GSM/GSM EDGE 1.93 – 1.99 GHz, 30 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

CASE 465E–03, STYLE 1
(NI–400)
(MRF18030B)



CASE 465F–03, STYLE 1
(NI–400S)
(MRF18030BS)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83.3 0.48	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

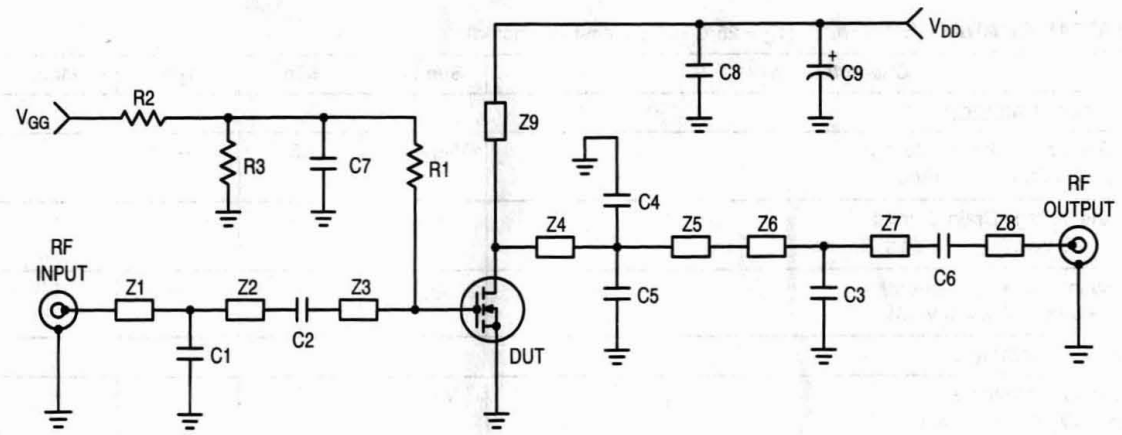
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 250 mAdc)	$V_{GS(Q)}$	2	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)					
Output Power, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1930 – 1990 MHz)	P1dB	27	30	—	Watts
Common–Source Amplifier Power Gain @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1930 – 1990 MHz)	G_{ps}	13	14	—	dB
Drain Efficiency @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1930 – 1990 MHz)	η	46.5	50	—	%
Input Return Loss @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f = 1930 – 1990 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress @ 30 W (V_{DD} = 26 Vdc, I_{DQ} = 250 mA, f1 = 1930 – 1990 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.
(2) Device specifications obtained on a Production Test Fixture.



C1	1.8 pF, 100B Chip Capacitor	Z2	1.022″ x 0.087″ Microstrip
C2	0.8 pF, 100B Chip Capacitor	Z3	0.257″ x 0.633″ Microstrip
C3	0.8 pF, 100B Chip Capacitor	Z4	0.189″ x 0.394″ Microstrip
C4, C5	1.2 pF, 100B Chip Capacitors	Z5	0.335″ x 0.394″ Microstrip
C6, C7, C8	8.2 pF, 100B Chip Capacitors	Z6	0.616″ x 0.087″ Microstrip
C9	220 μF, 63 V Electrolytic Capacitor	Z7	0.845″ x 0.087″ Microstrip
R1	1.0 kΩ, 1/8 W Chip Resistor (0805)	Z8	0.366″ x 0.087″ Microstrip
R2, R3	10 kΩ, 1/8 W Chip Resistors (0805)	Z9	≈0.500″ x 0.087″ Microstrip
Z1	0.496″ x 0.087″ Microstrip		

Figure 1. 1930 – 1990 MHz Test Fixture Schematic

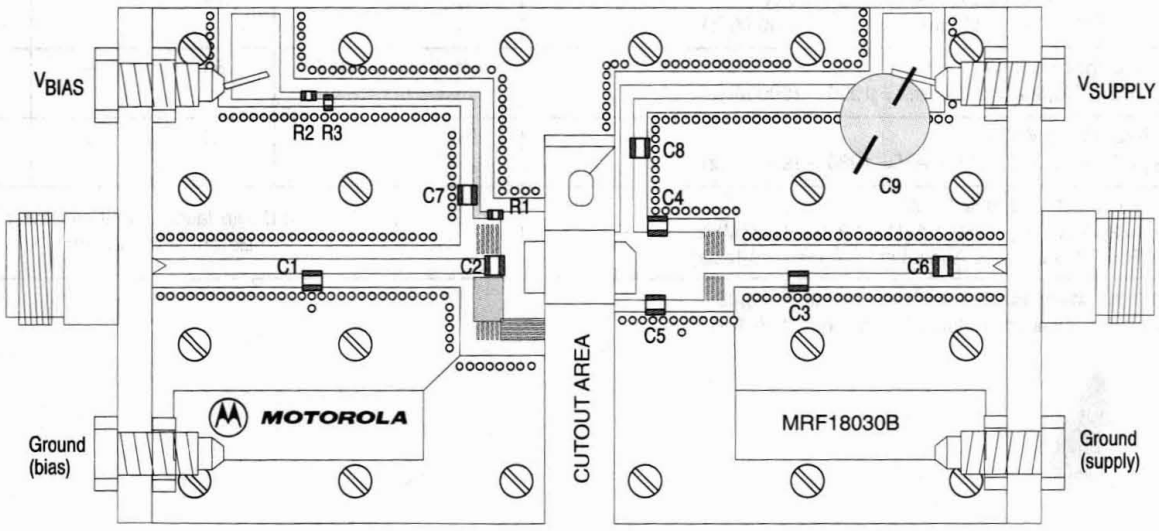


Figure 2. 1930 – 1990 MHz Test Fixture Component Layout

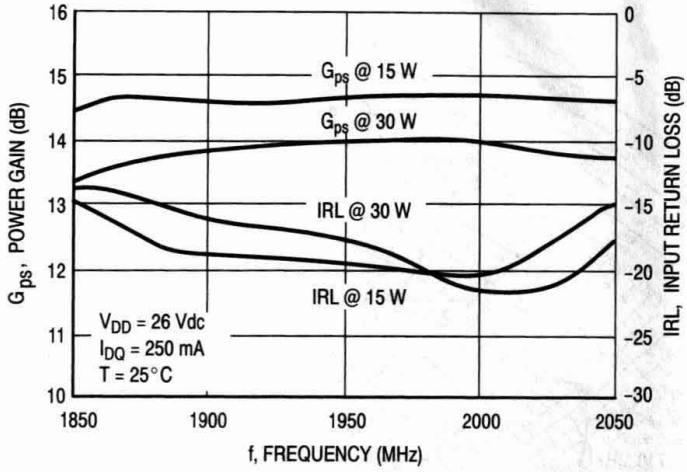


Figure 3. Wideband Gain and IRL at 30 W and 15 W Output Power

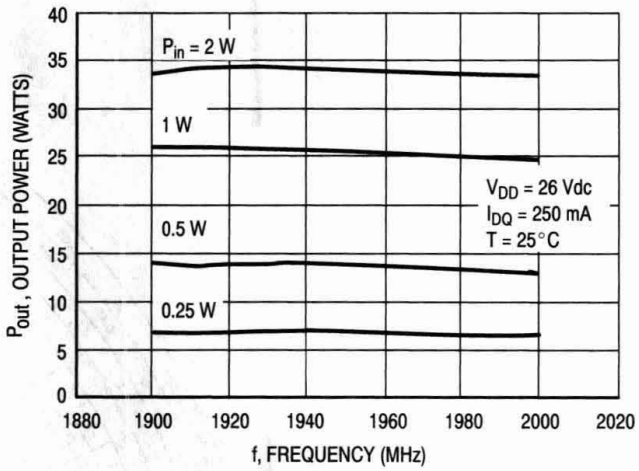


Figure 4. Output Power versus Frequency

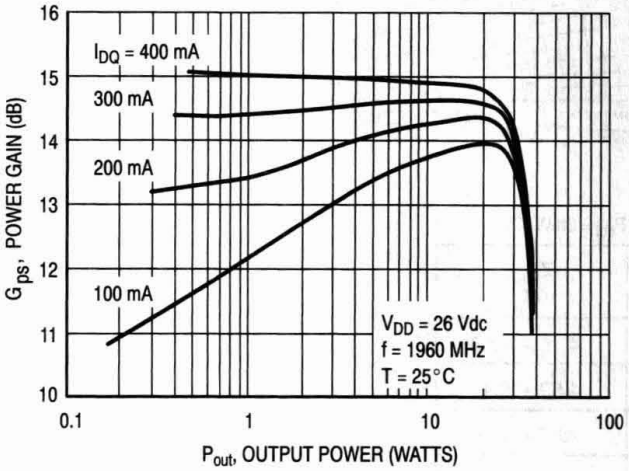


Figure 5. Power Gain versus Output Power

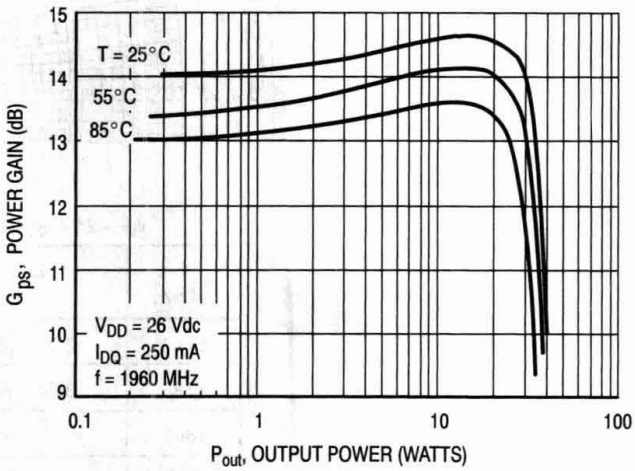


Figure 6. Power Gain versus Output Power

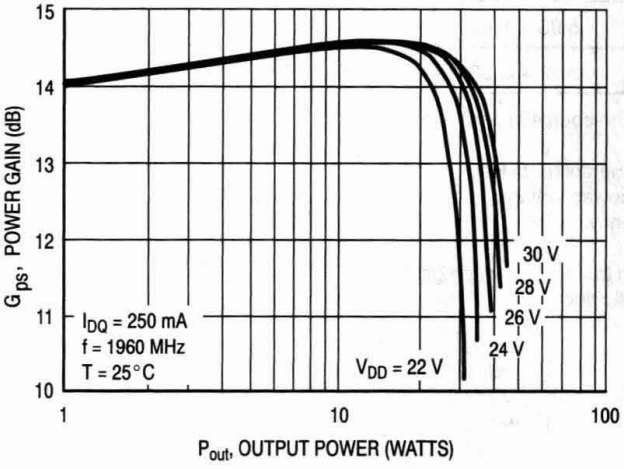


Figure 7. Power Gain versus Output Power

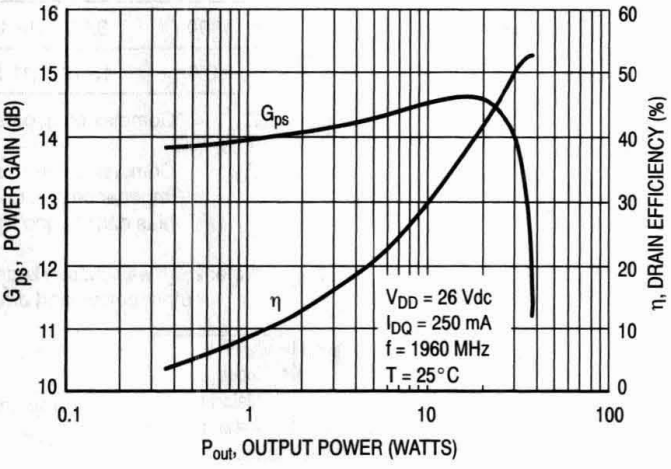
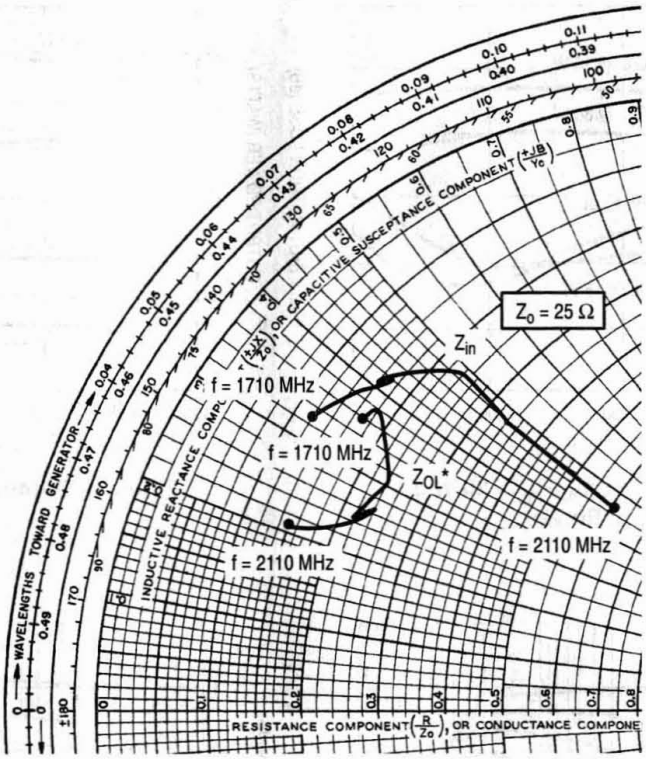


Figure 8. Power Gain and Efficiency versus Output Power



V_{DD} = 26 V, I_{DQ} = 250 mA, P_{out} = 30 W (CW)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1710	2.92 + j8.24	4.18 + j9.06
1785	3.84 + j9.75	4.59 + j9.46
1805	4.15 + j10.38	4.98 + j9.06
1840	4.04 + j10.22	6.10 + j7.63
1880	6.12 + j12.29	5.83 + j6.89
1960	6.20 + j12.29	5.55 + j6.33
1990	8.61 + j12.10	5.93 + j6.66
2110	15.19 + j11.85	3.82 + j5.33

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given power, voltage, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, and drain efficiency.

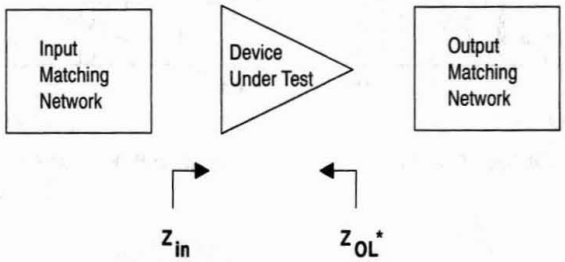


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

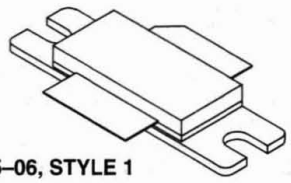
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18060A
MRF18060AR3
MRF18060AS
MRF18060ASR3

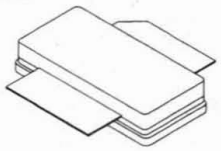
Designed for PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for PCN–PCS/cellular radio and WLL applications. Specified for GSM1805 – 1880 MHz.

- Typical GSM Performance, Full Frequency Band (1805 – 1880 MHz)
  Power Gain — 13 dB (Typ) @ 60 Watts
  Efficiency — 45% (Typ) @ 60 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

1.80 – 1.88 GHz, 60 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465–06, STYLE 1
(NI–780)
(MRF18060A)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF18060AS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ $T_C \geq 25°C$ Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

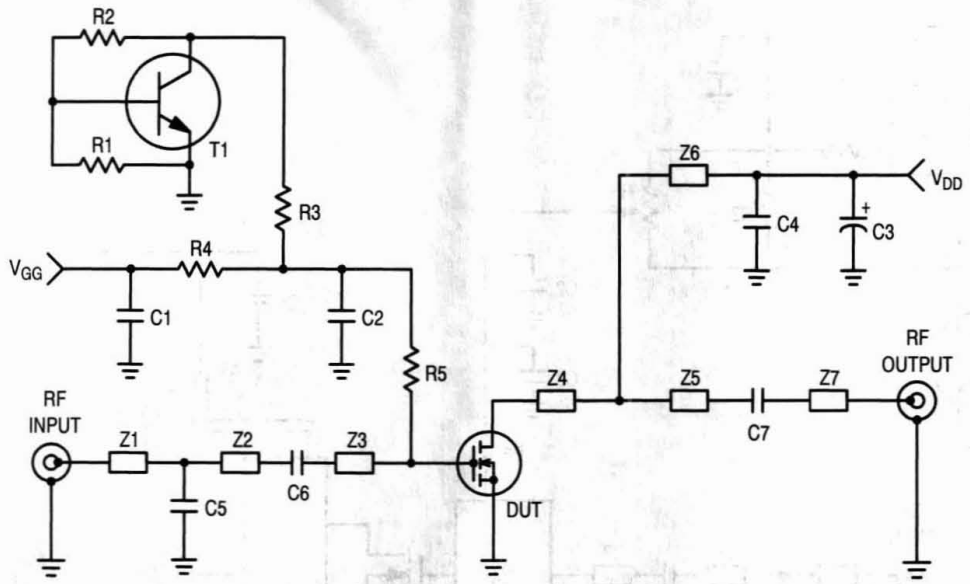
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	160	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	740	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	G_{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	η	43	45	—	%
Input Return Loss (2) (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1805 – 1880 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.
(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.



C1	100 nF Chip Capacitor (1203)	Z1	0.47″ x 0.09″ Microstrip
C2, C4, C7	10 pF Chip Capacitors	Z2	1.16″ x 0.09″ Microstrip
C3	10 μF, 35 V Electrolytic Tantalum Capacitor	Z3	0.57″ x 0.95″ Microstrip
C5	1.2 pF Chip Capacitor	Z4	0.59″ x 1.18″ Microstrip
C6	1.0 pF Chip Capacitor	Z5	1.26″ x 0.15″ Microstrip
R1, R3	2.2 kΩ Chip Resistors (0805)	Z6	1.15″ x 0.09″ Microstrip
R2, R4	2.7 kΩ Chip Resistors (0805)	Z7	0.37″ x 0.09″ Microstrip
R5	1.1 kΩ Chip Resistor (0805)		
T1	BC847 Transistor SOT–23		

Figure 1. 1805 – 1880 MHz Test Fixture Schematic

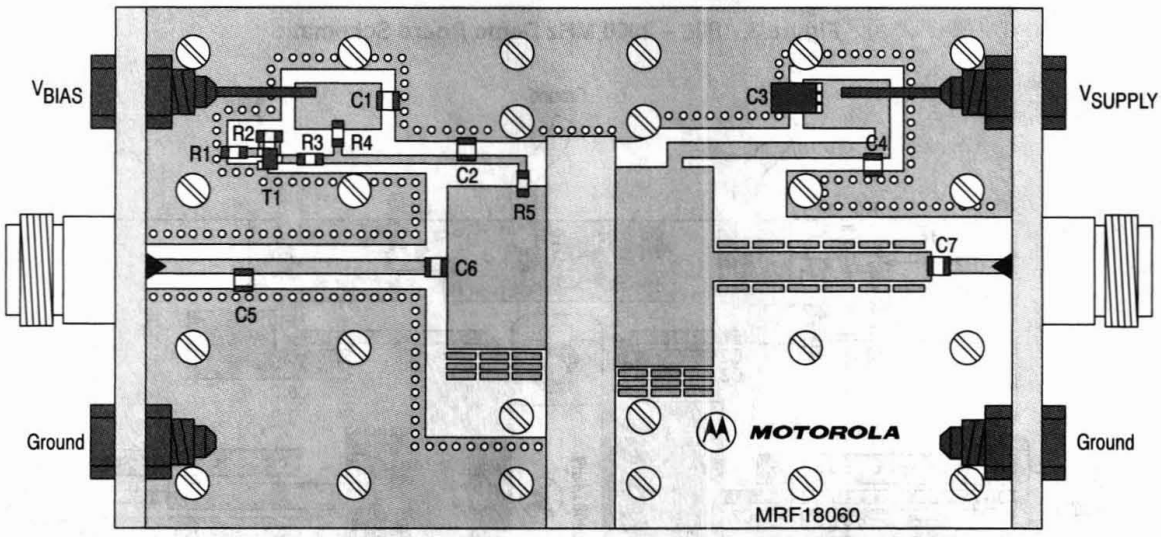
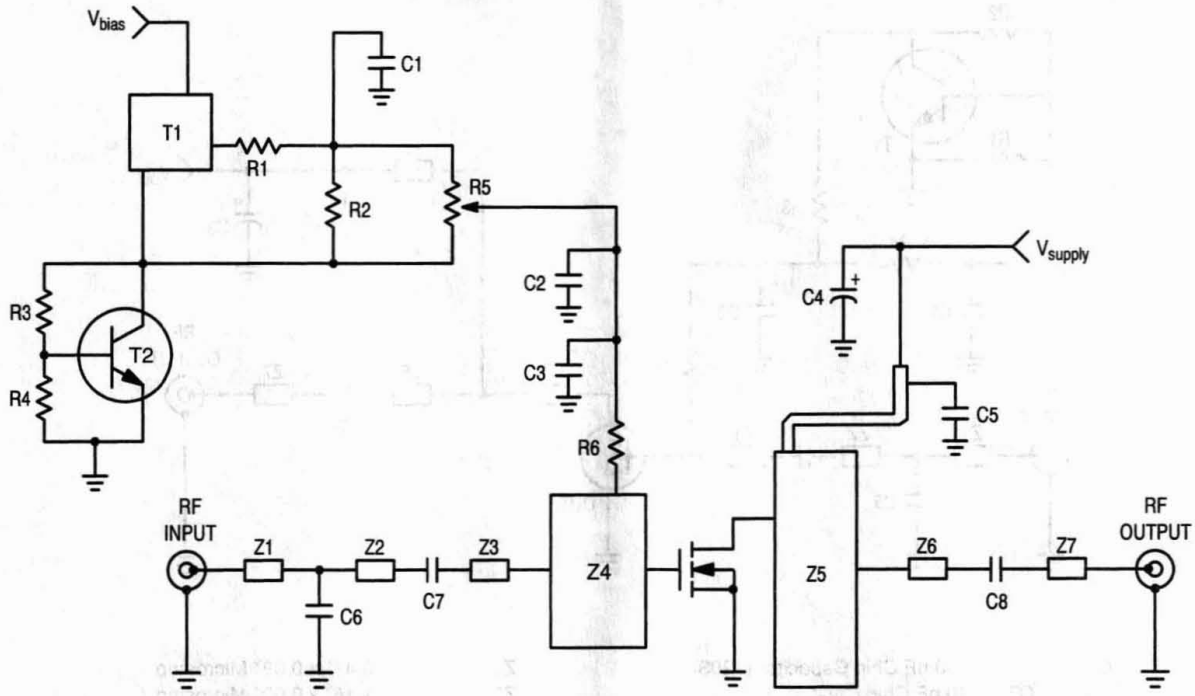


Figure 2. 1805 – 1880 MHz Test Fixture Component Layout



C1	1 μF Chip Capacitor (0805)	T1	LP2951 Micro–8 Voltage Regulator
C2	100 nF Chip Capacitor (0805)	T2	BC847 SOT–23 NPN Transistor
C3, C5, C8	10 pF Chip Capacitors, ACCU–P (0805)	Z1	0.159″ x 0.055″ Microstrip
C4	10 μF, 35 V Tantalum Electrolytic Capacitor	Z2	0.982″ x 0.055″ Microstrip
C6	1.8 pF Chip Capacitor, ACCU–P (0805)	Z3	0.087″ x 0.055″ Microstrip
C7	1 pF Chip Capacitor, ACCU–P (0805)	Z4	0.512″ x 0.787″ Microstrip
R1	10 Ω Chip Resistor (0805)	Z5	0.433″ x 1.220″ Microstrip
R2, R6	1 kΩ Chip Resistors (0805)	Z6	1.039″ x 0.118″ Microstrip
R3	1.2 kΩ Chip Resistor (0805)	Z7	0.268″ x 0.055″ Microstrip
R4	2.2 kΩ Chip Resistor (0805)	Substrate = 0.5 mm Teflon® Glass, ε_r = 2.55	
R5	5 kΩ, SMD Potentiometer		

Figure 3. 1800 – 2000 MHz Demo Board Schematic

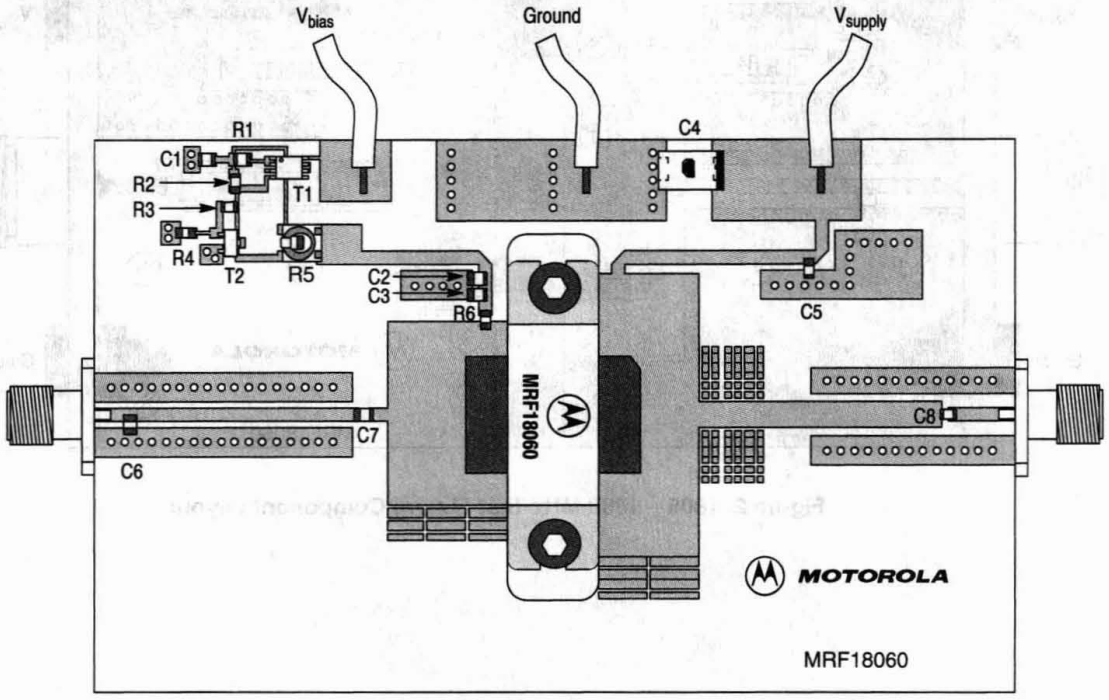


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

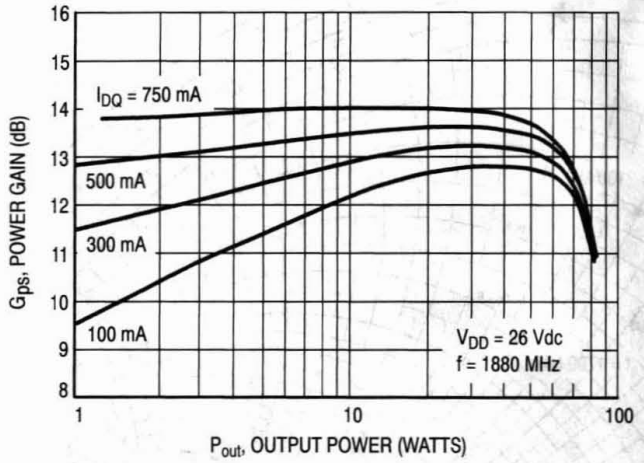


Figure 5. Power Gain versus Output Power

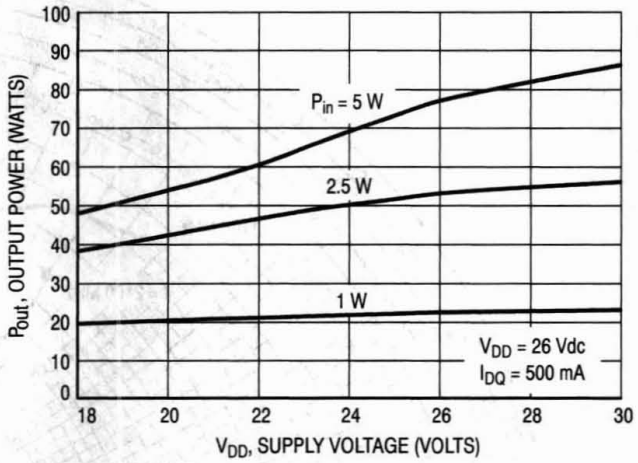


Figure 6. Output Power versus Supply Voltage

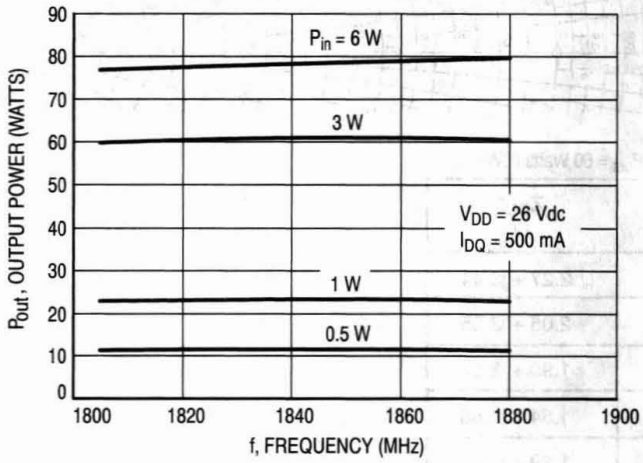


Figure 7. Output Power versus Frequency

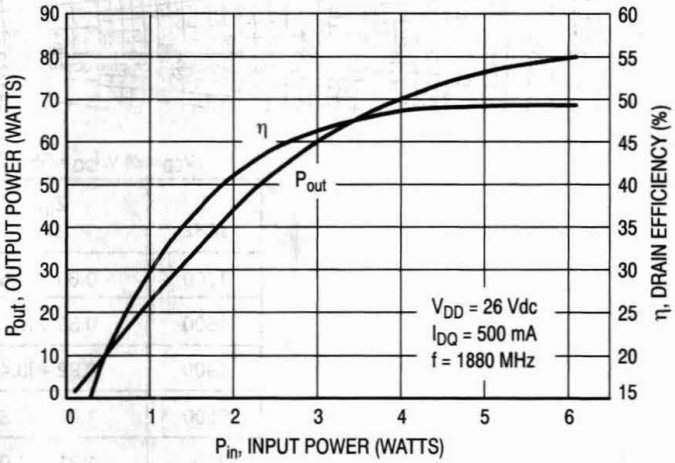


Figure 8. Output Power and Efficiency versus Input Power

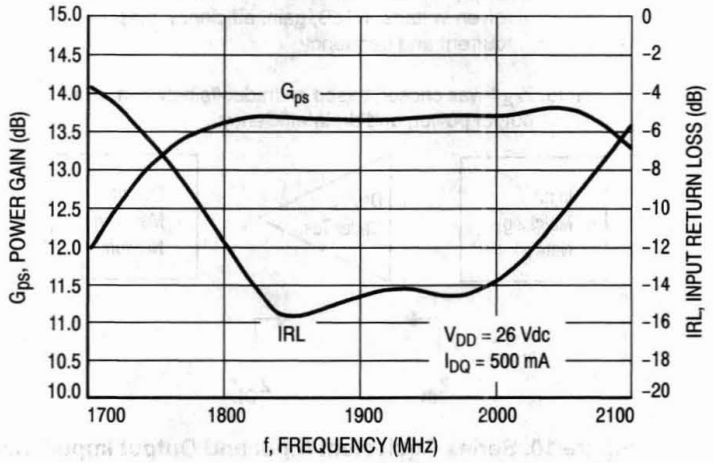
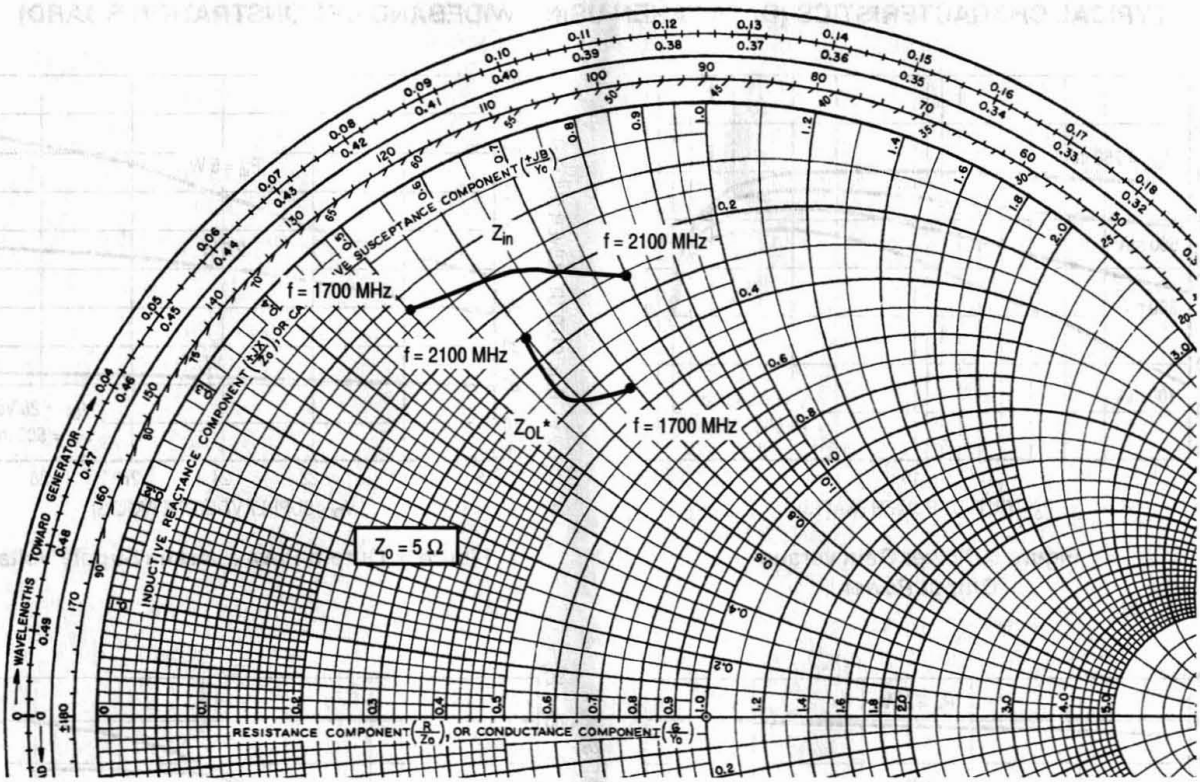


Figure 9. Wideband Gain and IRL (at Small Signal)



V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1700	0.60 + j2.53	2.27 + j3.44
1800	0.80 + j3.20	2.05 + j3.05
1900	0.92 + j3.42	1.90 + j2.90
2000	1.07 + j3.59	1.64 + j2.88
2100	1.31 + j4.00	1.29 + j2.99

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, and drain efficiency.

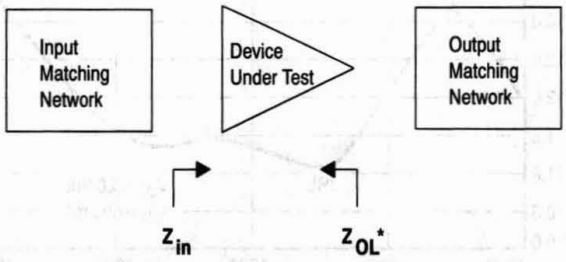


Figure 10. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

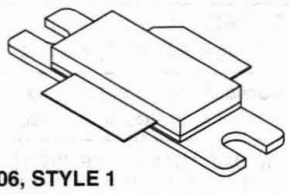
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18060B
MRF18060BR3
MRF18060BS
MRF18060BSR3

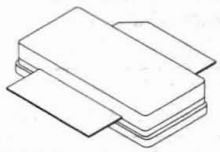
Designed for PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for PCN–PCS/cellular radio and WLL applications. Specified for GSM1930 – 1990 MHz.

- GSM Performance, Full Frequency Band (1930 – 1990 MHz)
  Power Gain — 13 dB (Typ) @ 60 Watts (CW)
  Efficiency — 45% (Typ) @ 60 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

1.90 – 1.99 GHz, 60 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465–06, STYLE 1
(NI–780)
(MRF18060B)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF18060BS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C > = 25°C Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

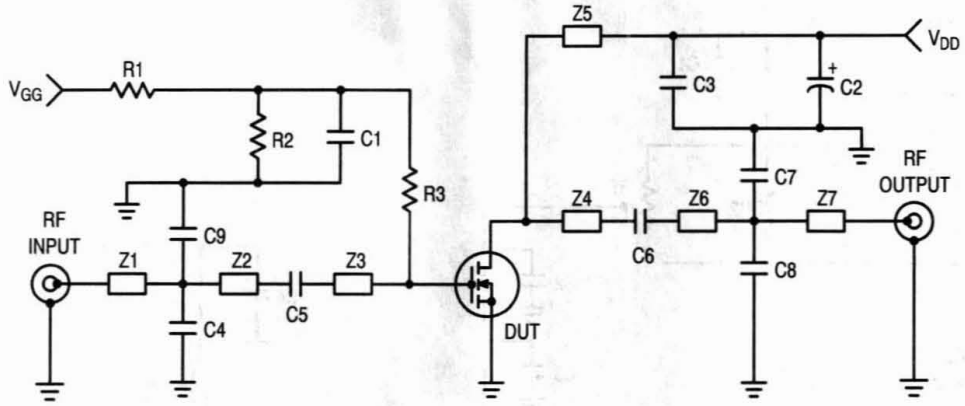
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	160	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	740	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	G_{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	η	40	45	—	%
Input Return Loss (2) (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1930 – 1990 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.
(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch–to–batch consistency.



C1, C3	10 pF, 100B Chip Capacitors	Z1	0.60″ x 0.09″ Microstrip
C2	10 μF, 35 V Electrolytic Tantalum Capacitor	Z2	1.00″ x 0.09″ Microstrip
C4, C8	1.2 pF, 100B Chip Capacitors	Z3	0.51″ x 0.94″ Microstrip
C5	1.0 pF, 100B Chip Capacitor	Z4	0.59″ x 0.98″ Microstrip
C6	2.2 pF, 100B Chip Capacitor	Z5	0.79″ x 0.09″ Microstrip
C7, C9	0.3 pF, 100B Chip Capacitors	Z6	1.38″ x 0.09″ Microstrip
R1, R2	10 kΩ Chip Resistors (0805)	Z7	0.79″ x 0.09″ Microstrip
R3	1.0 kΩ Chip Resistor (0805)	PCB	Teflon® Glass

Figure 1. 1930 – 1990 MHz Test Fixture Schematic

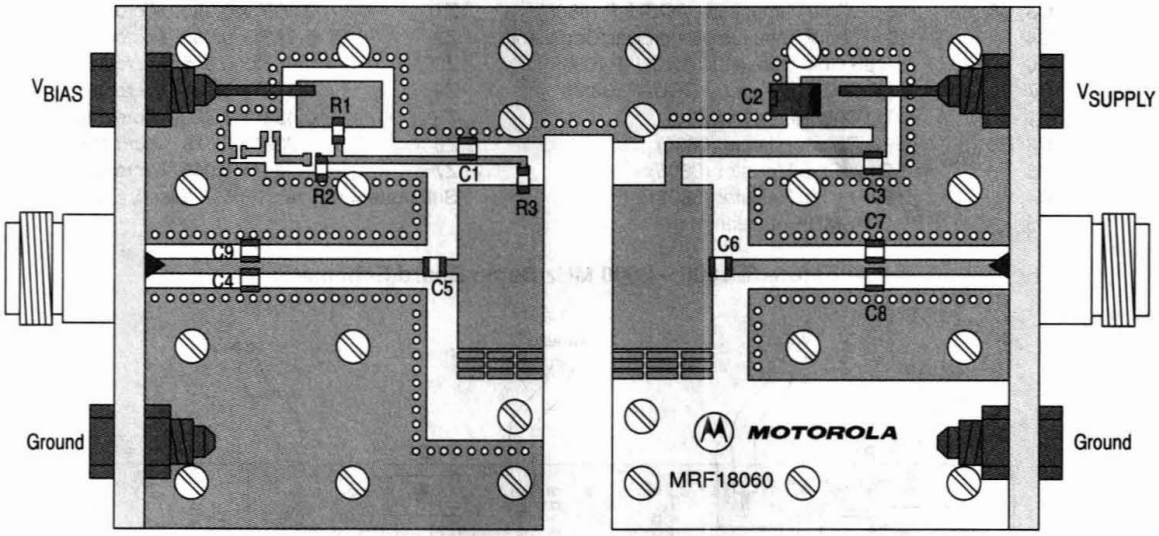
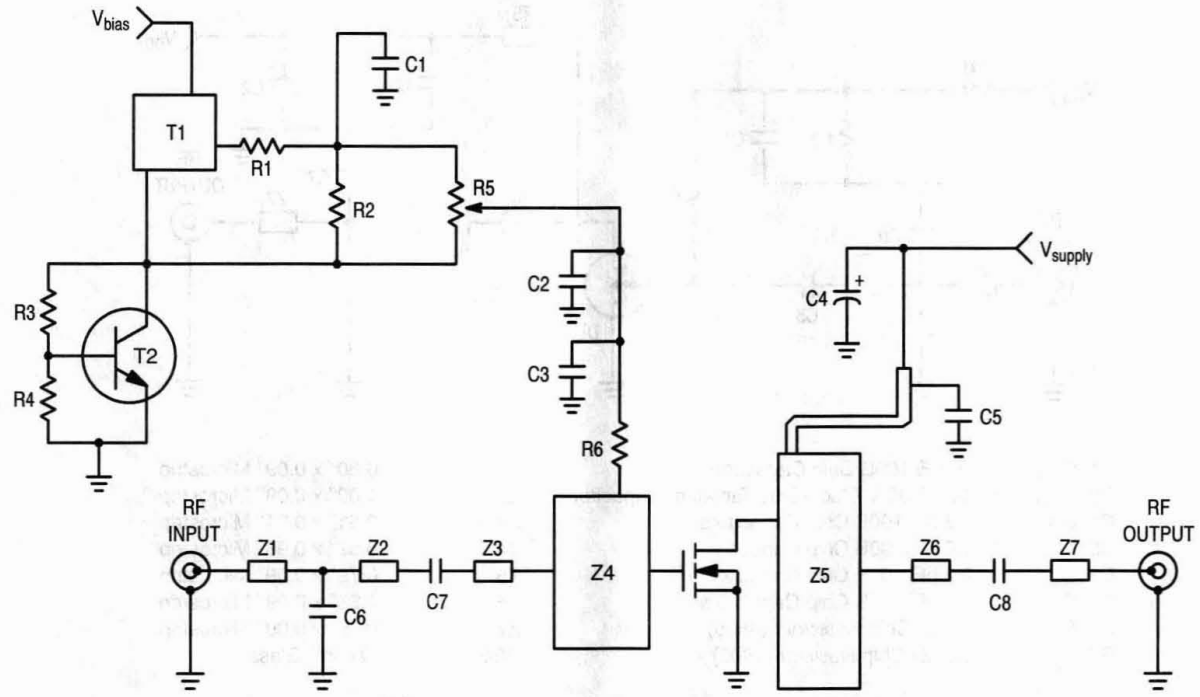


Figure 2. 1930 – 1990 MHz Test Fixture Component Layout



C1	1 μF Chip Capacitor (0805)	T1	LP2951 Micro–8 Voltage Regulator
C2	100 nF Chip Capacitor (0805)	T2	BC847 SOT–23 NPN Transistor
C3, C5, C8	10 pF Chip Capacitors, ACCU–P (0805)	Z1	0.159″ x 0.055″ Microstrip
C4	10 μF, 35 V Tantalum Electrolytic Capacitor	Z2	0.982″ x 0.055″ Microstrip
C6	1.8 pF Chip Capacitor, ACCU–P (0805)	Z3	0.087″ x 0.055″ Microstrip
C7	1 pF Chip Capacitor, ACCU–P (0805)	Z4	0.512″ x 0.787″ Microstrip
R1	10 Ω Chip Resistor (0805)	Z5	0.433″ x 1.220″ Microstrip
R2, R6	1 kΩ Chip Resistors (0805)	Z6	1.039″ x 0.118″ Microstrip
R3	1.2 kΩ Chip Resistor (0805)	Z7	0.268″ x 0.055″ Microstrip
R4	2.2 kΩ Chip Resistor (0805)	Substrate = 0.5 mm Teflon® Glass, ε_r = 2.55	
R5	5 kΩ, SMD Potentiometer		

Figure 3. 1800 – 2000 MHz Demo Board Schematic

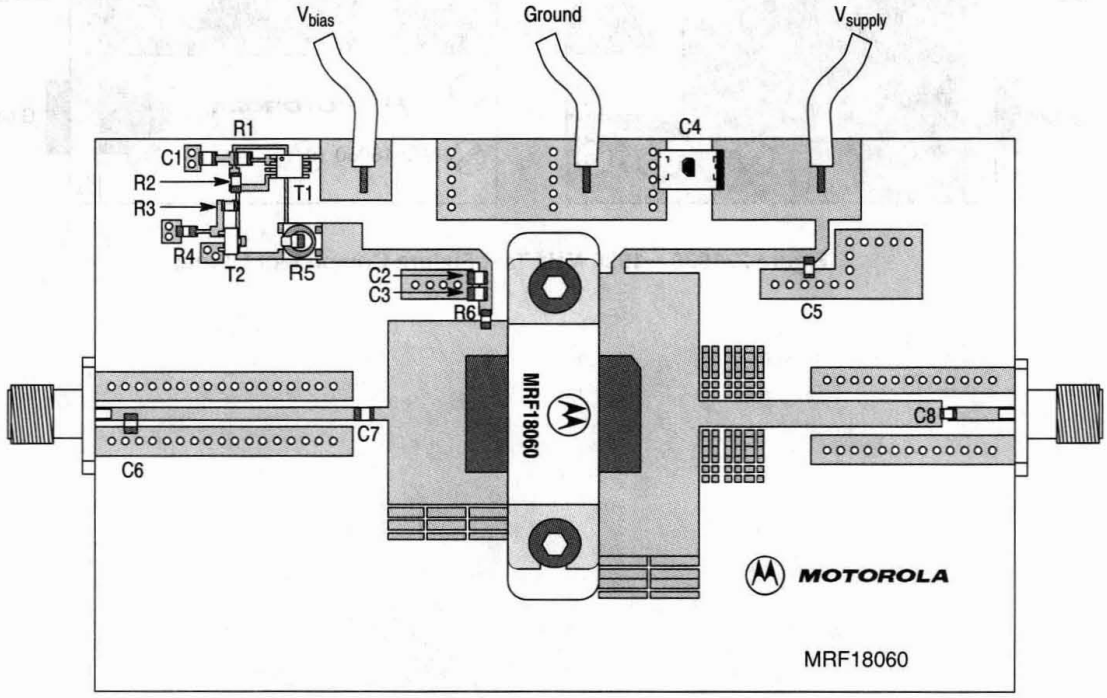


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

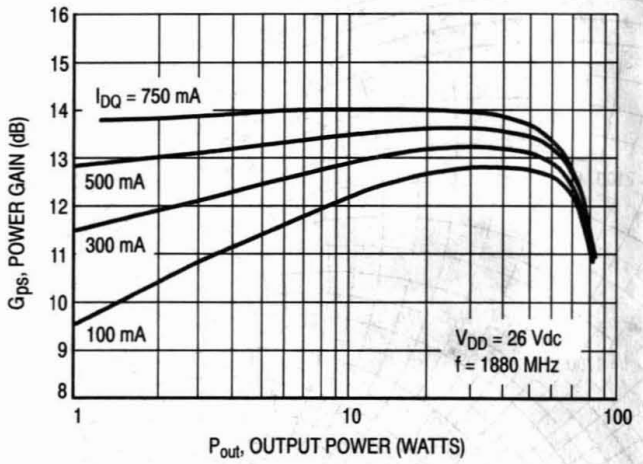


Figure 5. Power Gain versus Output Power

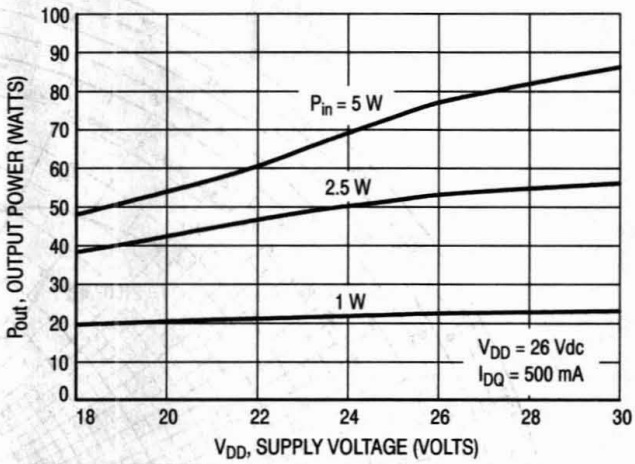


Figure 6. Output Power versus Supply Voltage

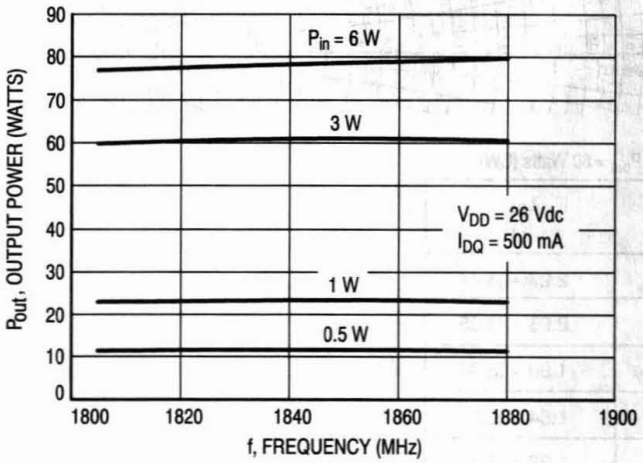


Figure 7. Output Power versus Frequency

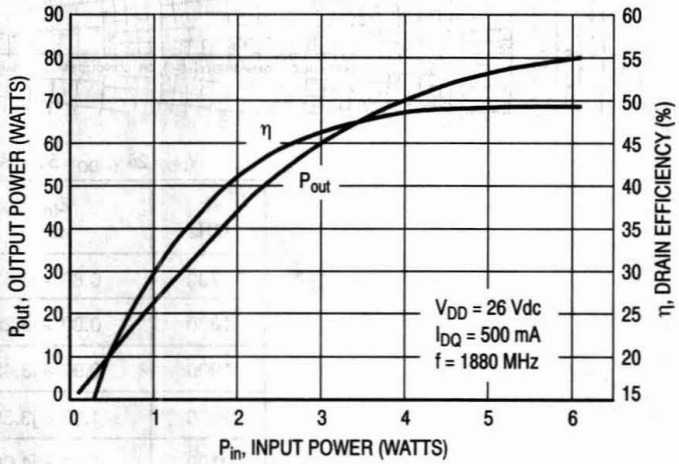


Figure 8. Output Power and Efficiency versus Input Power

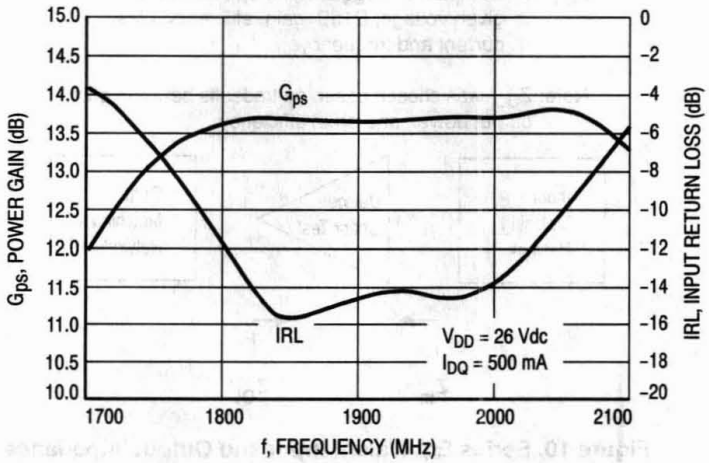
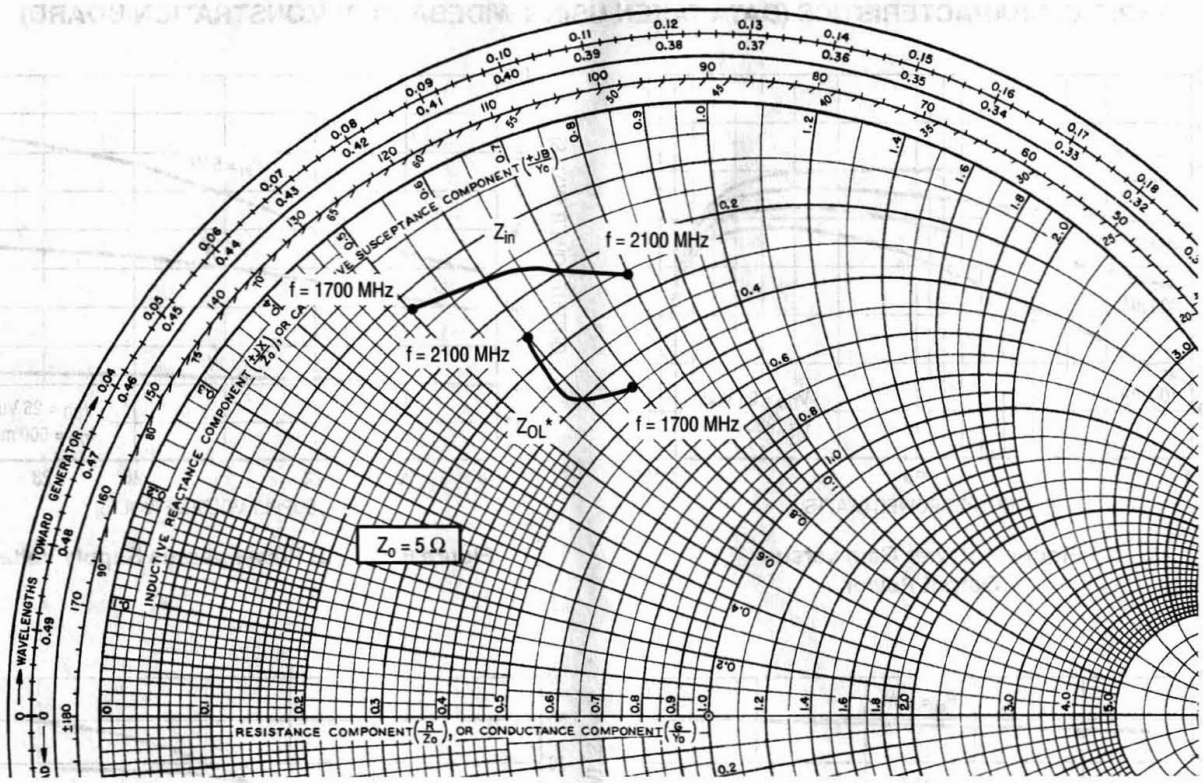


Figure 9. Wideband Gain and IRL (at Small Signal)



V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1700	0.60 + j2.53	2.27 + j3.44
1800	0.80 + j3.20	2.05 + j3.05
1900	0.92 + j3.42	1.90 + j2.90
2000	1.07 + j3.59	1.64 + j2.88
2100	1.31 + j4.00	1.29 + j2.99

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}^* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, and drain efficiency.

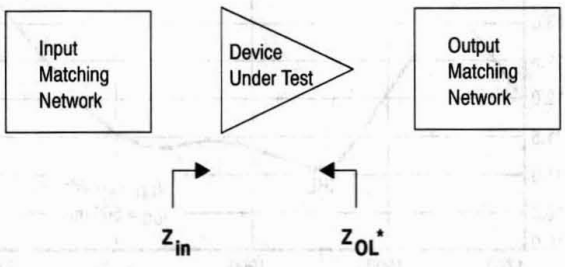


Figure 10. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

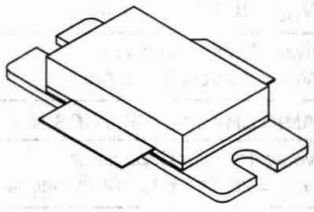
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18090A
MRF18090AS

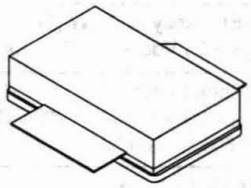
1.80 – 1.88 GHz, 90 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETS

Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for GSM and EDGE cellular radio applications.

- GSM and EDGE Performances, Full Frequency Band
  Power Gain — 13.5 dB (Typ) @ 90 Watts (CW)
  Efficiency — 52% (Typ) @ 90 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465B–03, STYLE 1
(NI–880)
(MRF18090A)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF18090AS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

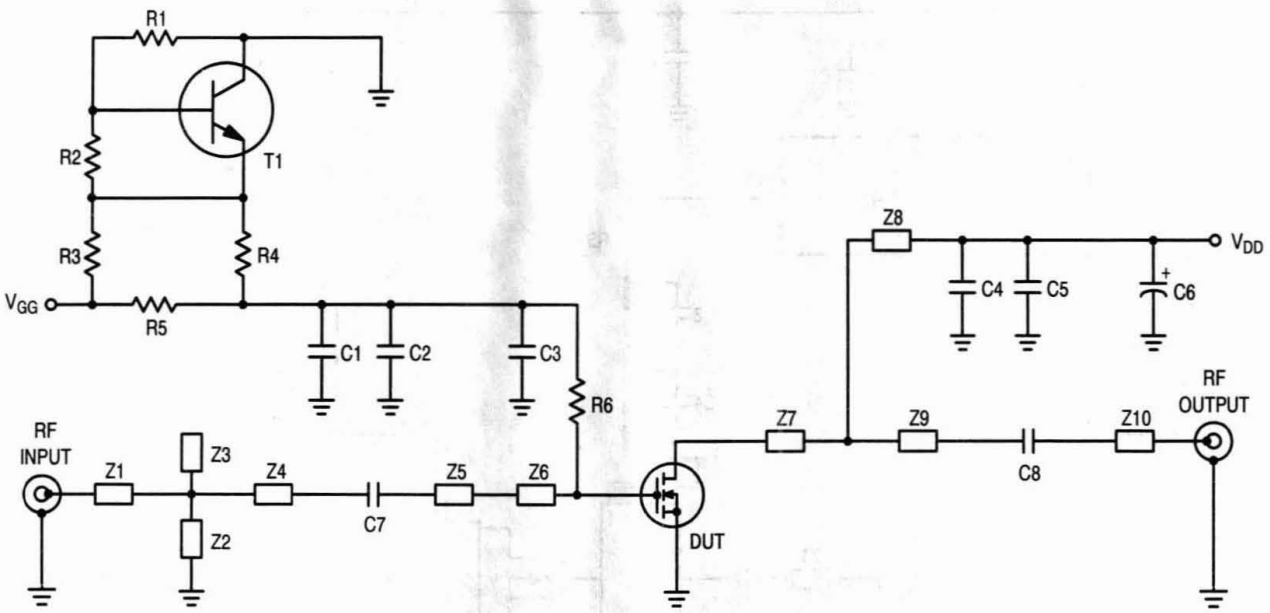
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.1	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1805 – 1880 MHz)	G_{ps}	12.0	13.5	—	dB
Drain Efficiency @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1805 – 1880 MHz)	η	47	52	—	%
Input Return Loss (1) (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 1805 – 1880 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.



C1, C3	1.0 μF Chip Capacitors (0805)	Z2	0.197″ x 0.087″ Microstrip
C2	1.0 nF Chip Capacitor (0805)	Z3	0.819″ x 0.087″ Microstrip
C4, C5	6.8 pF, 100B Chip Capacitors, ATC	Z4	0.181″ x 0.144″ Microstrip
C6	220 μF, 50 V Electrolytic Capacitor	Z5	0.383″ x 1.148″ Microstrip
C7, C8	12 pF, 100B Chip Capacitors, ATC	Z6	0.400″ x 1.380″ Microstrip
R1	2.2 kΩ Chip Resistor (0805)	Z7	0.351″ x 0.351″ Microstrip
R2, R3, R6	1.0 kΩ Chip Resistors (0805)	Z8	0.126″ x 0.087″ Microstrip
R4	10 kΩ Chip Resistor (0805)	Z9	1.280″ x 0.087″ Microstrip
R5	6.8 kΩ Chip Resistor (0805)	Z10	≈1.275″ x 0.055″ Microstrip
T1	BC847 SOT–23	PCB	Teflon® Glass
Z1	0.697″ x 0.087″ Microstrip		

Figure 1. 1.80 – 1.88 GHz Test Fixture Schematic

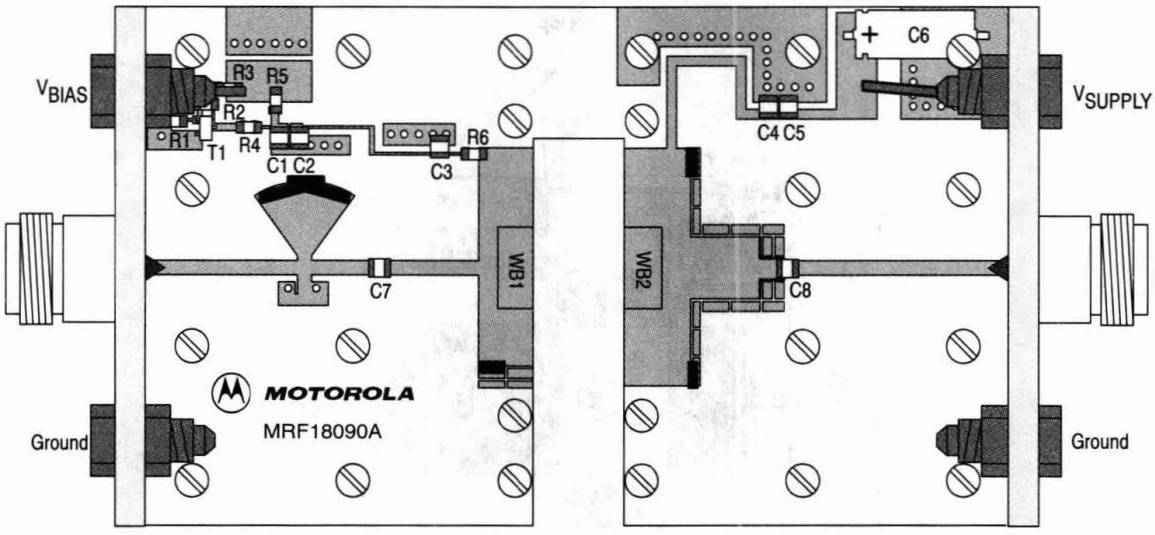
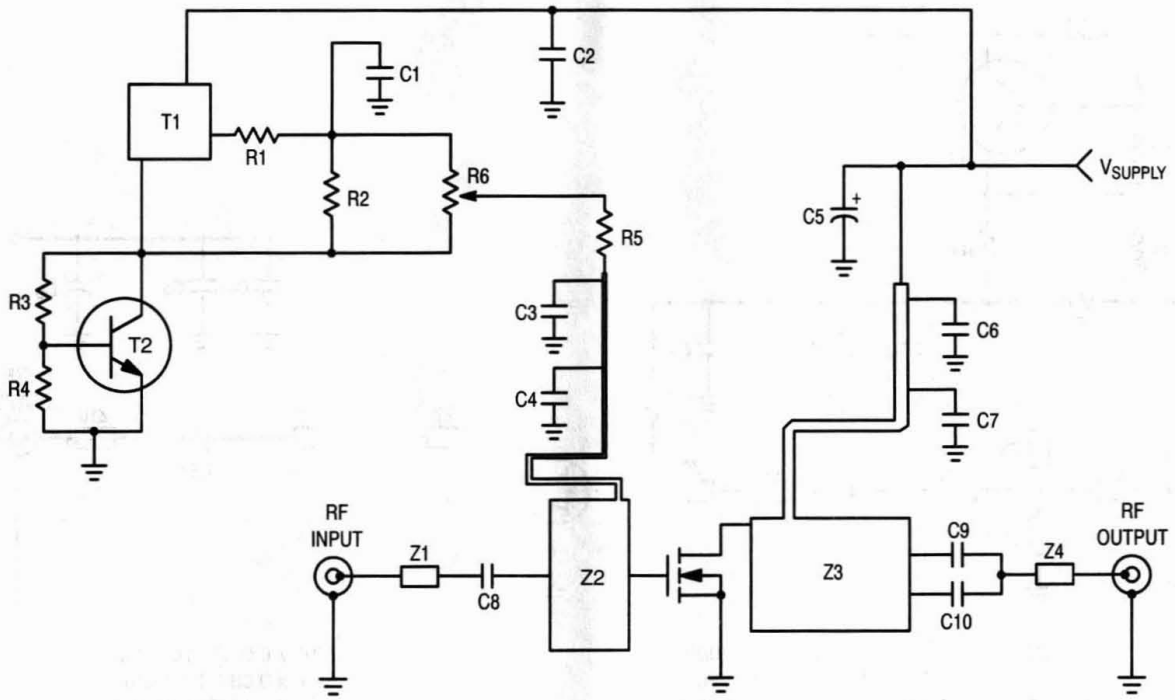


Figure 2. 1.80 – 1.88 GHz Test Fixture Component Layout



C1, C3	1 μF Chip Capacitors (0805)	R5	10 kΩ Chip Resistor (0603)
C2	0.1 μF Chip Capacitor (0805)	R6	5 kΩ, SMD Potentiometer
C4	1 nF Chip Capacitor (0805)	T1	LP2951 Micro–8 Voltage Regulator
C5	220 μF, 50 V Electrolytic Capacitor	T2	BC847 SOT–23 NPN Transistor
C6, C7	8.2 pF, 100A Chip Capacitors	Z1	0.210″ x 0.055″ Microstrip
C8, C9, C10	22 pF, 100A Chip Capacitors	Z2	0.419″ x 0.787″ Microstrip
R1	10 Ω Chip Resistor (0805)	Z3	0.836″ x 0.512″ Microstrip
R2, R3	1 kΩ Chip Resistors (0805)	Z4	0.164″ x 0.055″ Microstrip
R4	2.2 kΩ Chip Resistor (0805)	Substrate = 0.5 mm Teflon® Glass	

Figure 3. 1.80 – 1.88 GHz Demo Board Schematic

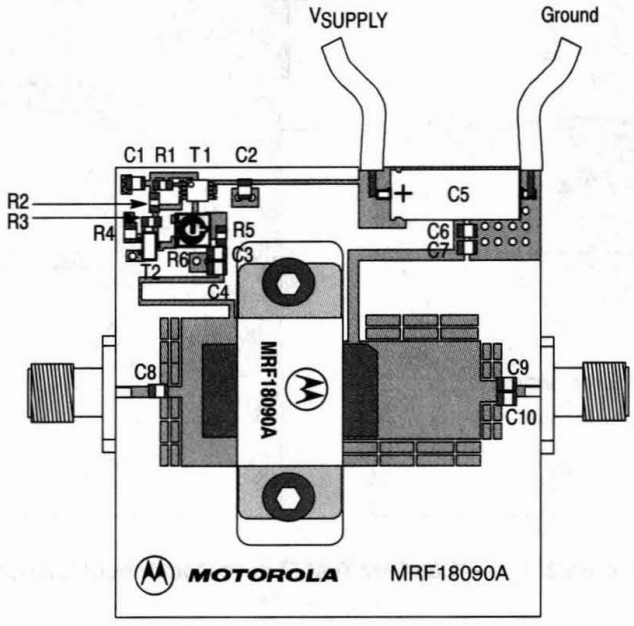


Figure 4. 1.80 – 1.88 GHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

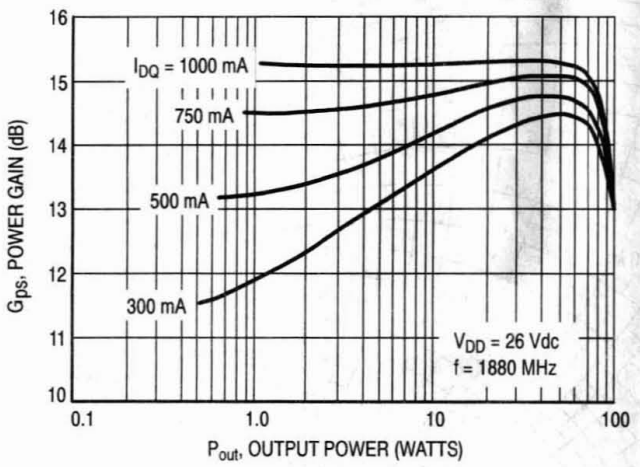


Figure 5. Power Gain versus Output Power

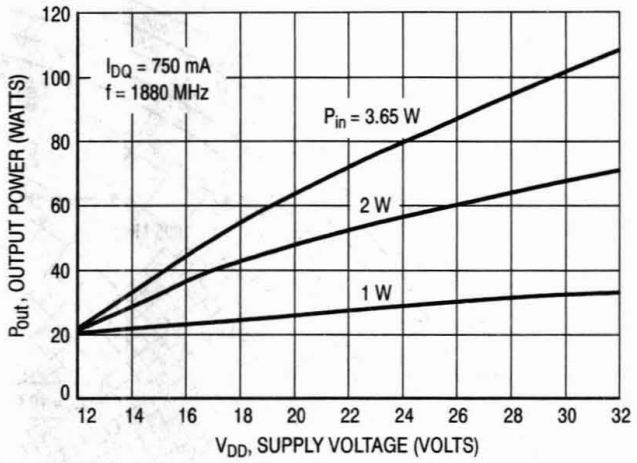


Figure 6. Output Power versus Supply Voltage

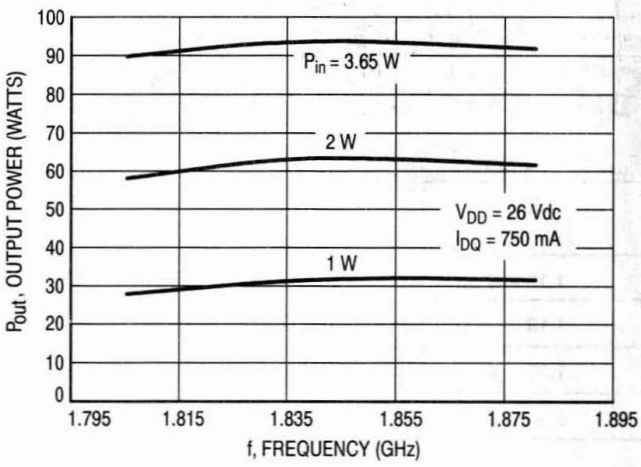


Figure 7. Output Power versus Frequency

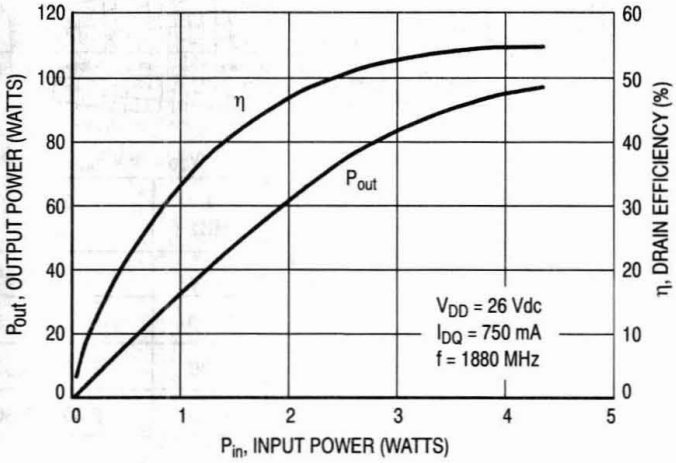


Figure 8. Output Power and Efficiency versus Input Power

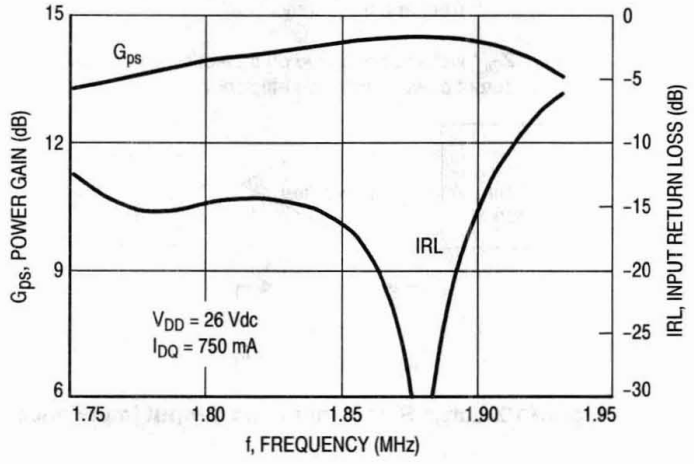
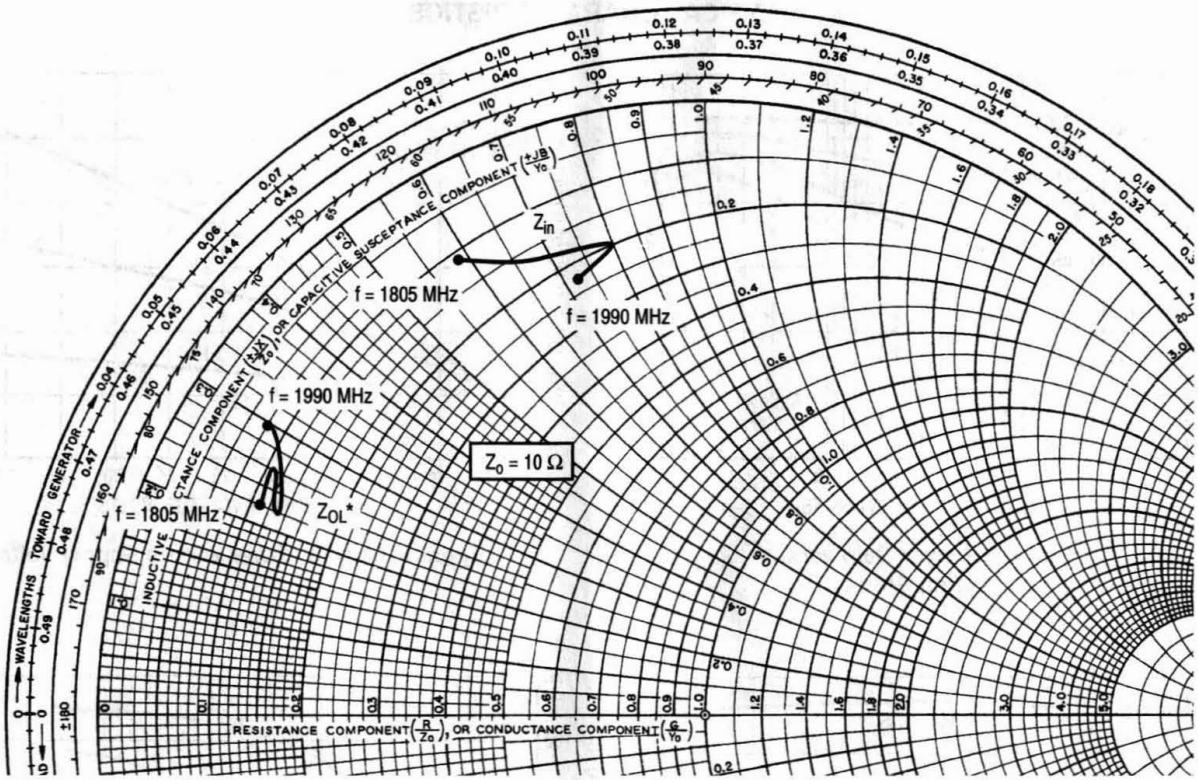


Figure 9. Wideband Gain and IRL (at Small Signal)



V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1805	1.10 + j5.85	1.15 + j2.16
1880	1.56 + j6.75	1.13 + j2.60
1930	2.05 + j8.00	1.30 + j2.23
1990	2.30 + j7.30	0.82 + j2.90

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, and drain efficiency.

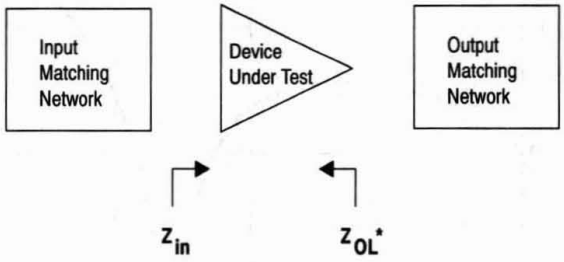


Figure 10. Large Signal Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

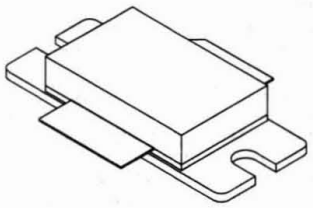
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18090B
MRF18090BS

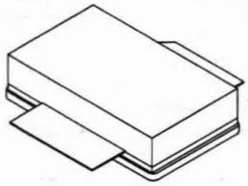
1.90 – 1.99 GHz, 90 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETS

Designed for GSM and EDGE base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for GSM and EDGE cellular radio applications.

- GSM and EDGE Performances, Full Frequency Band
  Power Gain — 13.5 dB (Typ) @ 90 Watts (CW)
  Efficiency — 45% (Typ) @ 90 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 465B–03, STYLE 1
(NI–880)
(MRF18090B)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF18090BS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

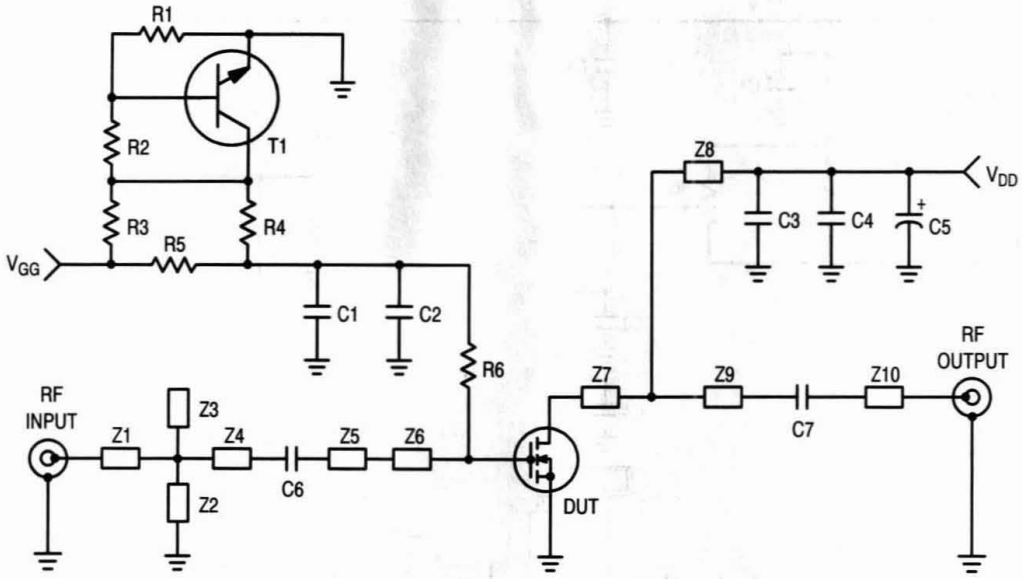
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.1	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	G_{ps}	12	13.5	—	dB
Drain Efficiency @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	η	40	45	—	%
Input Return Loss (1) (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch–to–batch consistency.



C1	1.0 μF Chip Capacitor (0805)	Z2	Printed Inductance
C2	1.0 nF Chip Capacitor (0805)	Z3	Printed Inductance (Butterfly)
C3, C4	6.8 pF, 100B Chip Capacitors	Z4	0.70″ x 0.09″ Microstrip
C5	220 μF, 50 V Electrolytic Capacitor	Z5	0.36″ x 0.09″ Microstrip
C6, C7	12 pF, 100B Chip Capacitors	Z6	0.21″ x 1.25″ Microstrip
R1	2.2 kΩ Chip Resistor (0805)	Z7	0.45″ x 1.18″ Microstrip
R2, R3, R6	1.0 kΩ Chip Resistors (0805)	Z8	1.37″ x 0.05″ Microstrip
R4	10 kΩ Chip Resistor (0805)	Z9	0.39″ x 0.09″ Microstrip
R5	6.8 kΩ Chip Resistor (0805)	Z10	1.25″ x 0.09″ Microstrip
T1	BC847 SOT–23	PCB	Teflon® Glass
Z1	0.85″ x 0.09″ Microstrip		

Figure 1. 1.93 – 1.99 MHz Test Fixture Schematic

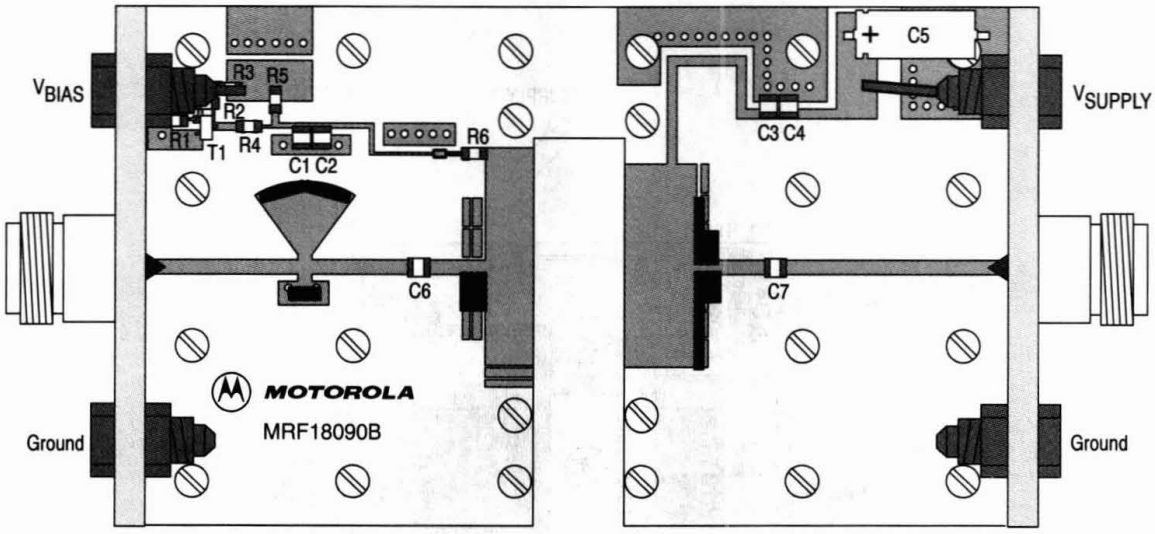
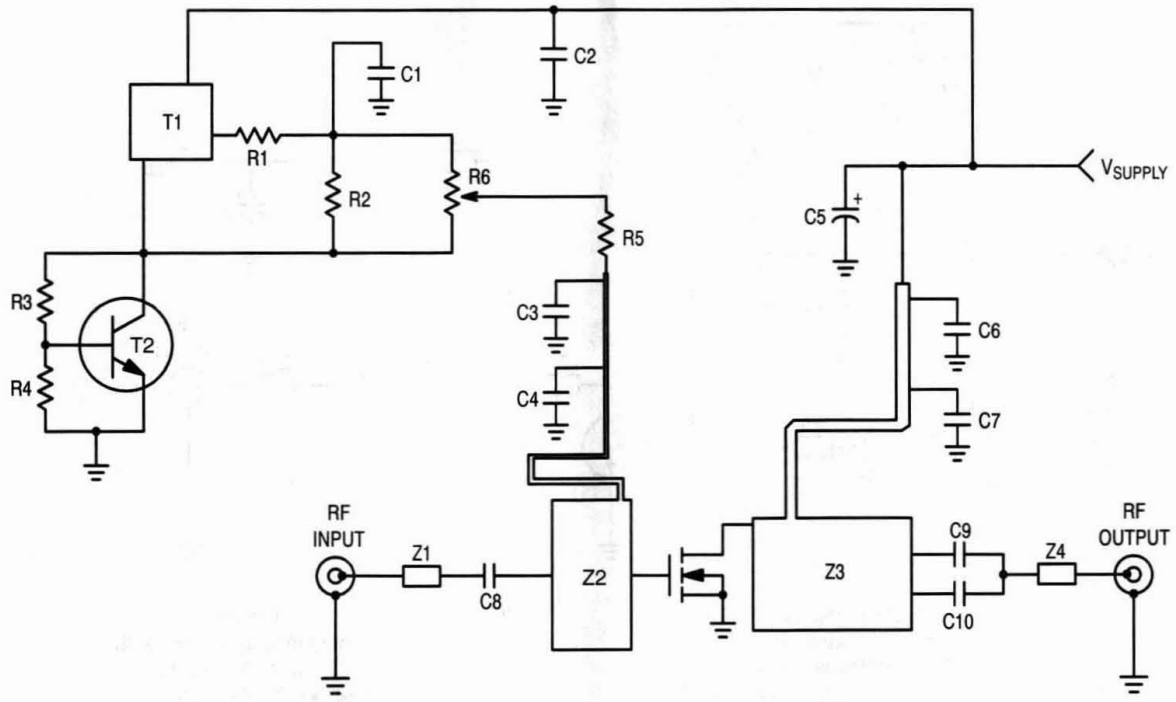


Figure 2. 1.93 – 1.99 GHz Test Fixture Component Layout



C1, C3	1 μF Chip Capacitors (0805)	R5	10 kΩ Chip Resistor (0603)
C2	0.1 μF Chip Capacitor (0805)	R6	5 kΩ, SMD Potentiometer
C4	1 nF Chip Capacitor (0805)	T1	LP2951 Micro–8 Voltage Regulator
C5	220 μF, 50 V Electrolytic Capacitor	T2	BC847 SOT–23 NPN Transistor
C6, C7	8.2 pF, 100A Chip Capacitors	Z1	0.491″ x 0.110″ Microstrip
C8, C9, C10	22 pF, 100A Chip Capacitors	Z2	0.756″ x 1.260″ Microstrip
R1	10 Ω Chip Resistor (0805)	Z3	1.433″ x 1.260″ Microstrip
R2, R3	1 kΩ Chip Resistors (0805)	Z4	0.567″ x 0.110″ Microstrip
R4	2.2 kΩ Chip Resistor (0805)	Substrate = 0.5 mm Teflon® Glass	

Figure 3. 1.93 – 1.99 GHz Demo Board Schematic

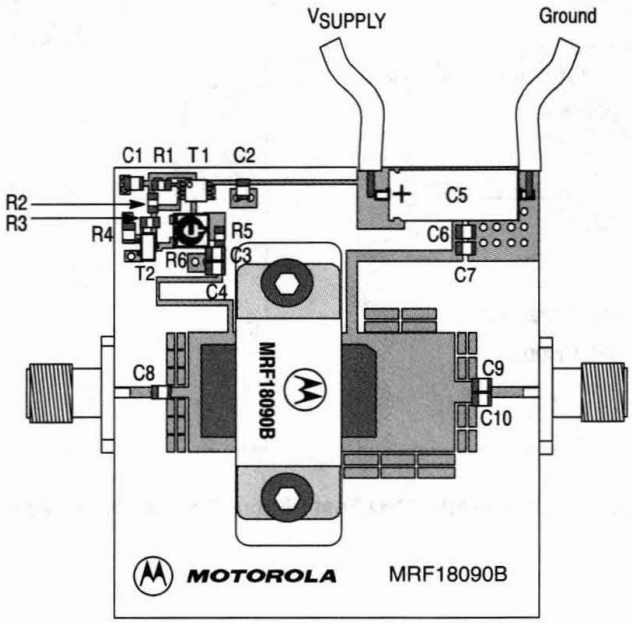


Figure 4. 1.93 – 1.99 GHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

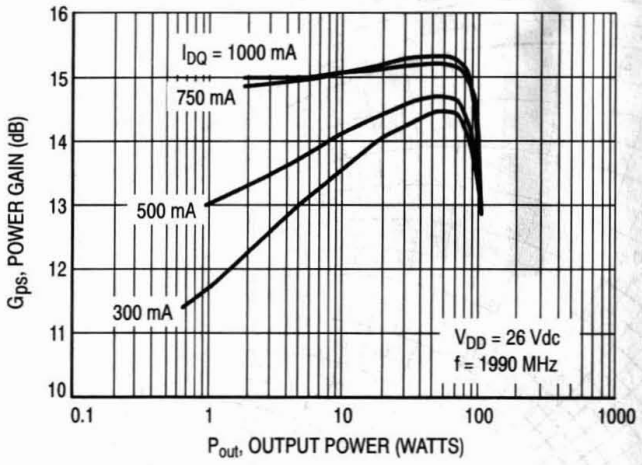


Figure 5. Power Gain versus Output Power

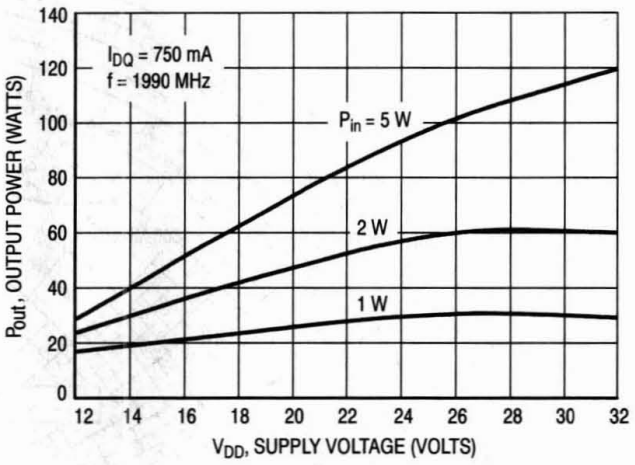


Figure 6. Output Power versus Supply Voltage

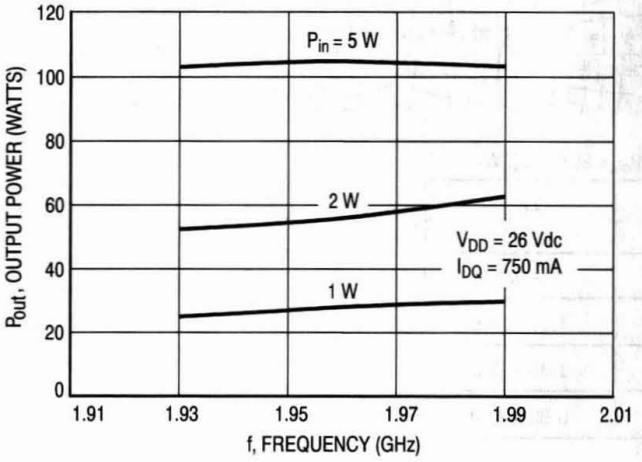


Figure 7. Output Power versus Frequency

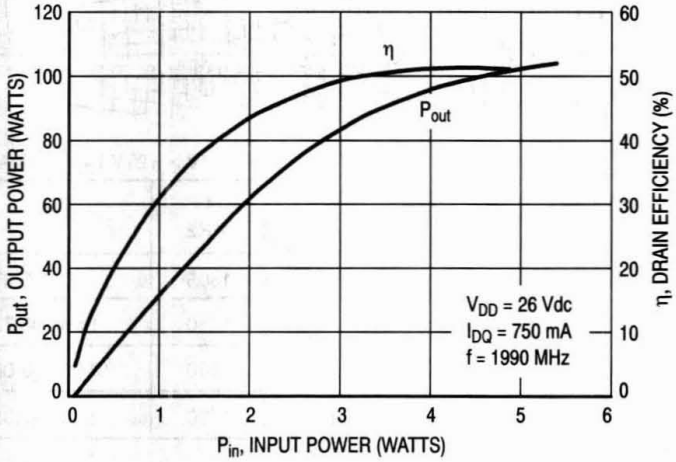


Figure 8. Output Power and Efficiency versus Input Power

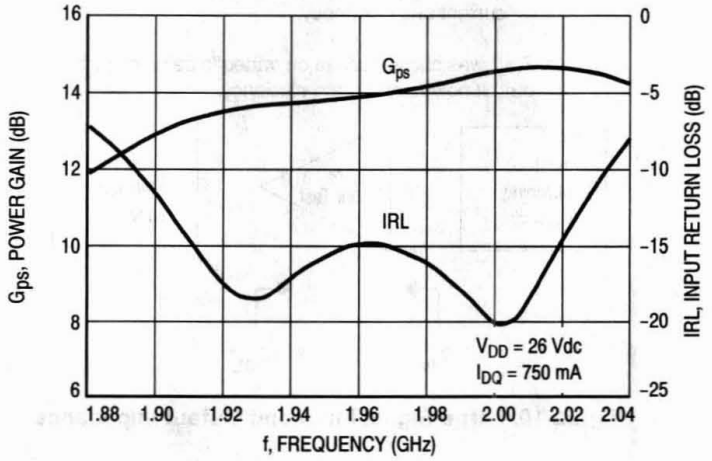
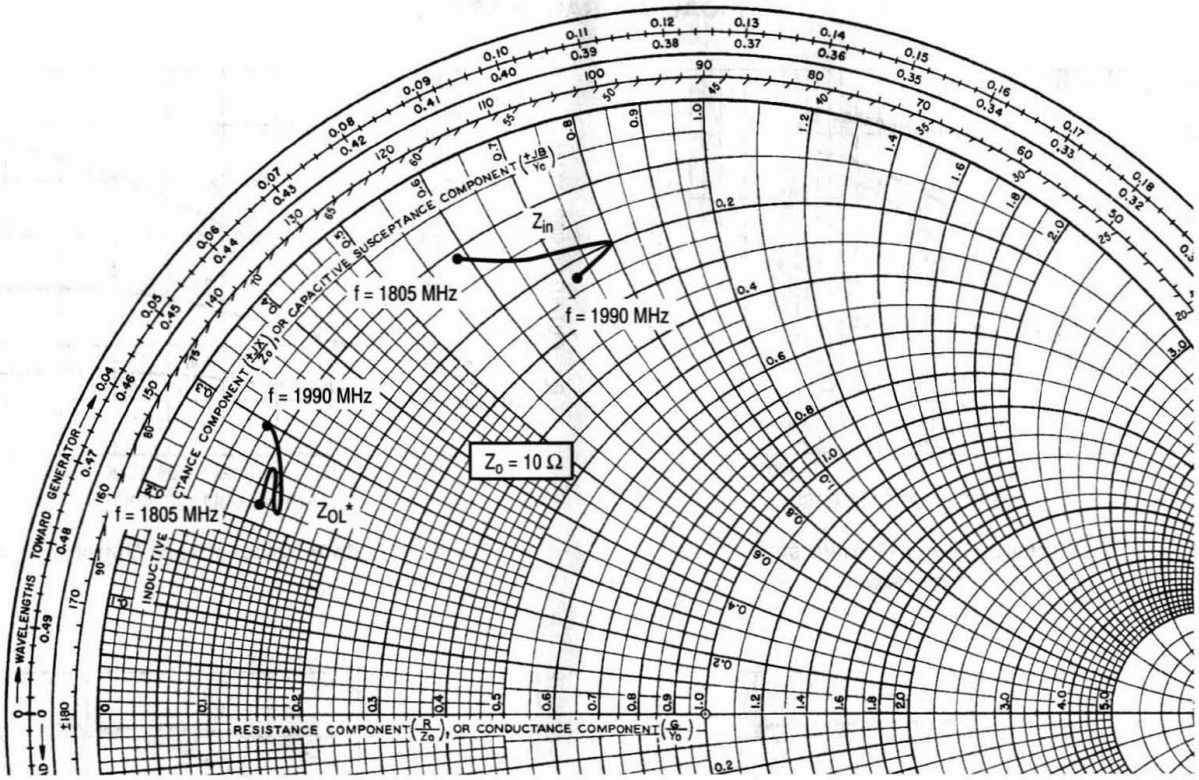


Figure 9. Wideband Gain and IRL (at Small Signal)



V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1805	1.10 + j5.85	1.15 + j2.16
1880	1.56 + j6.75	1.13 + j2.60
1930	2.05 + j8.00	1.30 + j2.23
1990	2.30 + j7.30	0.82 + j2.90

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, and drain efficiency.

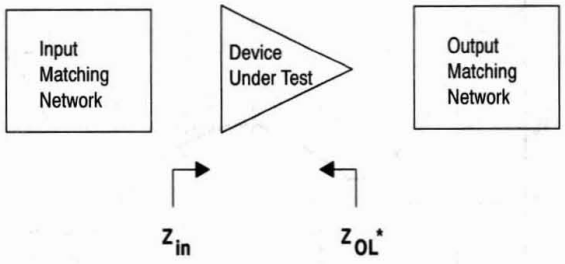


Figure 10. Large Signal Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

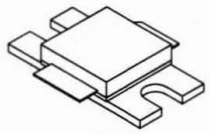
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19030
MRF19030R3
MRF19030S
MRF19030SR3

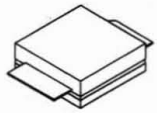
2.0 GHz, 30 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for class AB PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

- CDMA Performance @ 1990 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
  885 kHz — –47 dBc @ 30 kHz BW
  1.25 MHz — –55 dBc @ 12.5 kHz BW
  2.25 MHz — –55 dBc @ 1 MHz BW
  Output Power — 4.5 Watts (Avg.)
  Power Gain — 13.5 dB
  Efficiency — 17%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.



CASE 465E–03, STYLE 1
(NI–400)
(MRF19030)



CASE 465F–03, STYLE 1
(NI–400S)
(MRF19030S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83.3 0.48	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

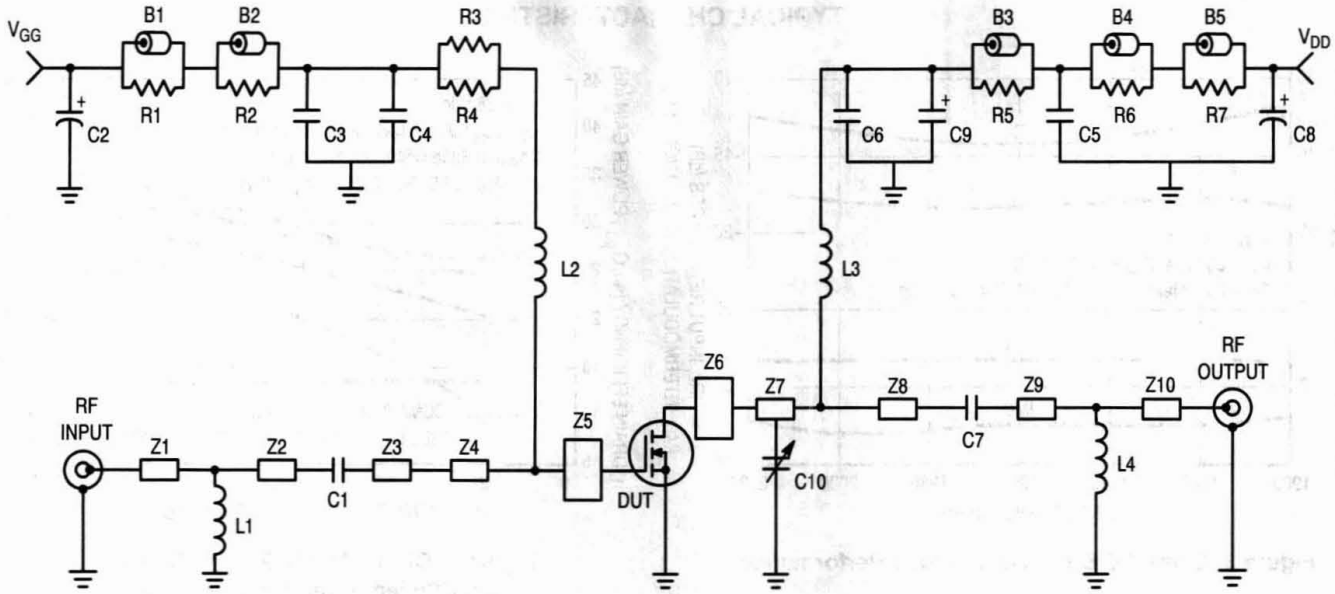
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 300 mA)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	98.5	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	η	—	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	IRL	—	–13	—	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz and f1 = 1990.0 MHz, f2 = 1990.1 MHz)	G_{ps}	12	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz and f1 = 1990.0 MHz, f2 = 1990.1 MHz)	η	33	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz and f1 = 1990.0 MHz, f2 = 1990.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz and f1 = 1990.0 MHz, f2 = 1990.1 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 300 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1 – B5	Short Ferrite Beads	Z3	0.080″ x 0.480″ Microstrip
C1, C7	10 pF Chip Capacitors, B Case	Z4	0.325″ x 0.280″ Microstrip
C2, C8	470 µF, 35 V Electrolytic Capacitors	Z5	0.510″ x 0.200″ Microstrip
C3, C5	0.1 µF Chip Capacitors, B Case	Z6	0.510″ x 0.200″ Microstrip
C4, C6	5.1 pF Chip Capacitors, B Case	Z7	0.325″ x 0.280″ Microstrip
C9	22 µF Tantalum Chip Capacitor	Z8	0.080″ x 0.480″ Microstrip
C10	0.4 – 2.5 pF Variable Capacitor, Johanson Gigatrim	Z9	0.080″ x 0.530″ Microstrip
L1 – L4	12.5 nH Inductors	Z10	0.080″ x 0.671″ Microstrip
R1 – R7	12 Ω Chip Resistors (0805)	Substrate	0.030″ x 3.00″ x 5.00″ Glass Teflon®, Arlon
Z1	0.080″ x 0.595″ Microstrip		
Z2	0.080″ x 0.600″ Microstrip		

Figure 1. MRF19030 Test Circuit Schematic

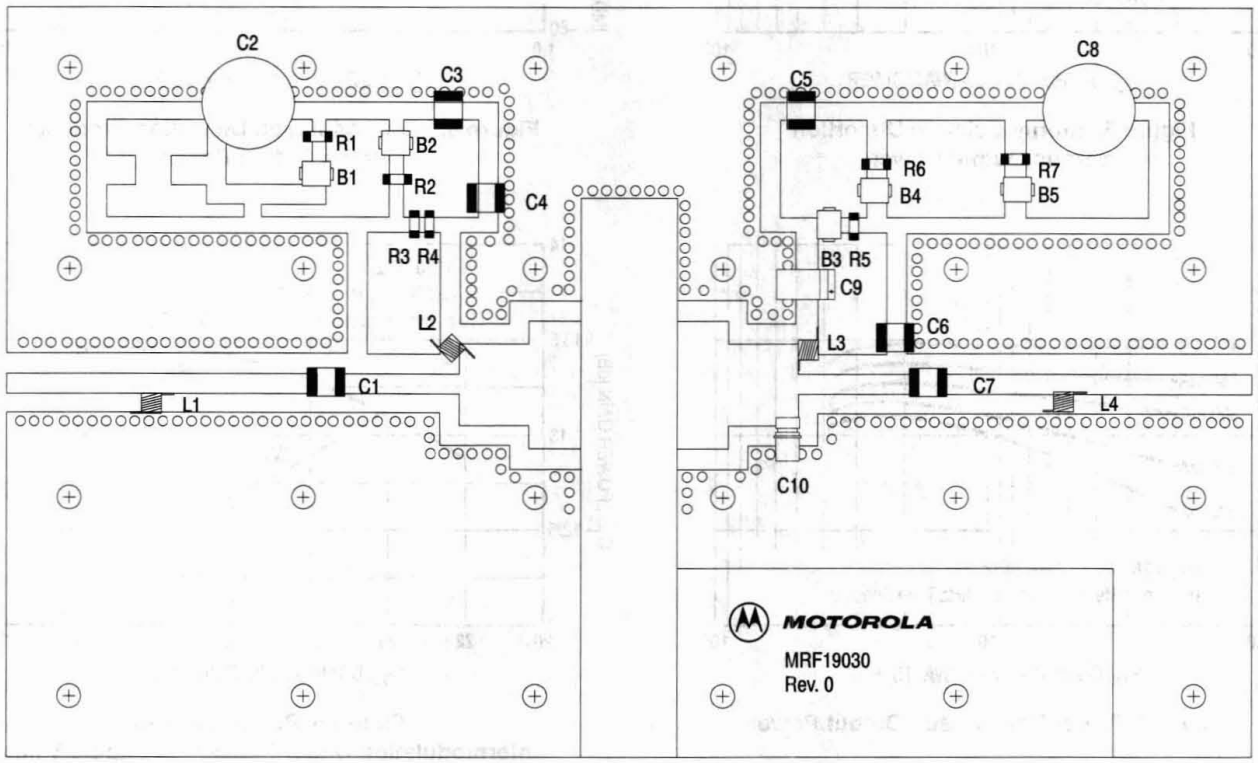


Figure 2. MRF19030 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

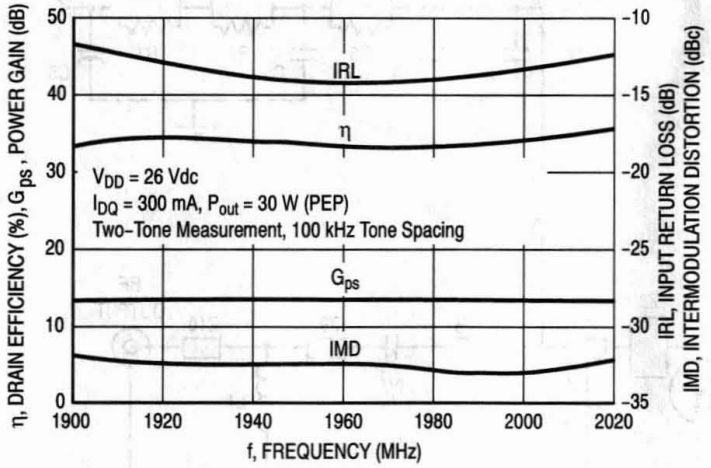


Figure 3. Class AB Broadband Circuit Performance

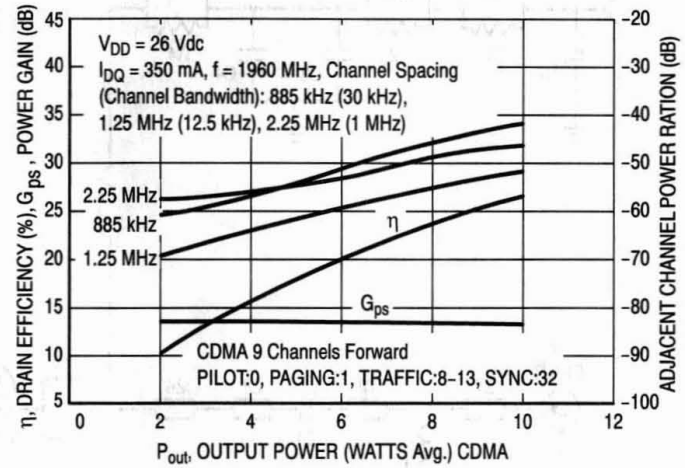


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

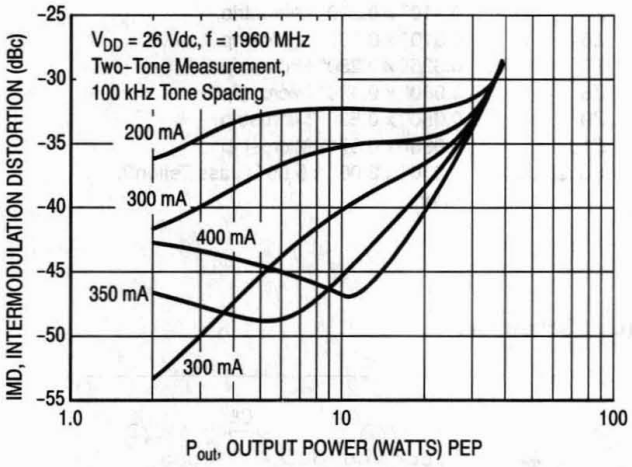


Figure 5. Intermodulation Distortion versus Output Power

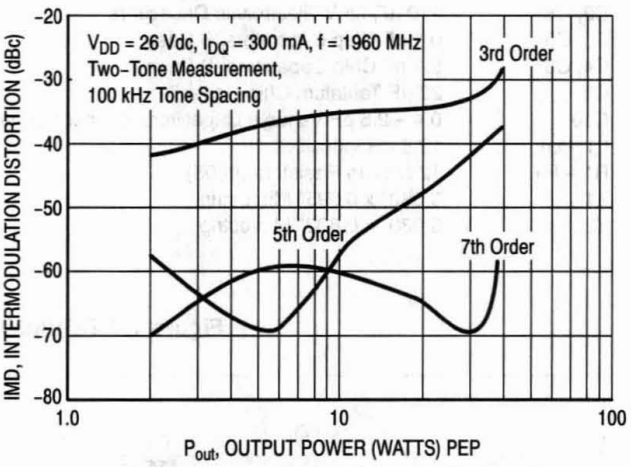


Figure 6. Intermodulation Distortion Products versus Output Power

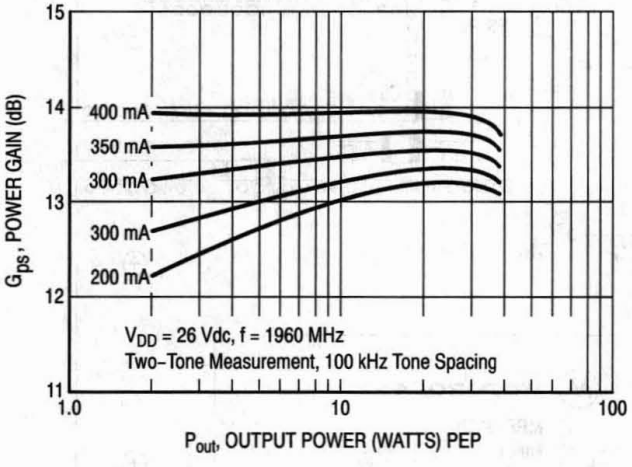


Figure 7. Power Gain versus Output Power

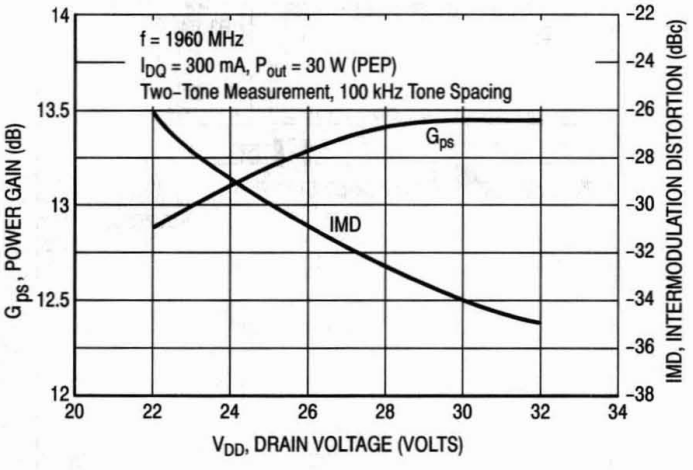
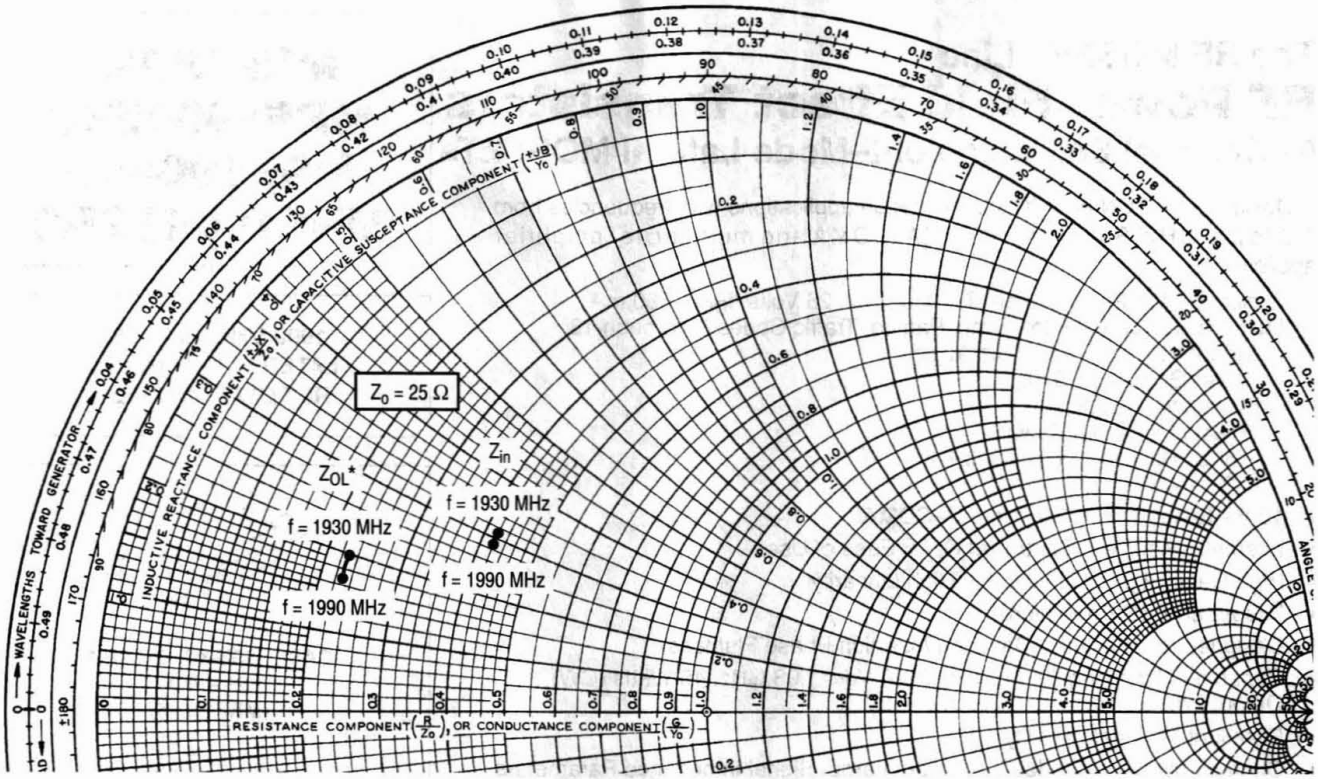


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 300 mA, P_{out} = 30 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	10.57 + j7.69	5.81 + j5.01
1960	10.54 + j7.43	5.84 + j4.67
1990	10.47 + j7.21	5.84 + j4.35

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

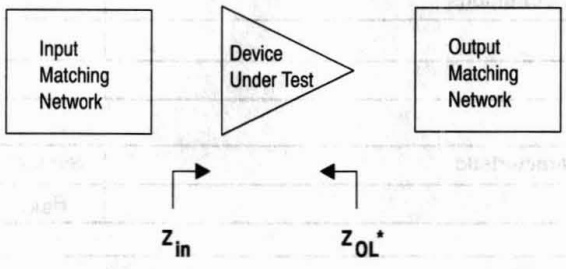


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

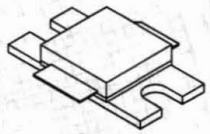
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19045
MRF19045R3
MRF19045S
MRF19045SR3

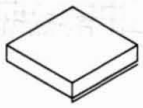
1990 MHz, 45 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

- Typical CDMA Performance @ 1960 MHz, 26 Volts, I_{DQ} = 550 mA
  Multi–carrier CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 9.5 Watts Avg.
  Power Gain — 14.9 dB
  Efficiency — 23.5%
  Adjacent Channel Power —
  885 kHz: –50 dBc @ 30 kHz BW
  IM3 — –37 dBc
- 100% Tested Under 2–Carrier N–CDMA
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1.93 GHz, 45 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.



CASE 465E–03, STYLE 1
(NI–400)
(MRF19045)



CASE 465F–03, STYLE 1
(NI–400S)
(MRF19045S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	105 0.60	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

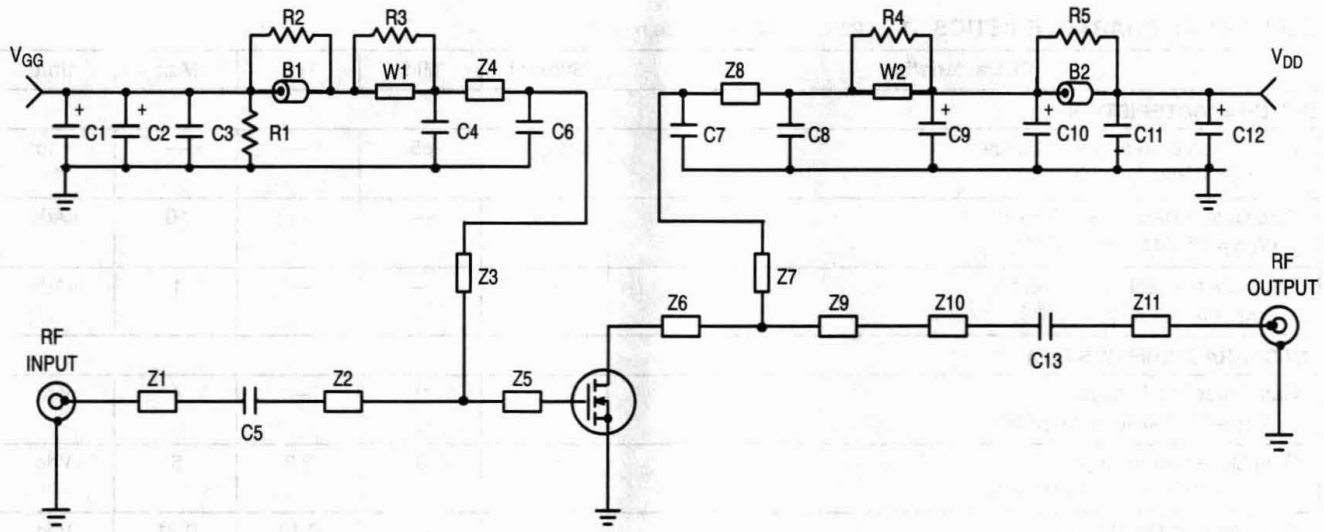
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (DC)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 550 mAdc)	$V_{GS(Q)}$	3	3.8	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.19	0.21	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	1.8	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture) 2–carrier N–CDMA, 1.2288 MHz Channel Bandwidth, IM3 measured in 1.2288 MHz Integrated Bandwidth. ACPR measured in 30 kHz Integrated Bandwidth.

Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–Carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 =1987.5 MHz, f2 = 1990 MHz)	G_{ps}	13	14.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–Carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 =1987.5 MHz, f2 = 1990 MHz)	η	21	23.5	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–Carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 =1987.5 MHz, f2 = 1990 MHz; IM3 Measured in a 1.2288 MHz Integrated Bandwidth Centered at f1 –2.5 Mhz and f2 +2.5 MHz, Referenced to the Carrier Channel Power)	IM3	—	–37	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; ACPR measured in a 30 kHz Integrated Bandwith Centered at f1 –885 kHz and f2 +885 kHz)	ACPR	—	–51	–45	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–Carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 =1987.5 MHz, f2 = 1990 MHz)	IRL	—	–16	–9	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 550 mA, f = 1990 MHz)	P1dB	—	45	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 45 W CW, I_{DQ} = 550 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



Z1	1.336″ x 0.081″ Microstrip	Z9	0.519″ x 0.254″ Microstrip
Z2	0.693″ x 0.081″ Microstrip	Z10	0.874″ x 0.081″ Microstrip
Z3	1.033″ x 0.047″ Microstrip	Z11	0.645″ x 0.081″ Microstrip
Z4	0.468″ x 0.047″ Microstrip	Board	3″ x 5″ Copper Clad PCB,
Z5	0.271″ x 0.460″ Microstrip		Arlon GX0300-55-22, ε_r = 2.55
Z6	0.263″ x 0.930″ Microstrip	Printed Circuit	CMR Part Number 19045PC5.SKF
Z7	1.165″ x 0.047″ Microstrip	Board	
Z8	0.216″ x 0.047″ Microstrip		

NOTE: Z3, Z4, Z7, Z8 lengths and component placement tolerances are ±0.050″.
Zx lengths are microstrip lengths between components, center-line to center-line.
All component and z-length tolerances are ±0.015″, except as noted.

Figure 1. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Schematic

Table 1. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Component Designations and Values

Designators	Description
B1, B2	0.120″ x 0.333″ x 0.100″, Surface Mount Ferrite Beads, Fair Rite #2743019446
C1, C2	10 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T495X106K035AS4394
C3, C11	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C4, C8	24 pF Chip Capacitors, B Case, ATC #100B240JP500X
C5	470 pF Chip Capacitor, B Case, ATC #100B471JP200X
C6, C7	11 pF Chip Capacitors, B Case, ATC #100B110JP500X
C9, C10, C12	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T491X226K035AS4394
C13	8.2 pF Chip Capacitor, B Case, ATC #100B8R2CP500X
R1	560 kΩ, 1/4 W Chip Resistor (0.08″ x 0.13″)
R2, R3, R4, R5	8.2 Ω, 1/4 W Chip Resistors (0.08″ x 0.13″), Garrett Instruments #RM73B2B110JT
W1, W2	Solid Copper Buss Wire, 16 AWG
WS1, WS2	Beryllium Copper Wear Blocks (0.005″ x 0.150″ x 0.350″) Nominal
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type “N” Jack Connectors, Omni-Spectra #3052-1648-10
	4-40 Ph Head Screws, 0.125″ long
	4-40 Ph Head Screws, 0.312″ long
	4-40 Ph Head Screws, 0.625″ long
	4-40 Ph Rec. Hd. Screws, 0.625″ long

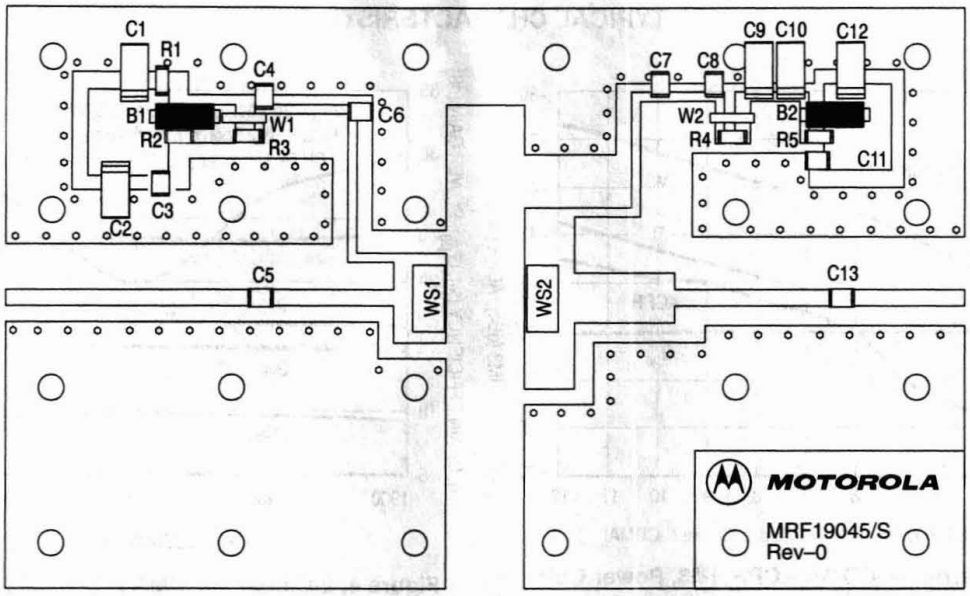


Figure 2. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Component Layout

TYPICAL CHARACTERISTICS

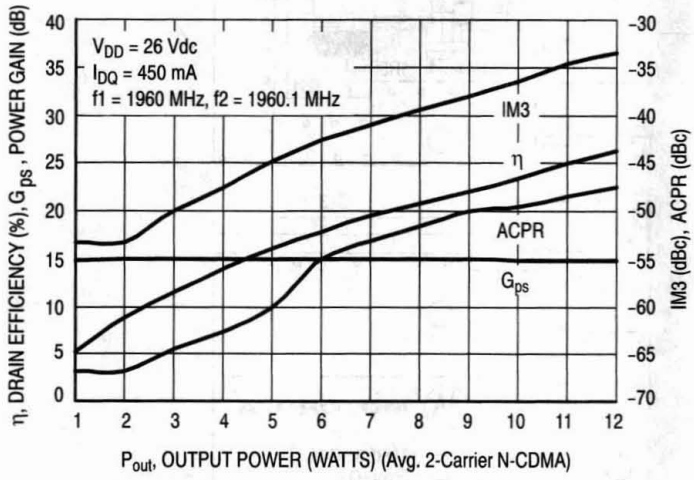


Figure 3. 2-Carrier N–CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

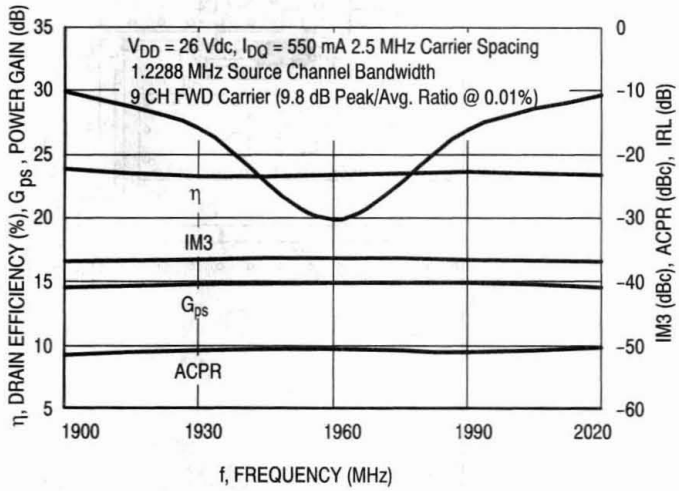


Figure 4. 2-Carrier N-CDMA ACPR, IM3, Power Gain, IRL and Drain Efficiency versus Output Power

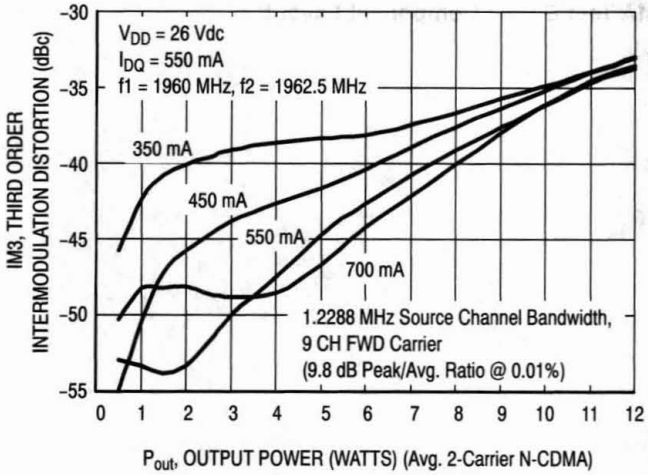


Figure 5. 2-Carrier N-CDMA IM3 versus Output Power

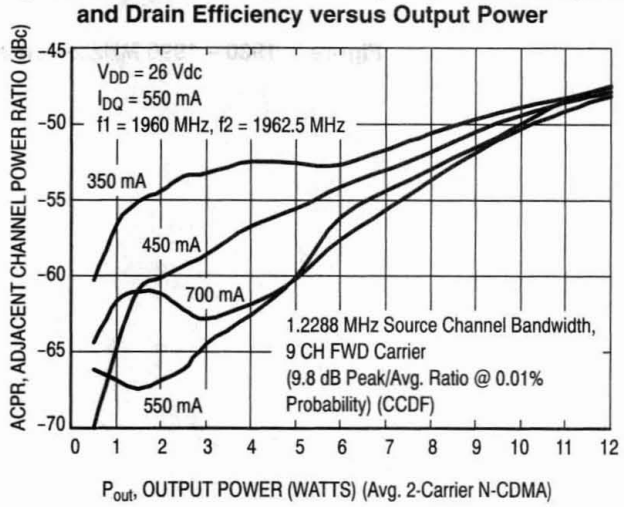


Figure 6. 2-Carrier N-CDMA ACPR versus Output Power

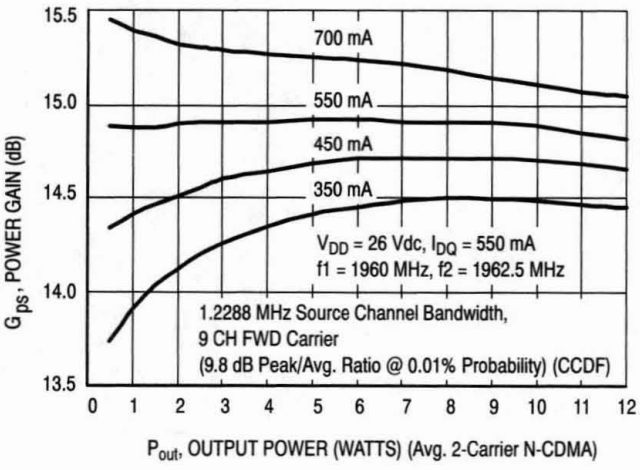


Figure 7. 2-Carrier N-CDMA Power Gain versus Output Power

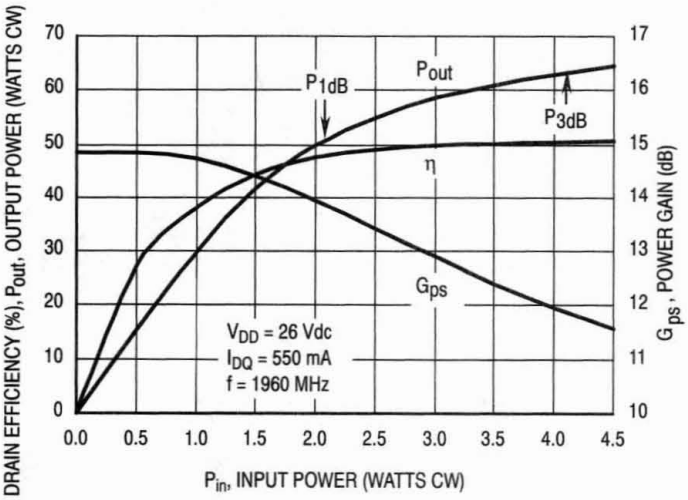


Figure 8. CW Output Power, Power Gain and Drain Efficiency versus Input Power

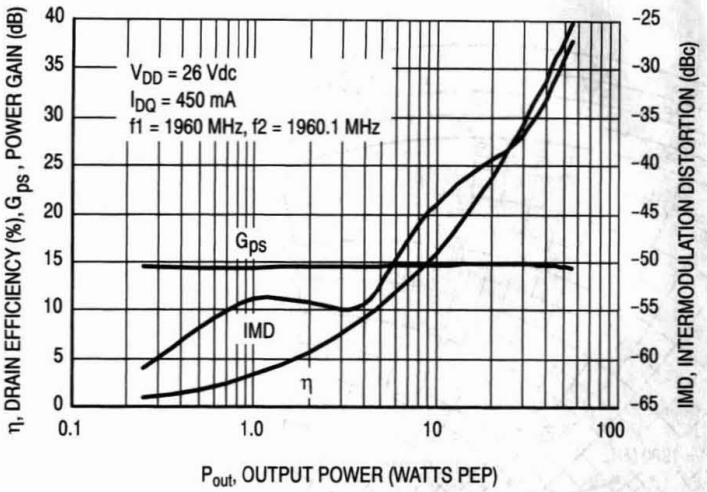


Figure 9. CW Two-Tone Power Gain, IMD and Drain Efficiency versus Output Power

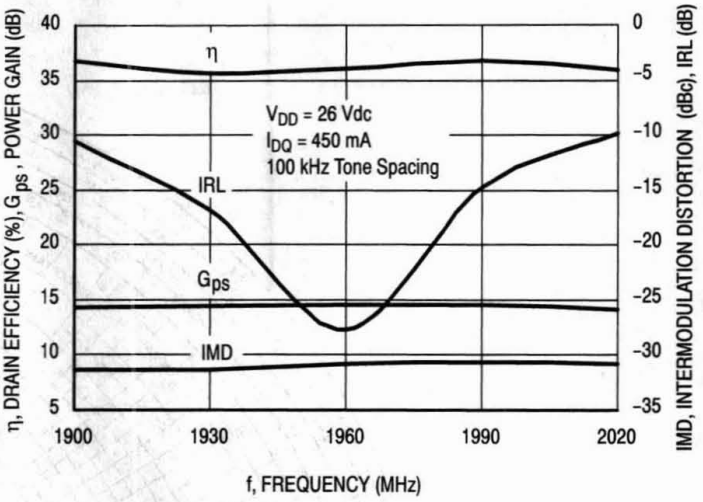


Figure 10. CW Two-Tone Power Gain, Input Return Loss, IMD and Drain Efficiency versus Frequency

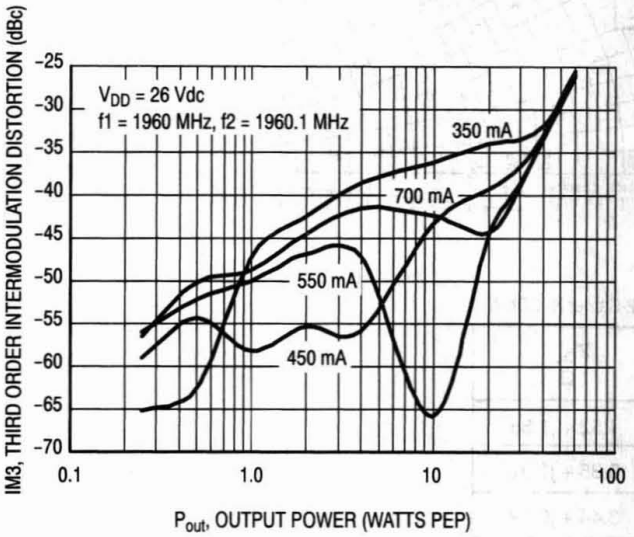


Figure 11. CW Two-Tone Intermodulation Distortion versus Output Power

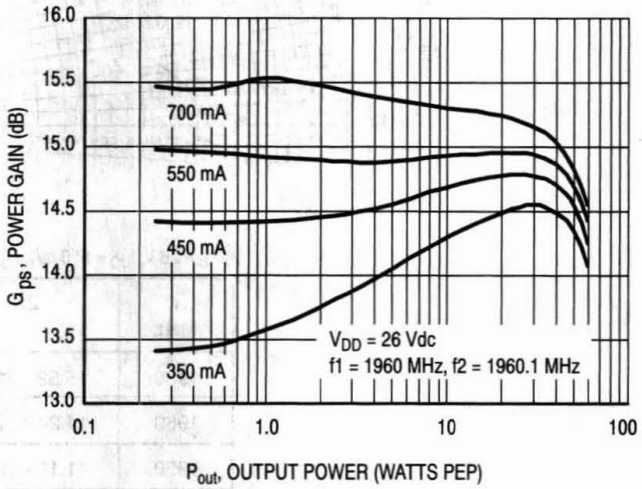


Figure 12. CW Two-Tone Power Gain versus Output Power

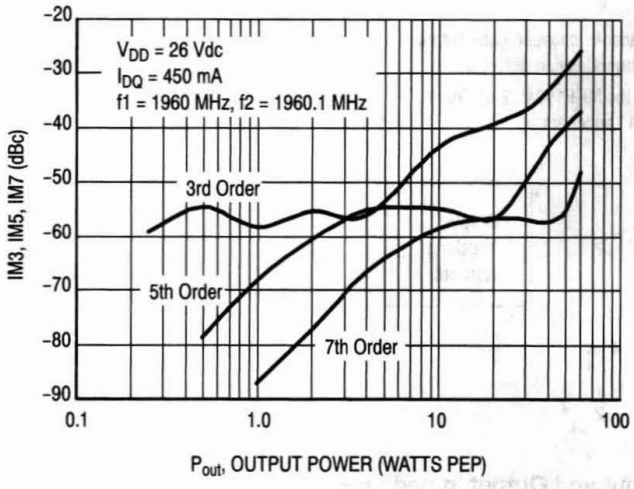


Figure 13. CW Two-Tone Intermodulation Distortion Products versus Output Power

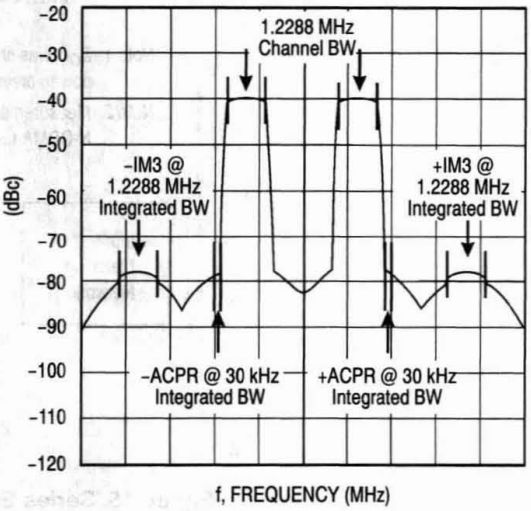
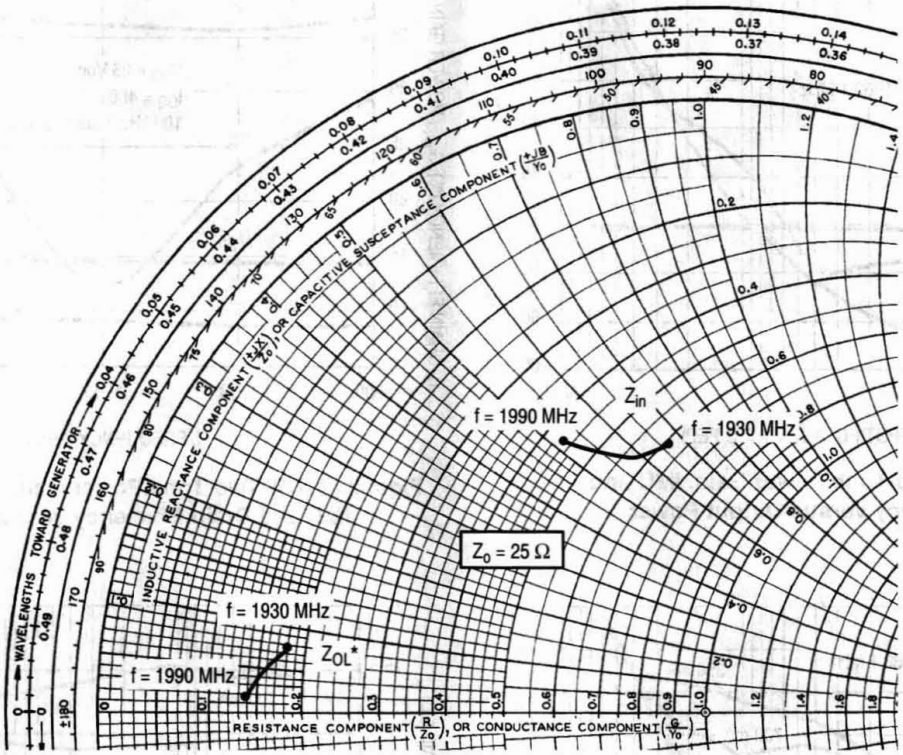


Figure 14. 2-Carrier N-CDMA Spectrum



V_{DD} = 26 V, I_{DQ} = 550 mA, P_{out} = 9 W_{avg}., 2-Carrier N-CDMA

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	15.52 + j16.5	4.52 + j1.86
1960	14.24 + j14.44	3.85 + j1.04
1990	11.11 + j13.01	3.44 + j0.69

Z_{in} = Complex conjugate of the optimum source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note 1: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Note 2: Measurements were taken on the MRF19045 2-carrier N-CDMA test circuit, with SMA Launchers.

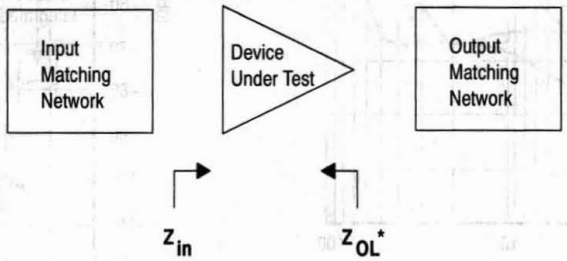


Figure 15. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

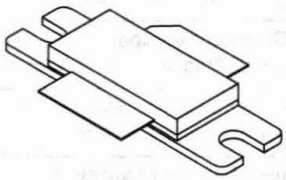
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19060
MRF19060R3
MRF19060S
MRF19060SR3

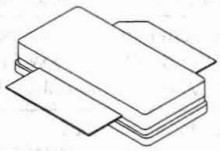
1990 MHz, 60 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM and multicarrier amplifier applications.

- Typical CDMA Performance: 1960 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 7.5 Watts
  Power Gain — 12.5 dB
  Adjacent Channel Power —
  885 kHz: –47 dBc @ 30 kHz BW
  1.25 MHz: –55 dBc @ 12.5 kHz BW
  2.25 MHz: –55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.



CASE 465–06, STYLE 1
(NI–780)
(MRF19060)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF19060S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ $T_C \geq = 25°C$ Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

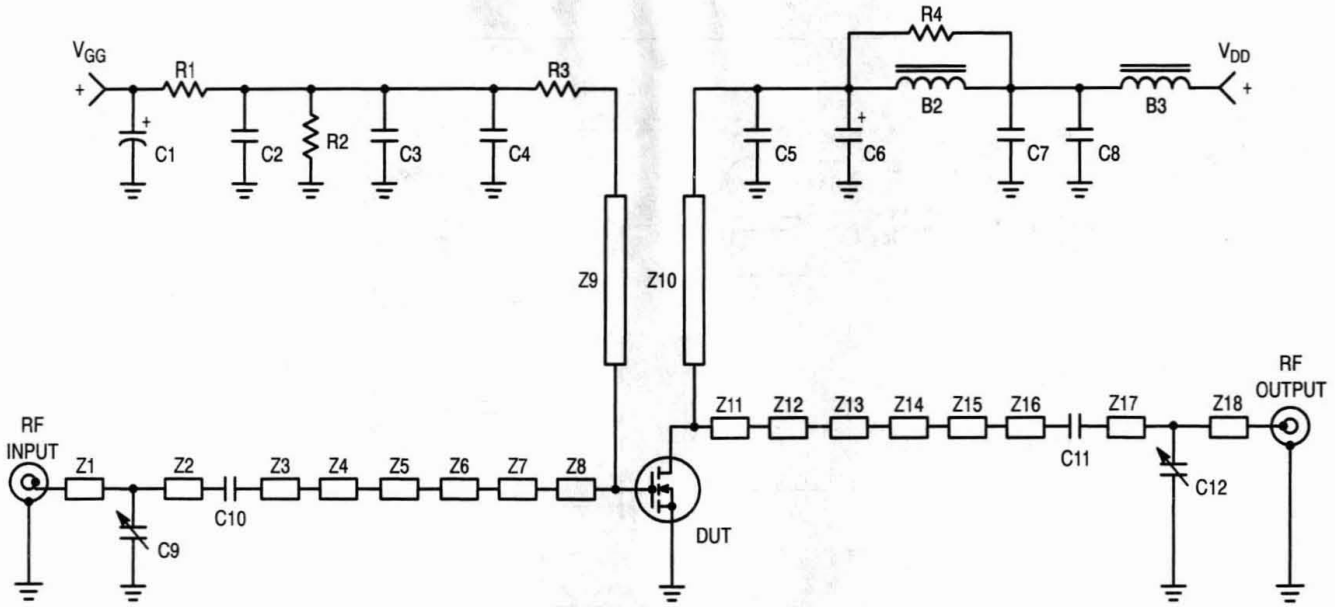
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$VGS_{(th)}$	2	—	4	V
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	V
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	V
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	33	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 60 W CW, f = 1990 MHz)	P1dB	—	60	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Beads, Fair Rite, 2743019447	Z4	0.152″ x 0.140″ Microstrip
C1	10 µF, 50 V Electrolytic Capacitor, Panasonic #ECEV1HV100R	Z5	0.090″ x 0.102″ Microstrip
C2, C7	1000 pF Chip Capacitors, B Case, ATC #100B102JCA500X	Z6	0.245″ x 0.217″ Microstrip
C3, C8	0.10 µF Chip Capacitors, B Case, Kemet #CDR33BX104AKWS	Z7	0.090″ x 0.737″ Microstrip
C4	5.1 pF Chip Capacitor, B Case, ATC #100B5R1JCA500X	Z8	0.530″ x 0.941″ Microstrip
C5	6.2 pF Chip Capacitor, B Case, ATC #100B6R2JCA500X	Z9	1.010″ x 0.050″ Microstrip
C6	22 µF, 35 V Tantalum Capacitor, SMT, Sprague	Z10	1.060″ x 0.050″ Microstrip
C9	0.8 pF – 8.0 pF Variable Capacitor, Johanson Gigatrim	Z11	0.446″ x 1.137″ Microstrip
C10, C11	10 pF Chip Capacitors, B Case, ATC #100B100JCA500X	Z12	0.152″ x 0.567″ Microstrip
C12	0.4 pF – 2.5 pF Variable Capacitor, Johanson Gigatrim	Z13	0.183″ x 0.220″ Microstrip
R1	1 kΩ, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″	Z14	0.100″ x 0.338″ Microstrip
R2	560 kΩ, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″	Z15	0.480″ x 0.142″ Microstrip
R3	15 Ω, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″	Z16	0.140″ x 0.080″ Microstrip
R4	10 Ω, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″	Z17	0.173″ x 0.080″ Microstrip
Z1	0.580″ x 0.074″ Microstrip	Z18	0.420″ x 0.080″ Microstrip
Z2	0.100″ x 0.074″ Microstrip	Board	0.030″ Glass Teflon® Arlon
Z3	0.384″ x 0.074″ Microstrip		GX–0300–55–22, 2 oz Cu

Figure 1. MRF19060 Test Circuit Schematic

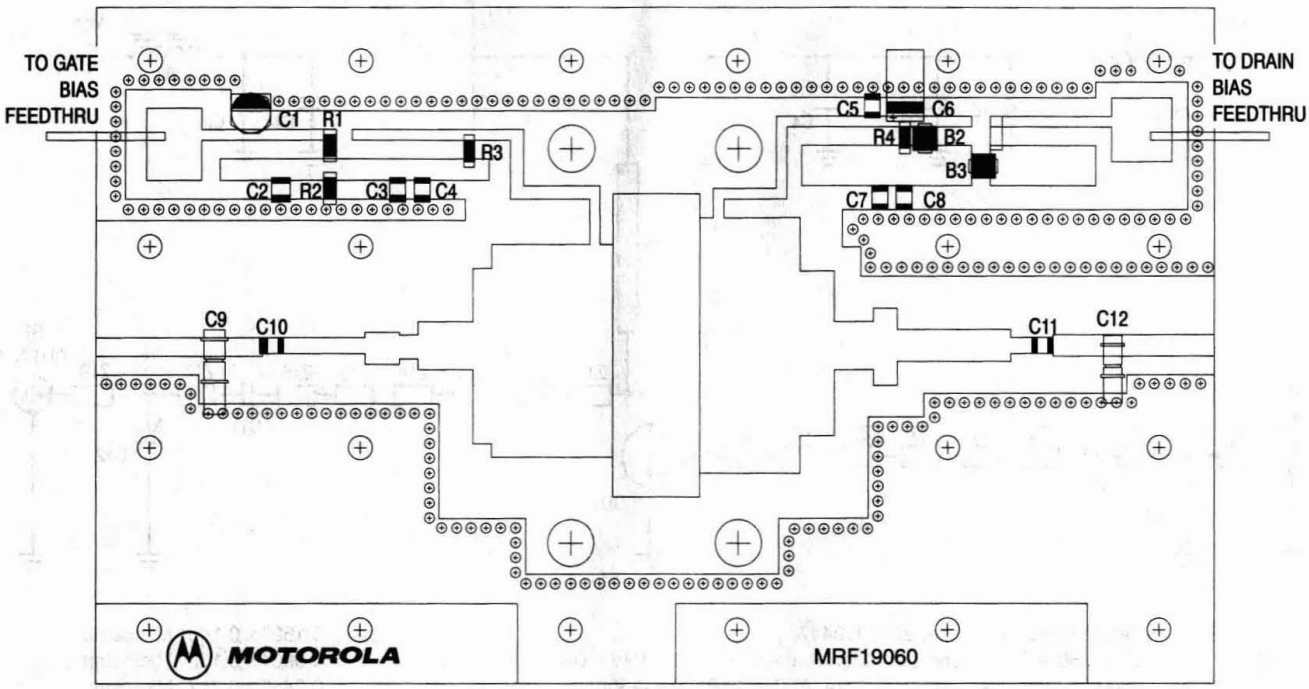


Figure 2. MRF19060 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

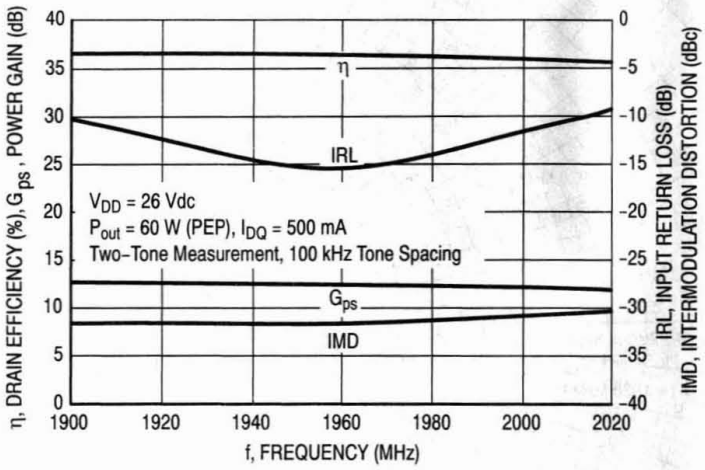


Figure 3. Class AB Broadband Circuit Performance

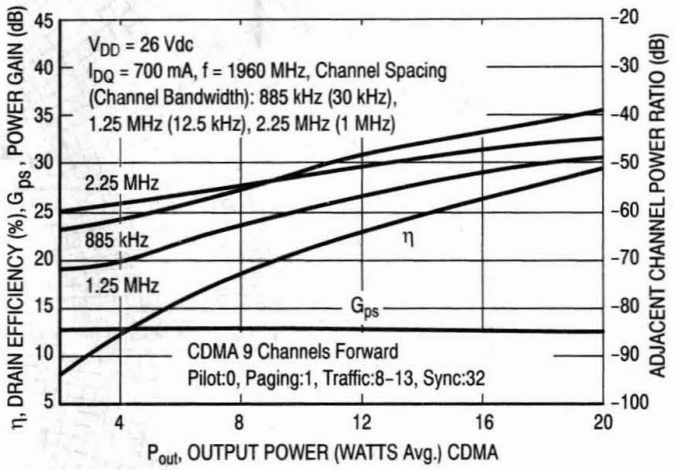


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

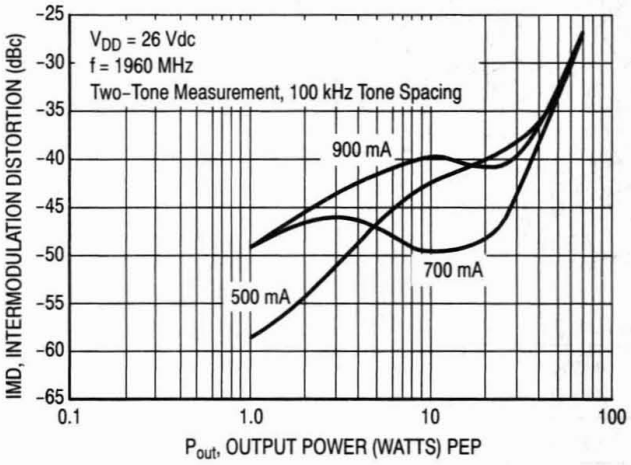


Figure 5. Intermodulation Distortion versus Output Power

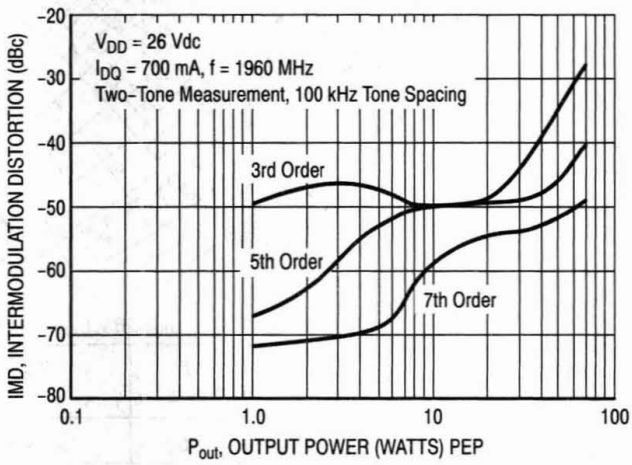


Figure 6. Intermodulation Products versus Output Power

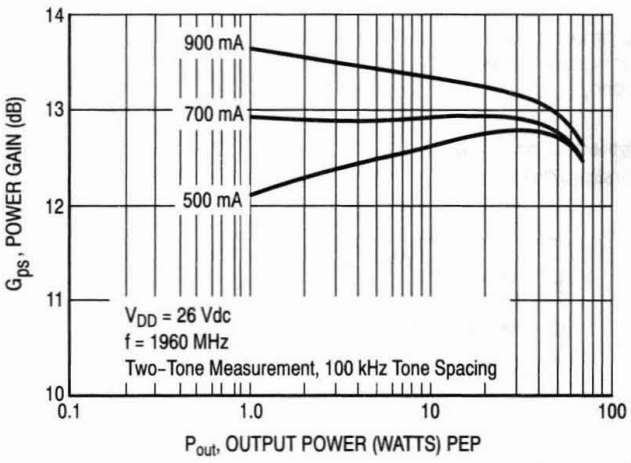


Figure 7. Power Gain versus Output Power

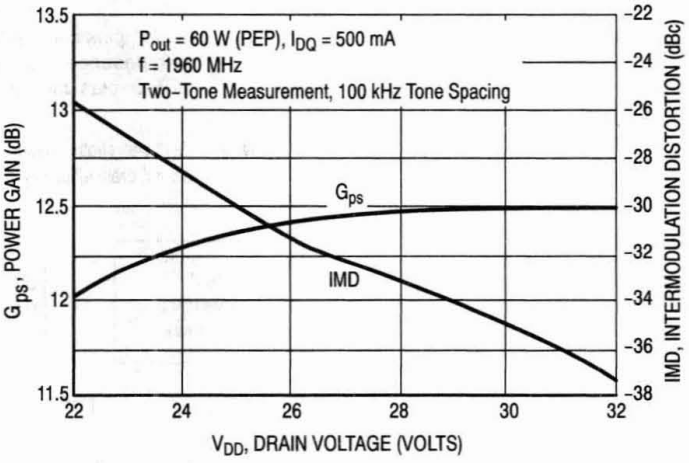
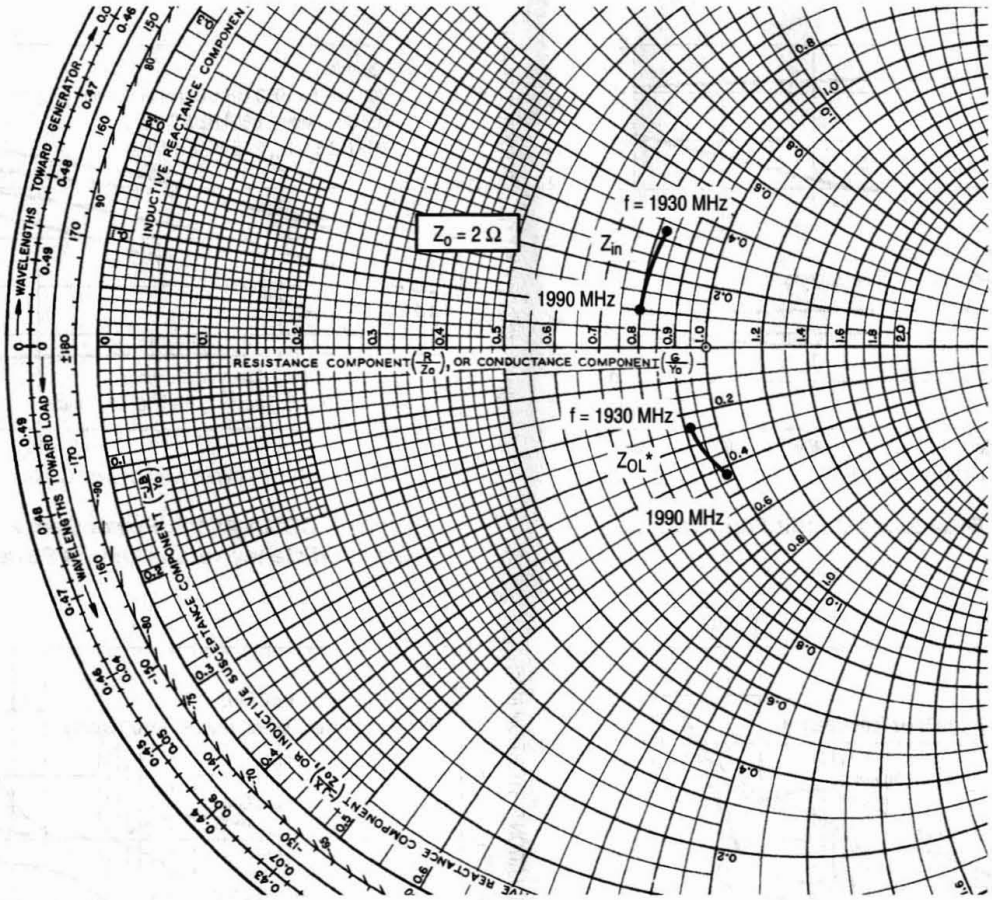


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1930	1.65 + j0.67	1.85 – j0.50
1960	1.64 + j0.45	1.89 – j0.74
1990	1.60 + j0.20	1.96 – j0.94

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

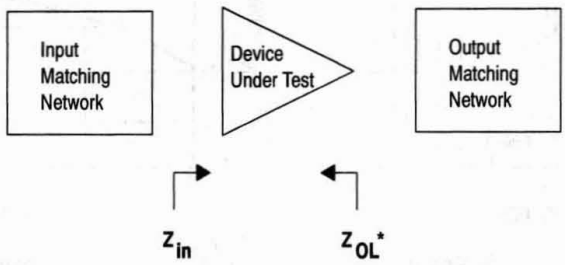


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

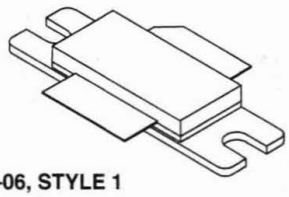
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19085
MRF19085R3
MRF19085S
MRF19085SR3
MRF19085LS
MRF19085LSR3

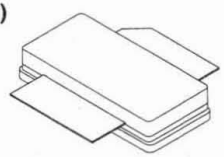
1990 MHz, 90 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

- Typical 2–Carrier N–CDMA Performance for V_{DD} = 26 Volts, I_{DQ} = 850 mA, P_{out} = 18 Watts Avg., f1 = 1960 MHz, f2 = 1962.5 MHz IS–95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13) 1.2288 MHz Channel Bandwidth Carrier. Adjacent Channels Measured over a 30 kHz Bandwidth at f1 –885 Khz and f2 +885 kHz. Distortion Products Measured over 1.2288 MHz Bandwidth at f1 –2.5 MHz and f2 +2.5 MHz. Peak/Avg. = 9.8 dB @ 0.01% Probability on CCDF.
  Output Power — 18 Watts Avg.
  Power Gain — 13.0 dB
  Efficiency — 23%
  ACPR — –51 dB
  IM3 — –36.5 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1.93 GHz, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ″ Nominal.



CASE 465–06, STYLE 1
(NI–780)
(MRF19085)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF19085S, MRF19085LS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	273 1.56	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.64	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (DC)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 850 mAdc)	$V_{GS(Q)}$	2.5	3.5	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.18	0.210	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	6	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	3.6	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) 2–Carrier N–CDMA, 1.2288 MHz Channel Bandwidth Carriers. Peak/Avg. Ratio = 9.8 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 18 W Avg., I_{DQ} = 850 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 =1990 MHz)	G_{ps}	12	13	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 18 W Avg., I_{DQ} = 850 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 =1990 MHz)	η	21	23	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 18 W Avg., I_{DQ} = 850 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 =1990 MHz); IM3 measured over 1.2288 MHz bandwidth @ f1 –2.5 MHz and f2 = +2.5 MHz)	IMD	—	–36.5	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 26 Vdc, P_{out} = 18 W Avg., I_{DQ} = 850 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 =1990 MHz); ACPR measured over 30 kHz bandwidth @ f1 –885 MHz and f2 =+885 MHz)	ACPR	—	–51	–48	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 18 W Avg., I_{DQ} = 850 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 =1990 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 850 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 850 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 850 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	—	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 850 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 850 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 850 mA, f = 1990 MHz)	P1dB	—	90	—	W

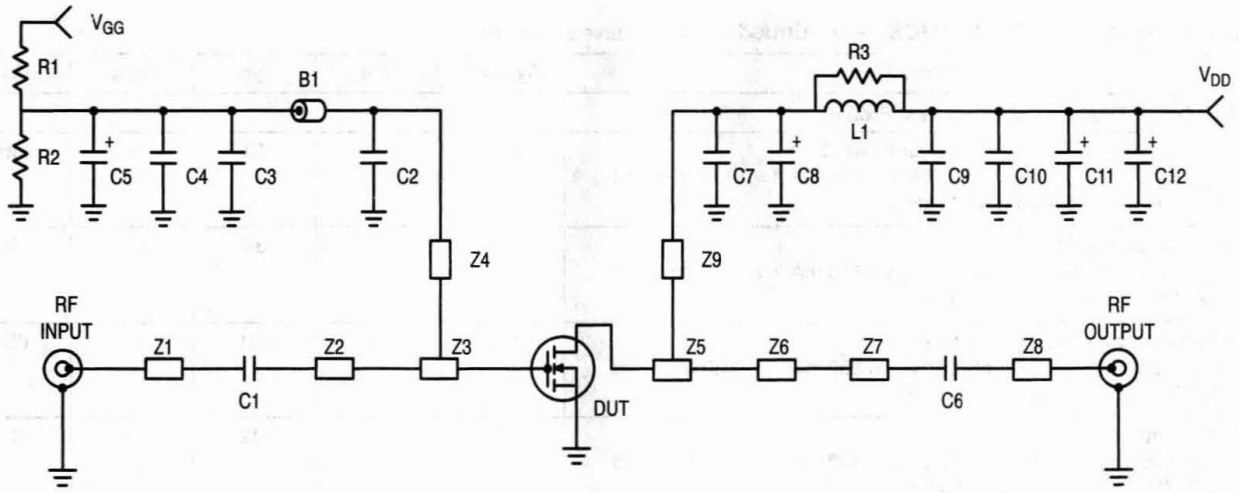


Figure 1. 1930 – 1990 MHz 2–Carrier N–CDMA Test Circuit Schematic

Table 1. 1930 – 1990 MHz 2–Carrier N–CDMA Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1	Short Ferrite Bead	2743019447	Fair Rite
C1	51 pF Chip Capacitor	100B510JCA500X	ATC
C2, C7	5.1 pF Chip Capacitors	100B5R1JCA500X	ATC
C3, C9	1000 pF Chip Capacitors	100B102JCA500X	ATC
C4, C10	0.1 μF Chip Capacitors	CDR33BX104AKWS	Kemet
C5	0.1 μF Tantalum Surface Mount Capacitor	T491C105M050	Kemet
C6	10 pF Chip Capacitor	100B100JCA500X	ATC
C8	10 μF Tantalum Surface Mount Capacitor	T495X106K035AS4394	Kemet
C11, C12	22 μF Tantalum Surface Mount Capacitors	T491X226K035AS4394	Kemet
L1	1 Turn, 20 AWG, 0.100″ ID		Motorola
N1, N2	Type N Flange Mounts	3052-1648-10	Omni Spectra
R1	1.0 kΩ, 1/8 W Chip Resistor		
R2	220 kΩ, 1/8 W Chip Resistor		
R3	10 Ω, 1/8 W Chip Resistor		
Z1	Microstrip	0.750″ x 0.0840″	
Z2	Microstrip	1.090″ x 0.0840″	
Z3	Microstrip	0.400″ x 1.400″	
Z4	Microstrip	0.520″ x 0.050″	
Z5	Microstrip	0.540″ x 1.133″	
Z6	Microstrip	0.400″ x 0.140″	
Z7	Microstrip	0.555″ x 0.0840″	
Z8	Microstrip	0.720″ x 0.0840″	
Z9	Microstrip	0.560″ x 0.070″	
Board	0.030″ Glass Teflon®	GX-0300-55-22, ε_r = 2.55	Keene
PCB	Etched Circuit Boards	MRF19085 Rev. 4	CMR

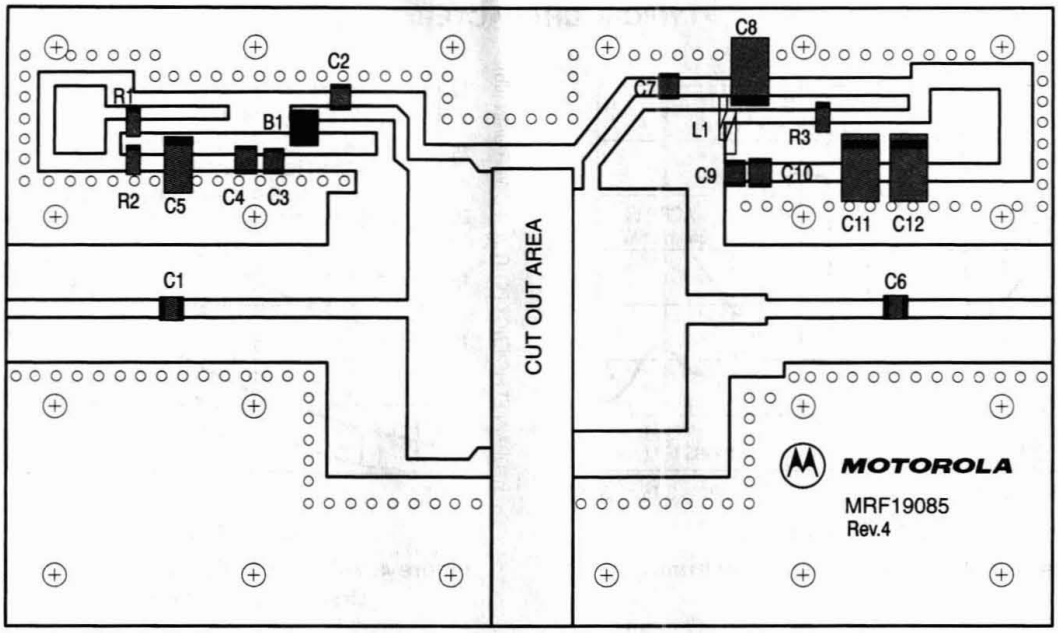


Figure 2. 1930 – 1990 MHz 2–Carrier N–CDMA Test Circuit Component Layout

TYPICAL CHARACTERISTICS

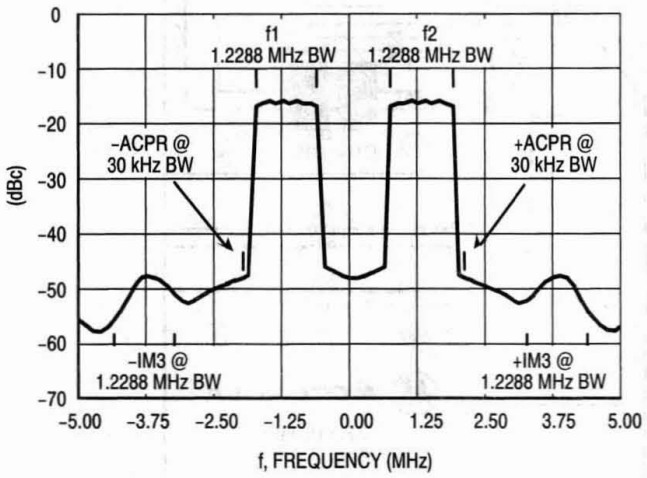


Figure 3. 2-Carrier N-CDMA Spectrum

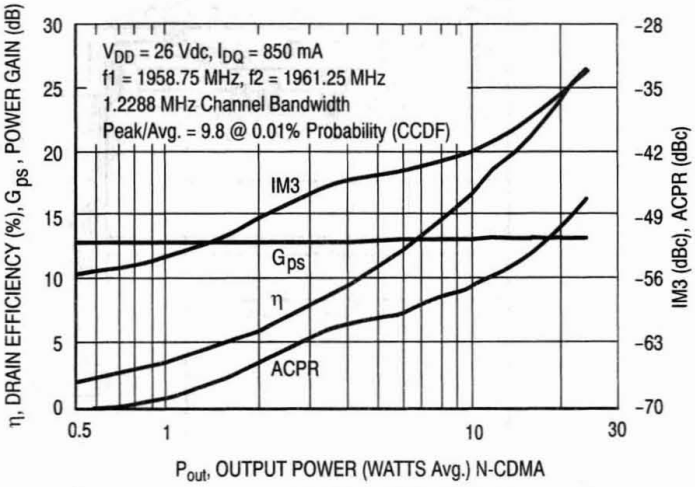


Figure 4. 2-Carrier N–CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

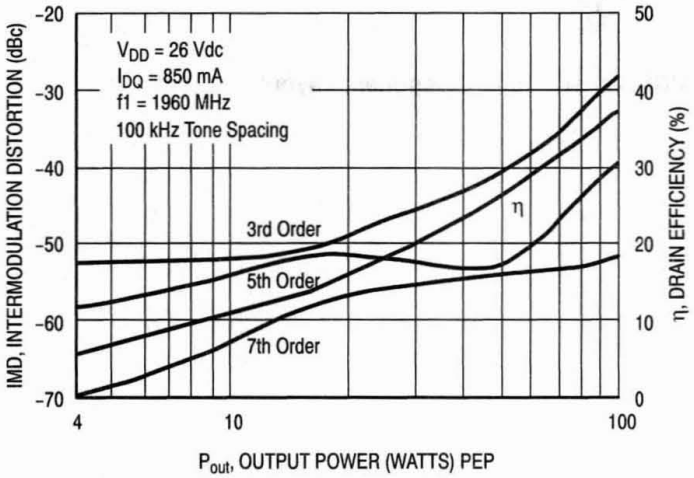


Figure 5. Intermodulation Distortion Products versus Output Power

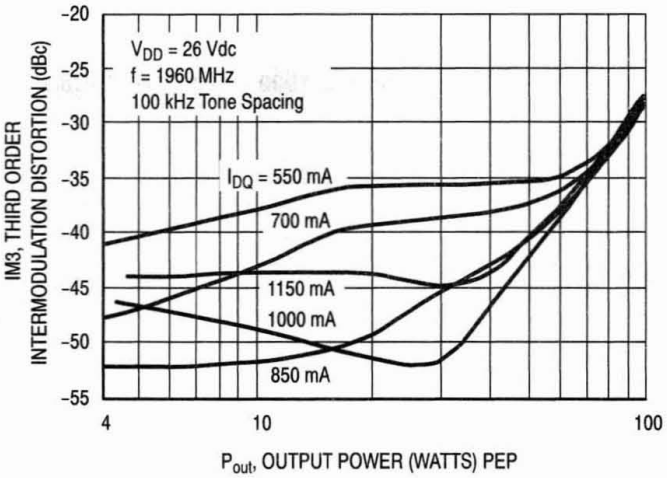


Figure 6. Third Order Intermodulation Distortion versus Output Power and I_{DQ}

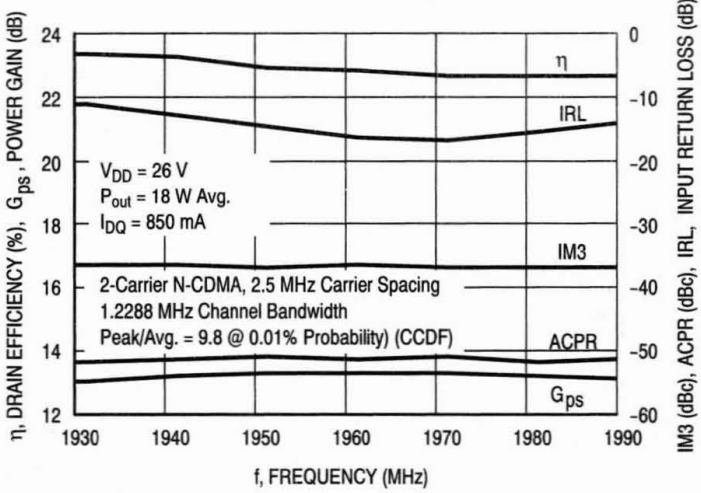


Figure 7. 2-Carrier N-CDMA Broadband Performance

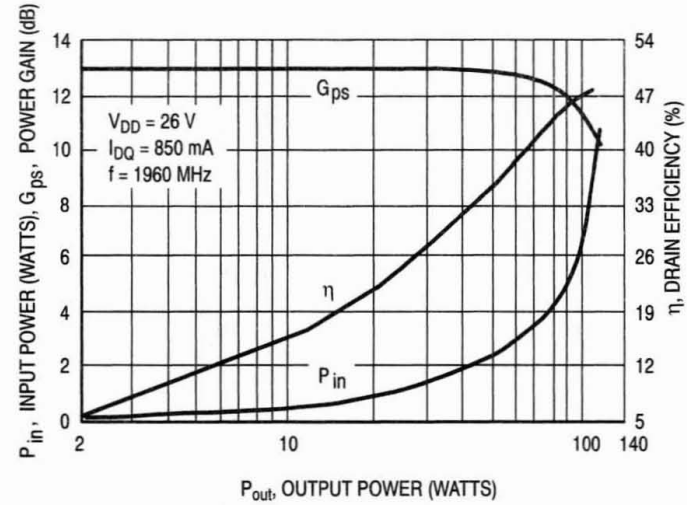


Figure 8. CW Performance

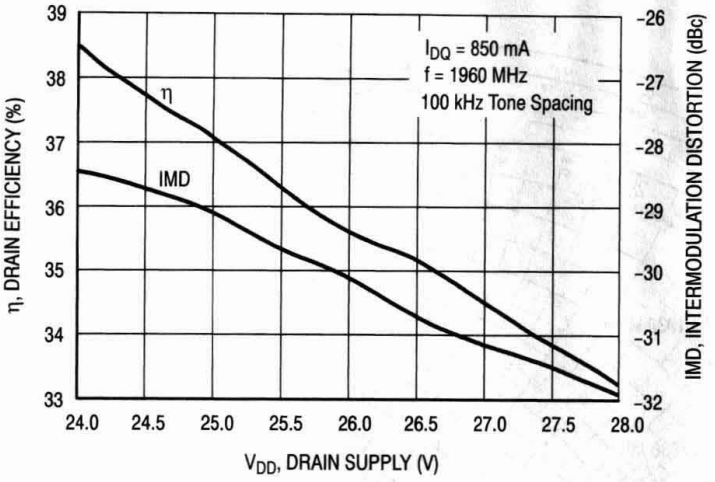


Figure 9. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

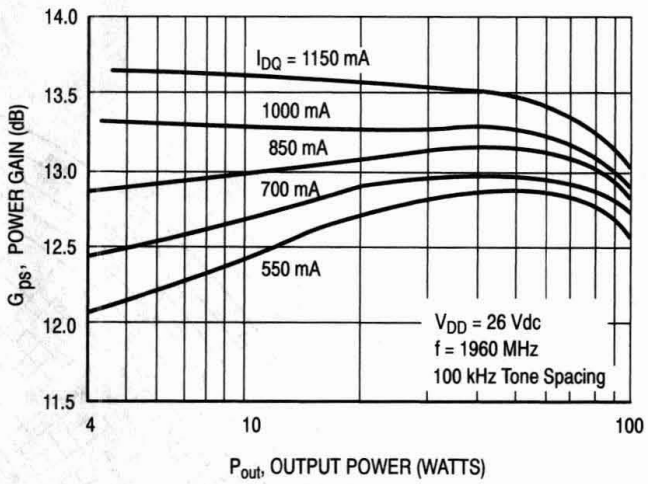


Figure 10. Two-Tone Power Gain versus Output Power

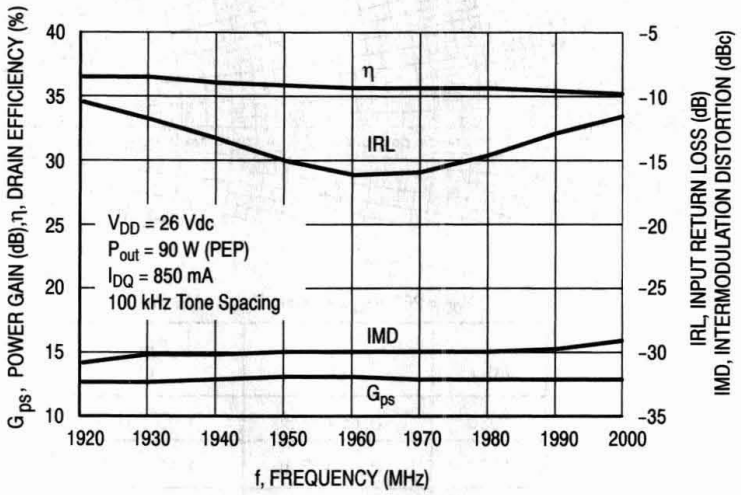
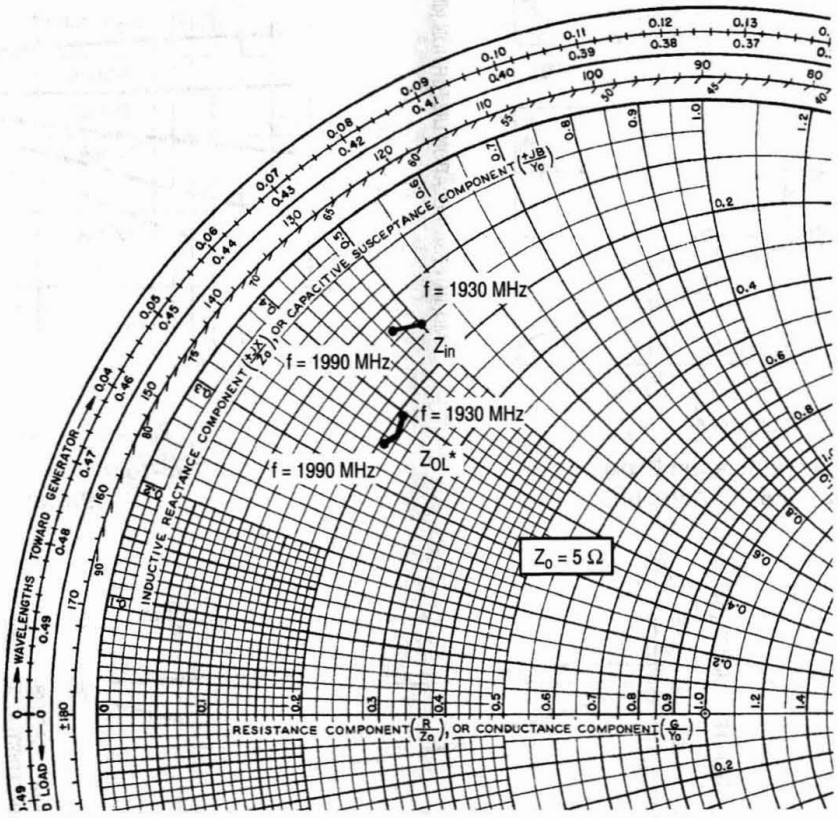


Figure 11. Two-Tone Broadband Performance



V_{DD} = 26 V, I_{DQ} = 850 mA, P_{out} = 18 W (Avg.)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	0.75 + j2.50	1.05 + j1.95
1960	0.70 + j2.40	1.10 + j1.85
1990	0.65 + j2.35	1.05 + j1.75

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

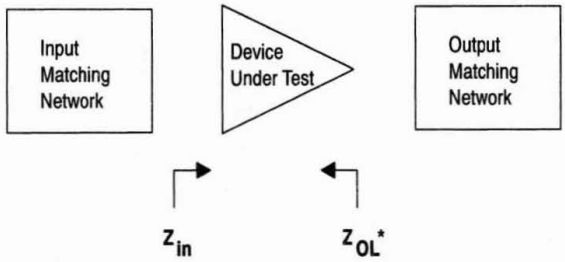


Figure 12. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

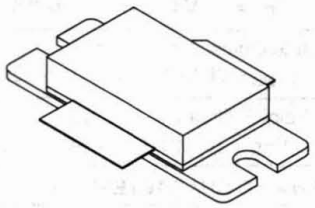
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19090
MRF19090S
MRF19090SR3

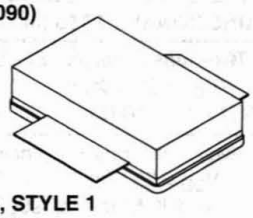
Designed for Class AB PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM, and multicarrier amplifier applications.

- Typical CDMA Performance: 1990 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 9 Watts
  Power Gain — 10 dB
  Adjacent Channel Power —
  885 kHz: –47 dBc @ 30 kHz BW
  1.25 MHz: –55 dBc @ 12.5 kHz BW
  2.25 MHz: –55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

1990 MHz, 90 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465B–03, STYLE 1
(NI–880)
(MRF19090)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF19090S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C > = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

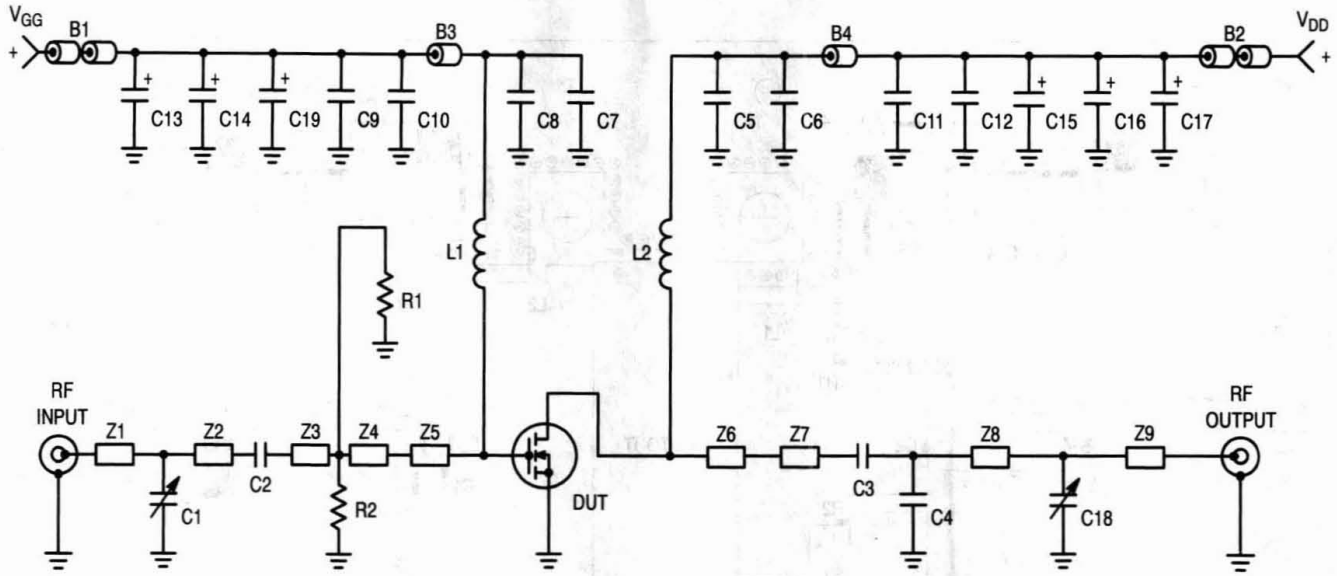
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$VGS_{(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.8	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.10	—	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	10	11.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	33	35	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 90 W CW, f = 1990 MHz)	P1dB	—	90	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1, B2	2 Ferrite Beads, Round, Ferroxcube #56–590–65–3B	L1, L2	8 Turns, #26 AWG, 0.085″ OD, 0.330″ Long, Copper Wire
B3, B34	Ferrite Beads, Surface Mount, Ferroxcube	R1, R2	270 Ω, 1/4 W Chip Resistors, Garrett Instruments #RM73B2B271JT
C1, C18	0.4 – 2.5 pF Variable Capacitors, Johanson Gigatrim #27285	Z1	ZO = 50 Ohms
C2, C5, C8	10 pF Chip Capacitors, B Case, ATC #100B100CCA500X	Z2	ZO = 50 Ohms, Lambda = 0.123
C3	12 pF Chip Capacitor, B Case, ATC #100B120CCA500X	Z3	ZO = 15.24 Ohms, Lambda = 0.0762
C4	0.3 pF Chip Capacitor, B Case, ATC #100B0R3CCA500X	Z4	ZO = 10.11 Ohms, Lambda = 0.0392
C6, C7	120 pF Chip Capacitors, B Case, ATC #100B12R1CCA500X	Z5	ZO = 6.34 Ohms, Lambda = 0.0711
C9, C12	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS	Z6	ZO = 5.02 Ohms, Lambda = 0.0476
C10, C11	1000 pF Chip Capacitors, B Case, ATC #100B102JCA50X	Z7	ZO = 5.54 Ohms, Lambda = 0.0972
C13, C17	22 μF, 35 V Tantalum Chip Capacitors, Kemet #T491X226K035AS4394	Z8	ZO = 50.0 Ohms, Lambda = 0.194
C14, C16	10 μF, 35 V Tantalum Chip Capacitors, Kemet #T495X106K035AS4394	Z9	ZO = 50.0 Ohms
C15, C19	1 μF, 35 V Tantalum Chip Capacitors, Kemet #T495X105K035AS4394	Raw PCB Material	0.030″ Glass Teflon®, ε_r = 2.55, 2 oz Copper, 3″ x 5″ Dimensions

Figure 1. MRF19090 Test Circuit Schematic

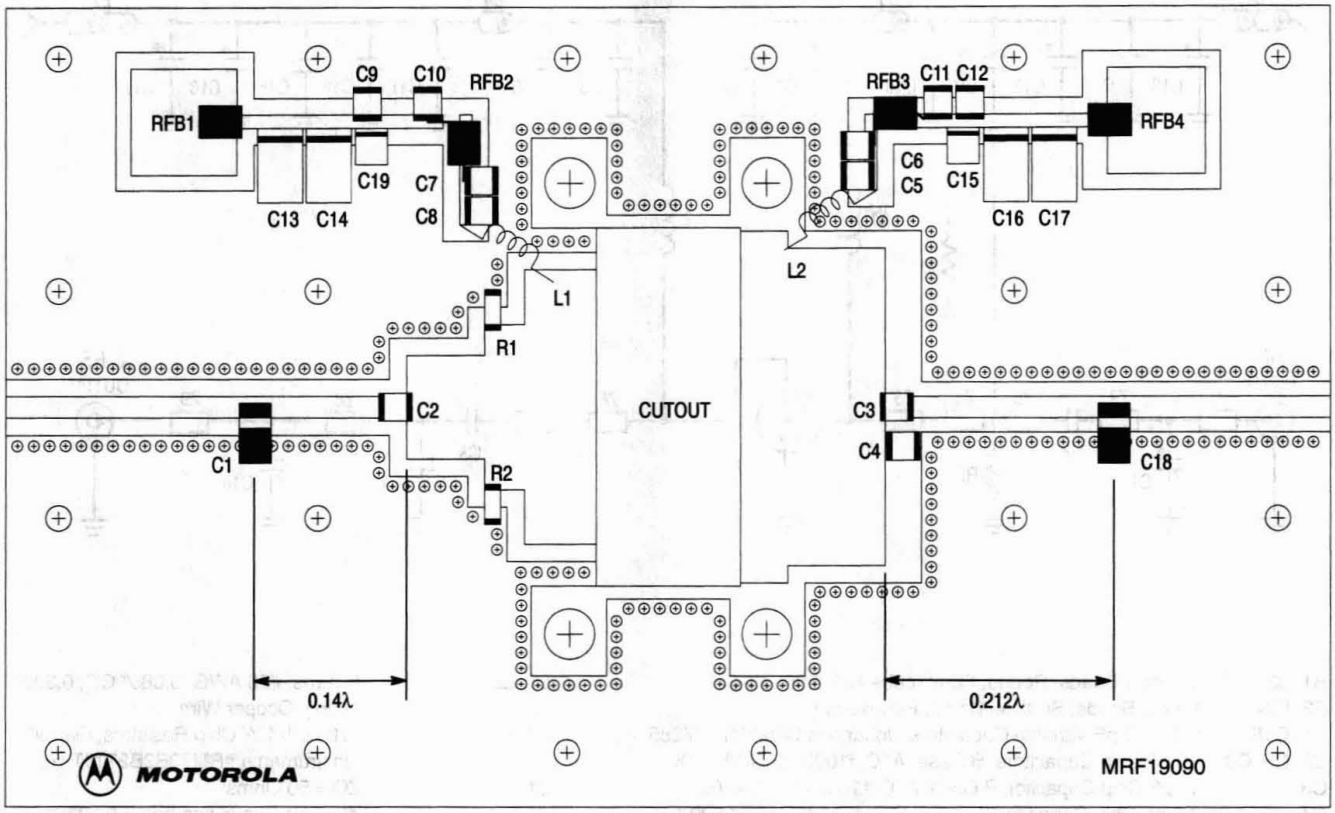


Figure 2. MRF19090 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

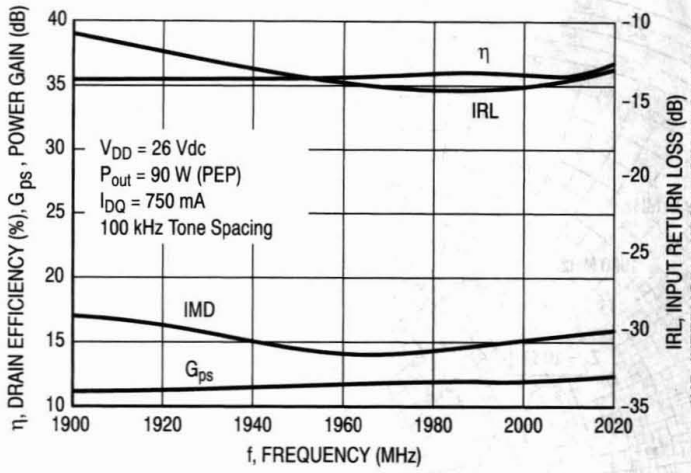


Figure 3. Class AB Performance versus Frequency

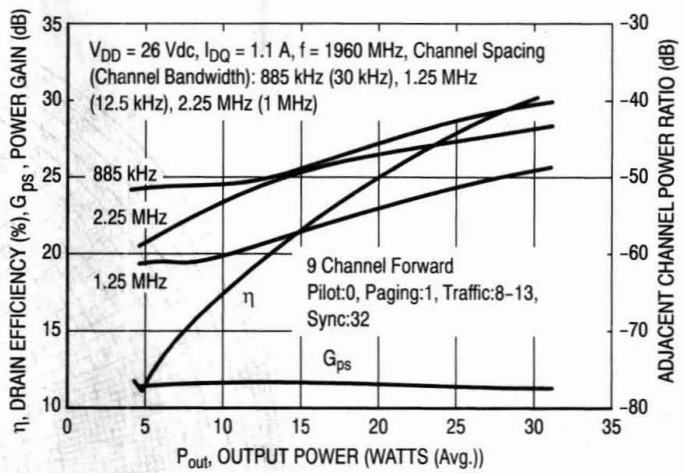


Figure 4. CDMA Performance ACPR, Gain and Drain Efficiency versus Output Power

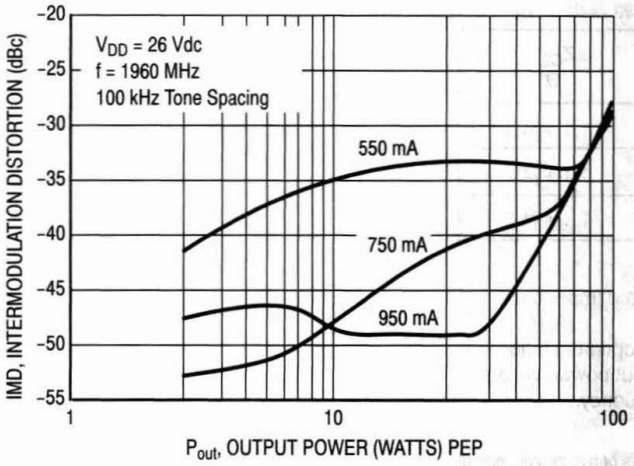


Figure 5. Third Order Intermodulation Distortion versus Output Power

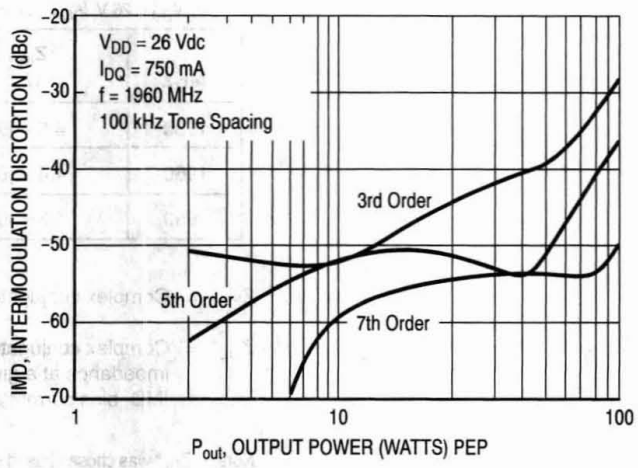


Figure 6. Intermodulation Products versus Output Power

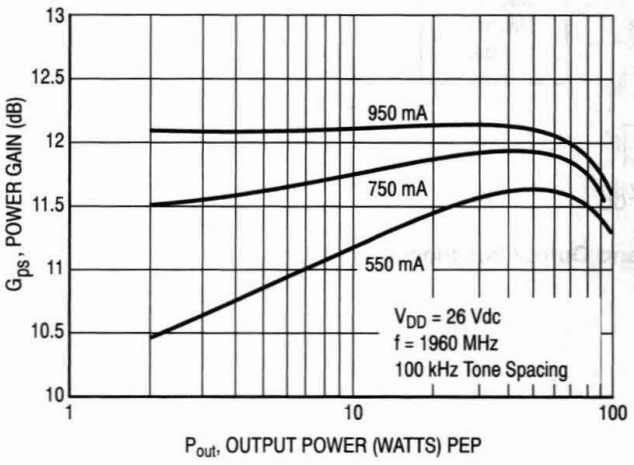


Figure 7. Power Gain versus Output Power

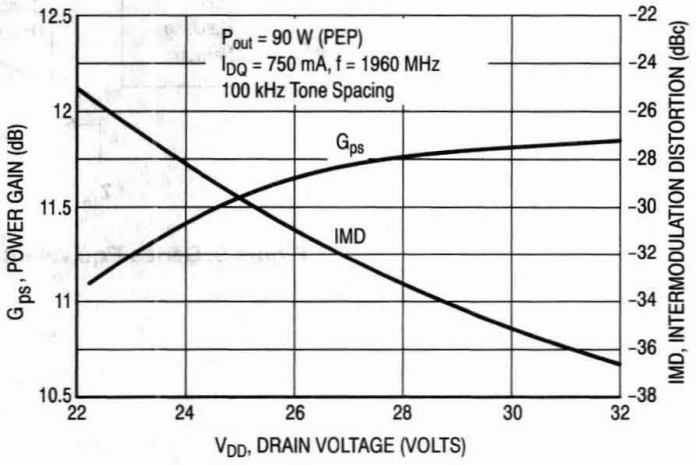
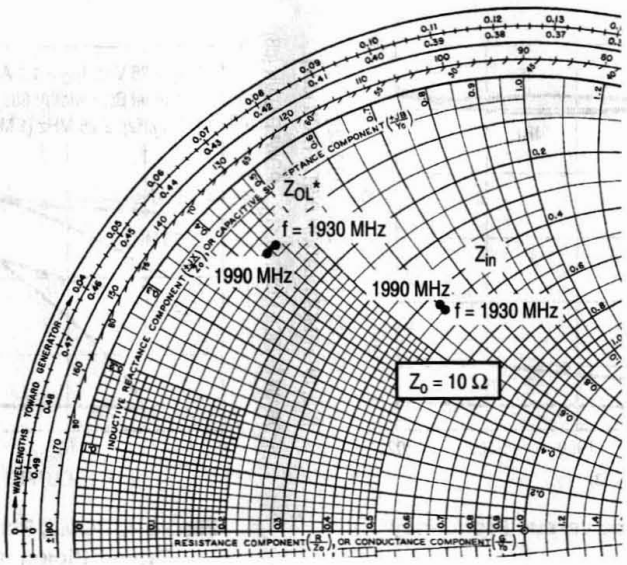


Figure 8. Third Order Intermodulation Distortion and Gain versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1930	4.5 + j6.1	1.1 + j4.5
1960	4.4 + j6.0	1.1 + j4.4
1990	4.3 + j6.1	1.1 + j4.3

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

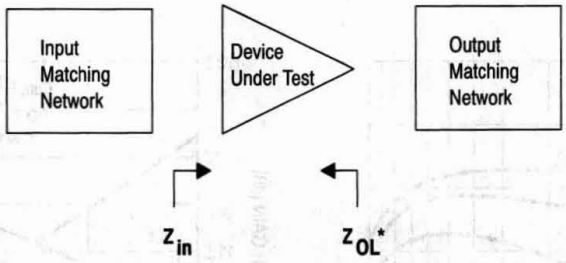


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

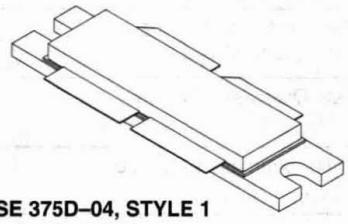
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19120
MRF19120S

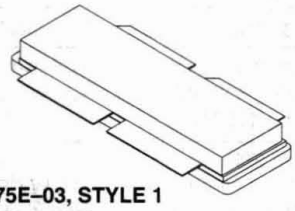
1990 MHz, 120 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- CDMA Performance @ 1990 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
  885 kHz — –47 dBc @ 30 kHz BW
  1.25 MHz — –55 dBc @ 12.5 kHz BW
  2.25 MHz — –55 dBc @ 1 MHz BW
  Output Power — 15 Watts (Avg.)
  Power Gain — 11.7 dB
  Efficiency — 16%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency, High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1990 MHz, 120 Watts (CW) Output Power
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 375D–04, STYLE 1
(NI–1230)
(MRF19120)



CASE 375E–03, STYLE 1
(NI–1230S)
(MRF19120S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	389 2.22	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

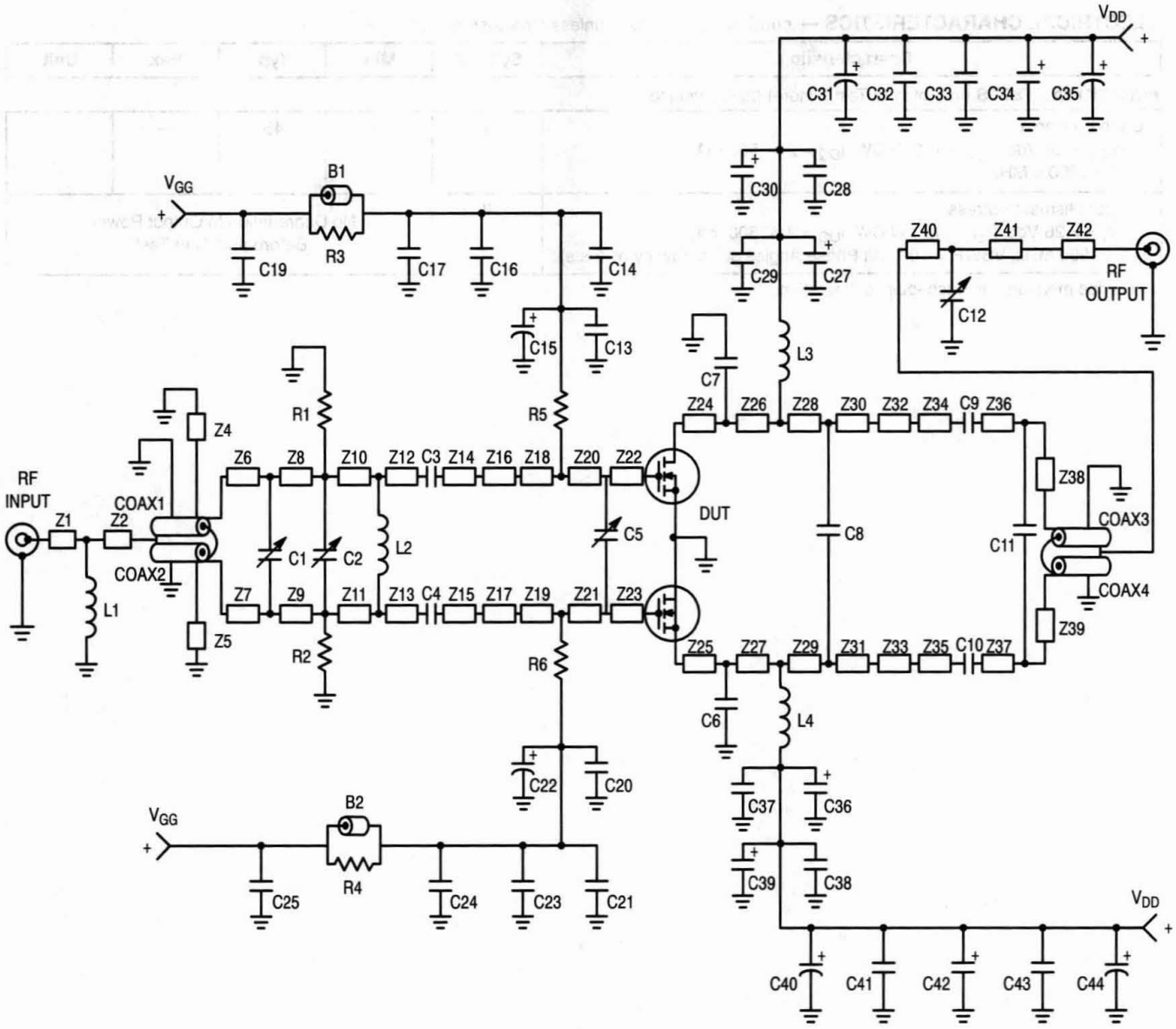
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)		$V_{(BR)DSS}$	65	—	—	Vdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
ON CHARACTERISTICS (1)						
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)		g_{fs}	—	4.8	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)		$V_{GS(th)}$	2.5	3	3.8	Vdc
Gate Quiescent Voltage (V_{DS} = 26 V, I_D = 500 mA)		$V_{GS(Q)}$	3	3.9	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 2 A)		$V_{DS(on)}$	—	0.38	0.5	Vdc
DYNAMIC CHARACTERISTICS (1)						
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	2.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)						
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 1990.0 MHz, f2 = 1990.1 MHz)	MRF19120 MRF19120S	G_{ps}	10.7 10.5	11.7 11.7	— —	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 1990.0 MHz, f2 = 1990.1 MHz)		η	30	34	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 1990.0 MHz, f2 = 1990.1 MHz)	MRF19120 MRF19120S	IMD	— —	–31 –31	–28 –27	dB
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 1990.0 MHz, f2 = 1990.1 MHz)		IRL	—	–12	–9	dB
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)		G_{ps}	—	11.7	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)		η	—	34	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)		IMD	—	–31	—	dB
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)		IRL	—	–14	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, CW, I_{DQ} = 2 × 500 mA, f1 = 1990.0 MHz)		P1dB	—	120	—	Watts
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 × 500 mA, f1 = 1990.0 MHz)		G_{ps}	—	11	—	dB

(1) Each side of device measured separately.
(2) Device measured in push–pull configuration.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture) (2) (continued)					
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 × 500 mA, f1 = 1990.0 MHz)	η	—	45	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 × 500 mA, f = 1990 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(2) Device measured in push–pull configuration.



B1, B2	Ferrite Beads, Fair Rite
C1, C2	0.6 – 4.5 pF Variable Capacitors, Johanson Gigatrim
C3, C4, C9, C10	10 pF Chip Capacitors, B Case, ATC
C5, C12	0.4 – 2.5 pF Variable Capacitors, Johanson Gigatrim
C6, C7	2.0 pF Chip Capacitors, B Case, ATC
C8	1.1 pF Chip Capacitor, B Case, ATC
C11	0.1 pF Chip Capacitor, B Case, ATC
C13, C20, C29, C37	5.1 pF Chip Capacitors, B Case, ATC
C14, C21, C28, C38	91 pF Chip Capacitors, B Case, ATC
C15, C22, C31, C40	100 μF, 50 V Electrolytic Capacitors, Sprague
C16, C23, C33, C43	0.039 μF Chip Capacitors, B Case, ATC
C17, C24, C32, C41	1000 pF Chip Capacitors, B Case, ATC
C19, C25	0.020 μF Chip Capacitors, B Case, ATC
C27, C34, C36, C42	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
C30, C39	1.0 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
C35, C44	470 μF, 63 V Electrolytic Capacitors, Sprague
Coax1, Coax2	25 Ω, Semi Rigid Coax, 70 mil OD, 1.05″ Long
Coax3, Coax4	50 Ω, Semi Rigid Coax, 85 mil OD, 1.05″ Long
L1	5.0 nH, Minispring Inductor, Coilcraft
L2	8.0 nH, Minispring Inductor, Coilcraft
L3, L4	5.60 nH, Microspring Inductors, Coilcraft
R1, R2	1 kΩ, 1/2 W Fixed Metal Film Resistors, Dale
R3, R4	270 Ω, 1/8 W Fixed Film Chip Resistors, Dale
R5, R6	1.0 kΩ, 1/8 W Fixed Film Chip Resistors, Dale
Z1	0.150″ x 0.080″ Microstrip
Z2	0.320″ x 0.080″ Microstrip
Z4, Z5	1.050″ x 0.080″ Microstrip
Z6, Z7	0.120″ x 0.080″ Microstrip
Z8, Z9	0.140″ x 0.080″ Microstrip
Z10, Z11	0.610″ x 0.080″ Microstrip
Z12, Z13	0.135″ x 0.080″ Microstrip
Z14, Z15	0.130″ x 0.080″ Microstrip
Z16, Z17	0.300″ x 0.350″ Microstrip
Z18, Z19	0.150″ x 0.500″ Microstrip
Z20, Z21	0.075″ x 0.500″ Microstrip
Z22, Z23	0.330″ x 0.500″ Microstrip
Z24, Z25	0.100″ x 0.550″ Microstrip
Z26, Z27	0.175″ x 0.550″ Microstrip
Z28, Z29	0.045″ x 0.550″ Microstrip
Z30, Z31	0.190″ x 0.325″ Microstrip
Z32, Z33	0.080″ x 0.325″ Microstrip
Z34, Z35	0.515″ x 0.080″ Microstrip
Z36, Z37	0.020″ x 0.080″ Microstrip
Z38, Z39	0.565″ x 0.080″ Microstrip
Z40	0.100″ x 0.080″ Microstrip
Z41	0.470″ x 0.080″ Microstrip
Z42	0.100″ x 0.080″ Microstrip
Board Material	0.03″ Teflon®, ε_r = 2.55 Copper Clad, 2 oz. Cu
Connectors	N–Type Panel Mount, Stripline

Figure 1. 1.93 – 1.99 GHz Broadband Test Circuit Schematic

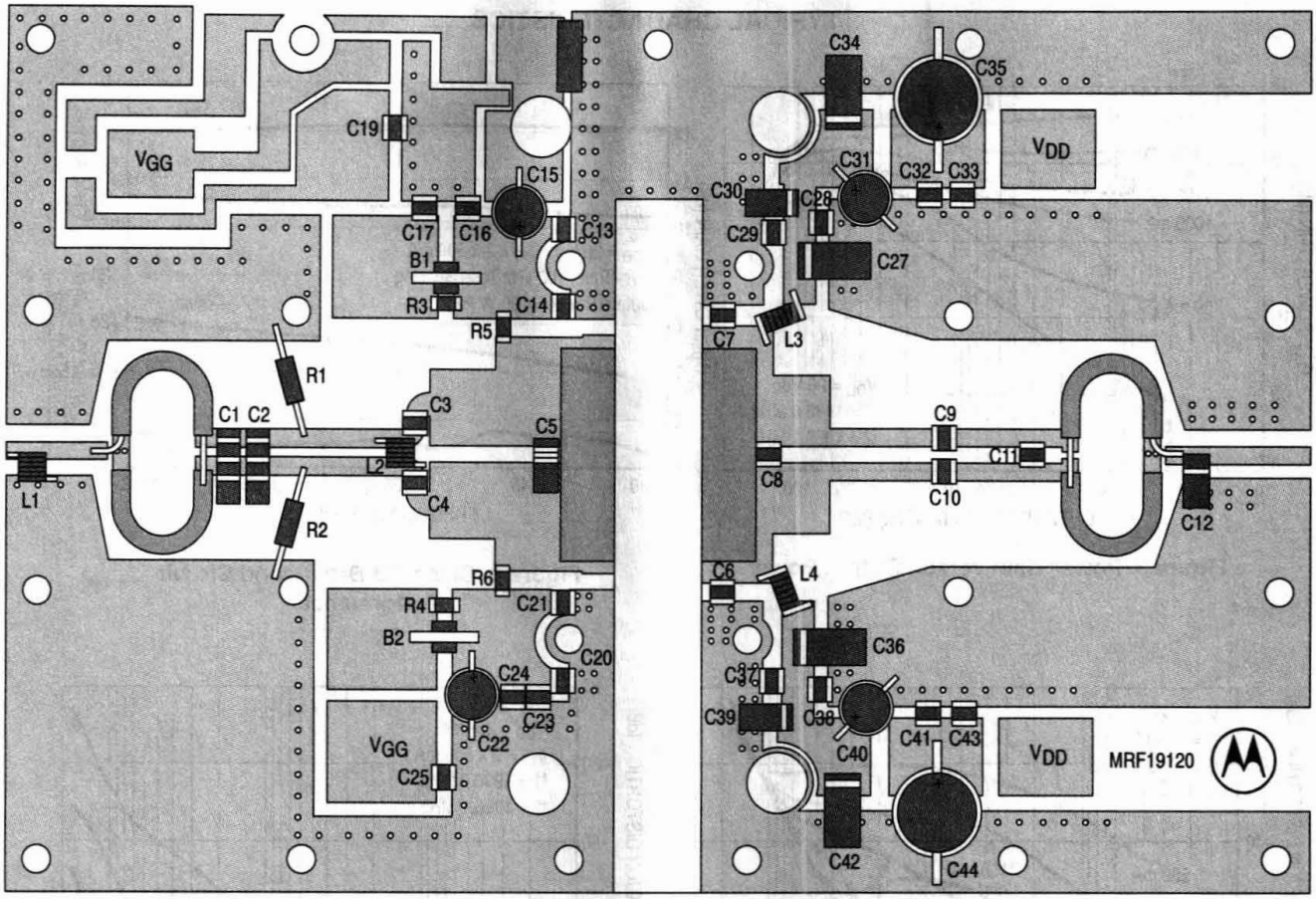


Figure 2. MRF19120 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

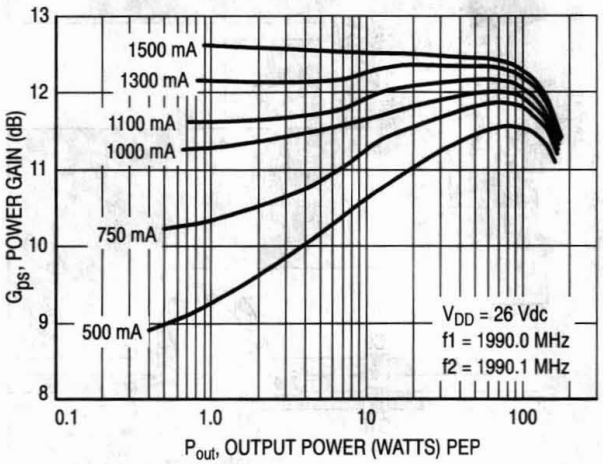


Figure 3. Power Gain versus Output Power

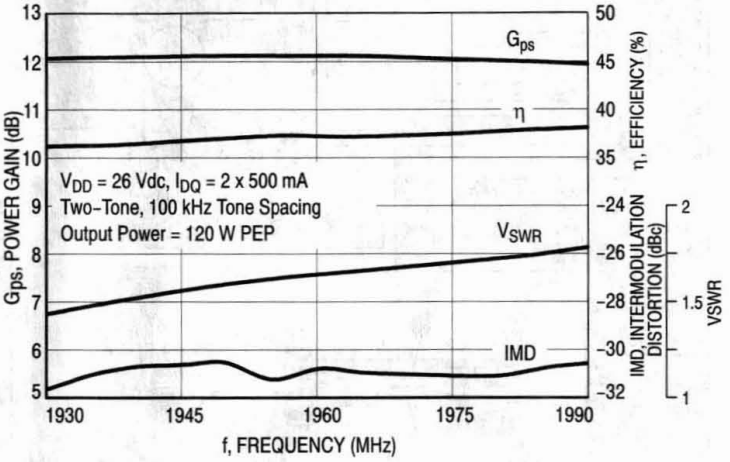


Figure 4. Class AB Broadband Circuit Performance

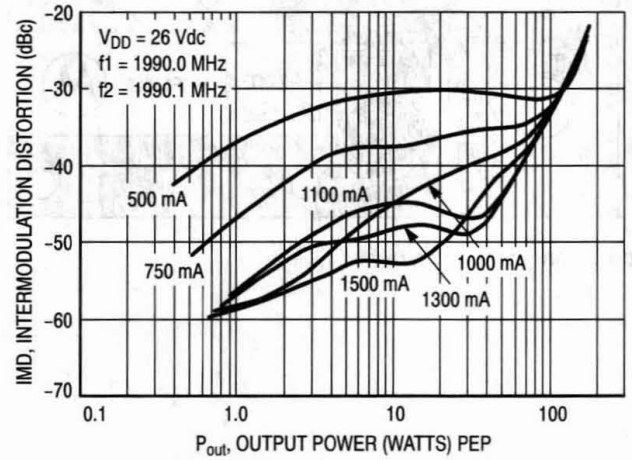


Figure 5. Intermodulation Distortion versus Output Power

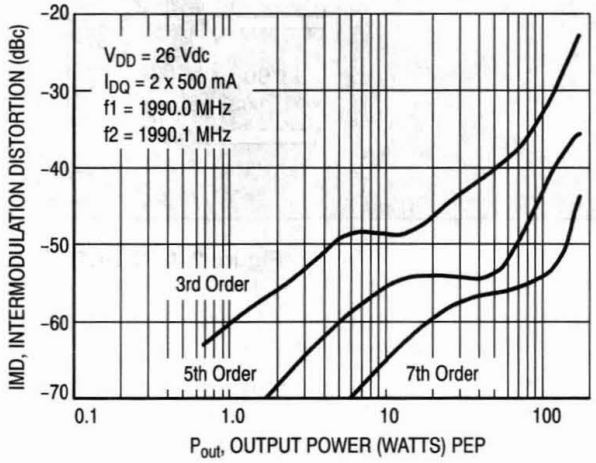


Figure 6. Intermodulation Distortion Products versus Output Power

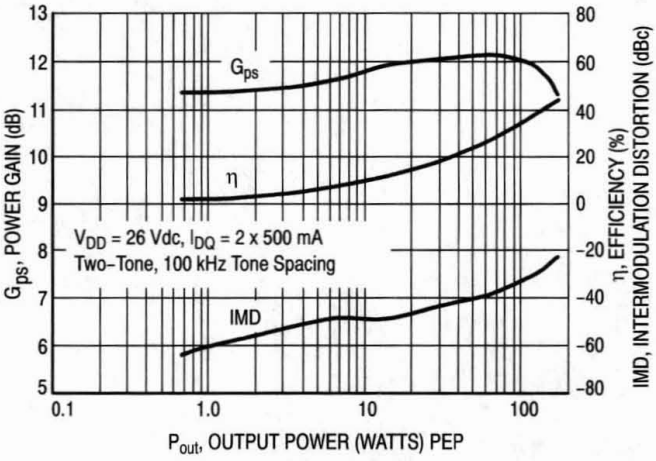


Figure 7. Power Gain, Efficiency, and IMD versus Output Power

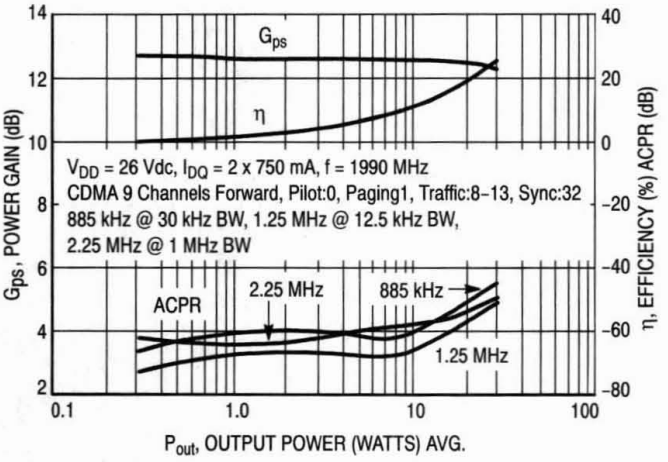
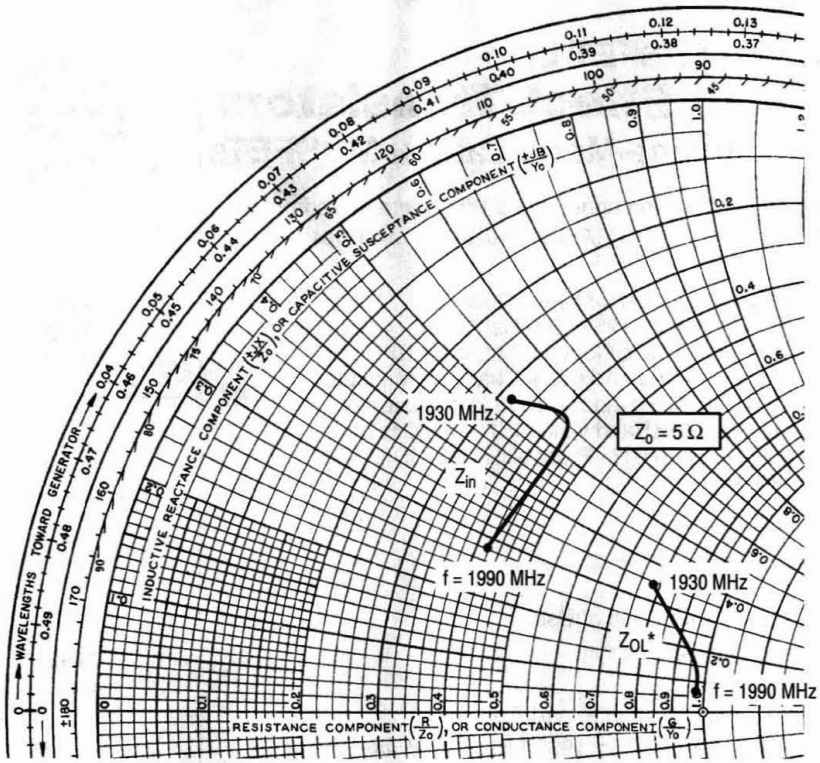


Figure 8. Power Gain, Efficiency, and ACPR versus Output Power



V_{DD} = 26 V, I_{DQ} = 2 × 500 mA, P_{out} = 120 Watts PEP

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1930	1.64 + j2.6	3.9 + j1.7
1960	2.10 + j2.8	4.8 + j0.8
1990	2.10 + j1.4	4.9 + j0.3

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

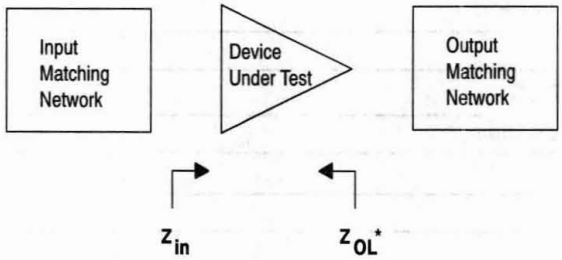


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

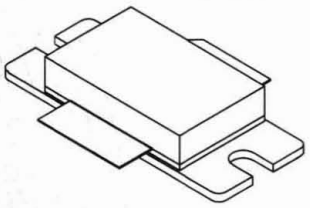
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19125
MRF19125S
MRF19125SR3

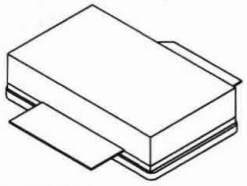
1990 MHz, 125 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

- Typical 2–Carrier N–CDMA Performance for V_{DD} = 26 Volts, I_{DQ} = 1300 mA, f1 = 1958.75 MHz, f2 = 1961.25 MHz
  IS–95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13)
  1.2288 MHz Channel Bandwidth Carrier. Adjacent Channels Measured over a 30 kHz Bandwidth at f1 –885 kHz and f2 +885 kHz. Distortion Products Measured over 1.2288 MHz Bandwidth at f1 –2.5 MHz and f2 +2.5 MHz. Peak/Avg. = 9.8 dB @ 0.01% Probability on CCDF.
  Output Power — 24 Watts Avg.
  Power Gain — 13.6 dB
  Efficiency — 22%
  ACPR — –51 dB
  IM3 — –37.0 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1990 MHz, 125 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465B–03, STYLE 1
(NI–880)
(MRF19125)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF19125S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	330 1.89	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.53	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

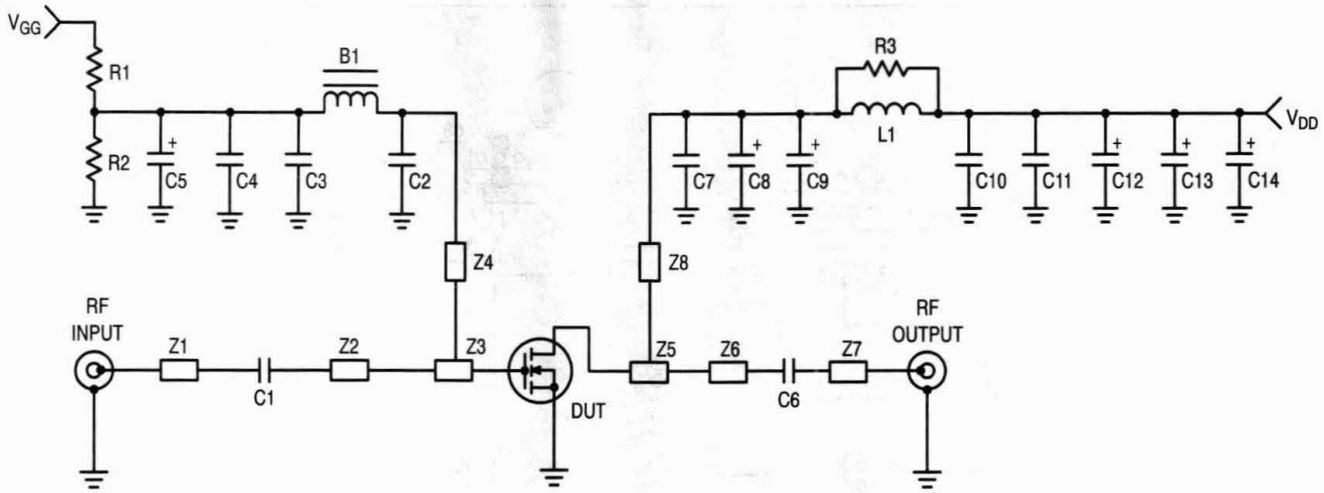
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	9	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 1300 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	—	0.185	0.21	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	5.4	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) 2–Carrier N–CDMA, 1.2288 MHz Channel Bandwidth Carriers. Peak/Avg = 9.8 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	G_{ps}	12	13.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	η	19	22	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; IM3 measured over 1.2288 MHz Bandwidth at f1 –2.5 MHz and f2 +2.5 MHz)	IMD	—	–37	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; ACPR measured over 30 kHz Bandwidth at f1 –885 MHz and f2 +885 MHz)	ACPR	—	–51	–47	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 24 W Avg, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 125 W CW, I_{DQ} = 1300 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	—	13.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1990 MHz, Tone Spacing = 100 kHz)	η	—	35	—	%
Third Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1300 mA, f1 = 1930 MHz, f2 = 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–13	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 1300 mA, f = 1990 MHz)	P1dB	—	130	—	W



Z1, Z7	0.500″ x 0.084″ Microstrip	Board	0.030″ Glass Teflon®, Keene GX–0300–55–22, ε_r = 2.55
Z2	1.105″ x 0.084″ Microstrip		
Z3	0.360″ x 0.895″ Microstrip	PCB	Etched Circuit Boards MRF19125 Rev. 5, CMR
Z4	0.920″ x 0.048″ Microstrip		
Z5	0.605″ x 1.195″ Microstrip		
Z6	0.800″ x 0.084″ Microstrip		
Z8	0.660″ x 0.095″ Microstrip		

Figure 1. MRF19125 Test Circuit Schematic

Table 1. MRF19125 Test Circuit Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite #2743019447
C1	51 pF Chip Capacitor, ATC #100B510JCA500X
C2, C7	5.1 pF Chip Capacitors, ATC #100B5R1JCA500X
C3, C10	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C11	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C5	0.1 μF Tantalum Chip Capacitor, Kemet #T491C105M050
C6	10 pF Chip Capacitor, ATC #100B100JCA500X
C8	10 μF Tantalum Chip Capacitor, Kemet #T491X106K035AS4394
C9, C12, C13, C14	22 μF Tantalum Chip Capacitors, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100″ ID, Motorola
N1, N2	Type N Flange Mounts, Omni Spectra #3052–1648–10
R1	1.0 kΩ, 1/8 W Chip Resistor
R2	220 kΩ, 1/8 W Chip Resistor
R3	10 Ω, 1/8 W Chip Resistor

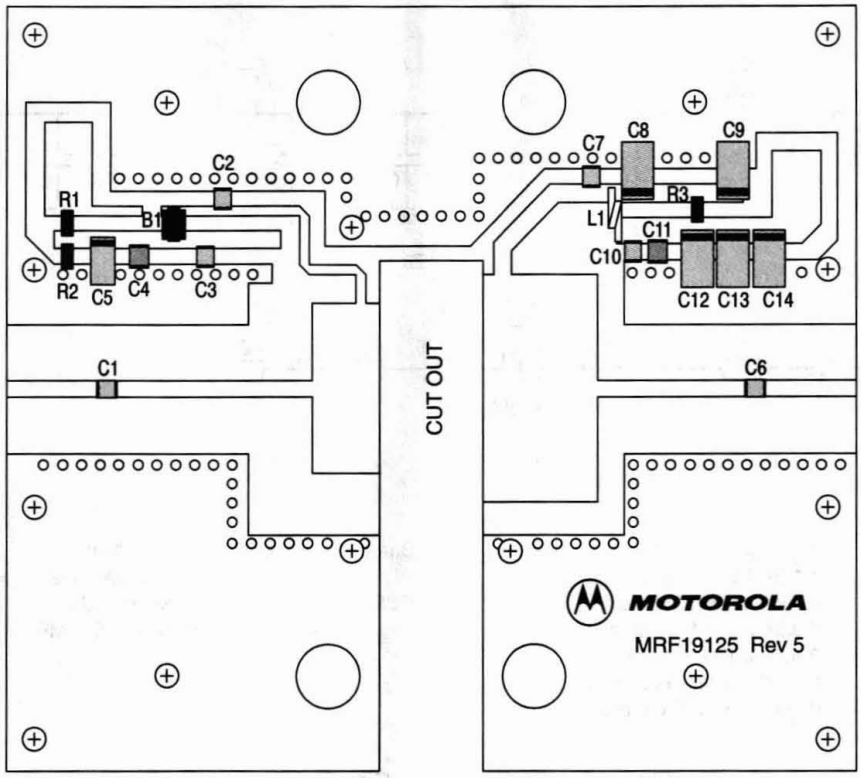


Figure 2. MRF19125 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

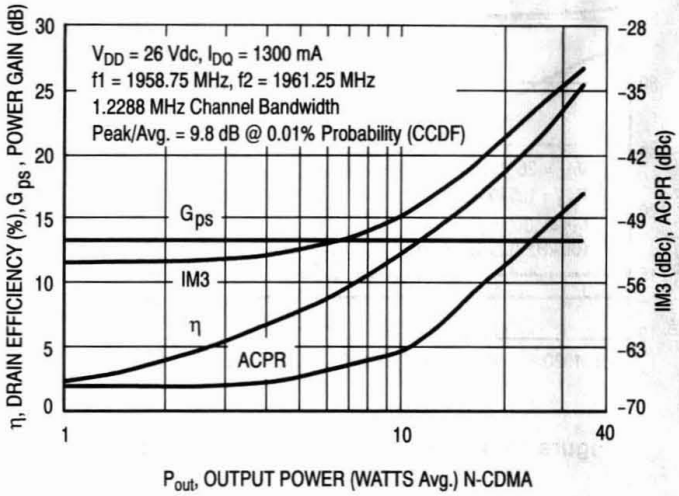


Figure 3. 2-Carrier CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

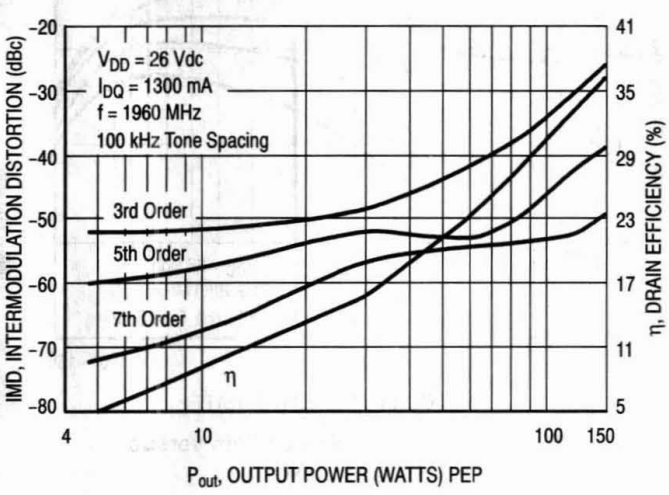


Figure 4. Intermodulation Distortion Products versus Output Power

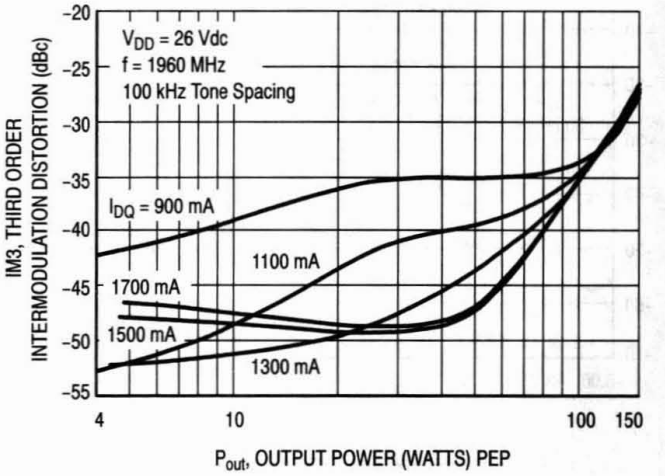


Figure 5. Third Order Intermodulation Distortion versus Output Power

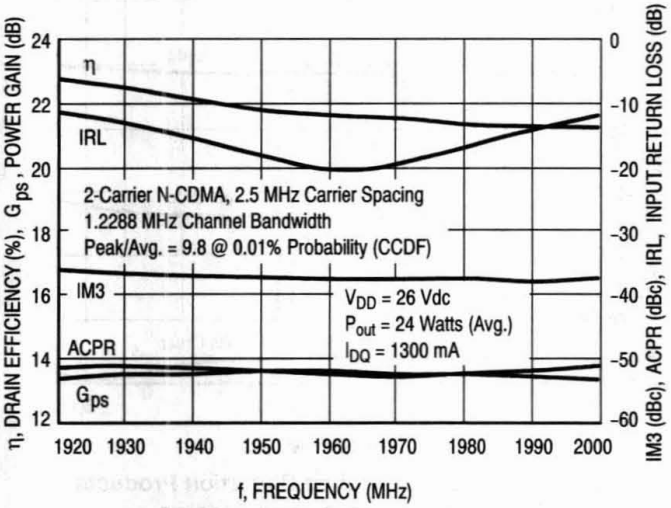


Figure 6. 2-Carrier N-CDMA Broadband Performance

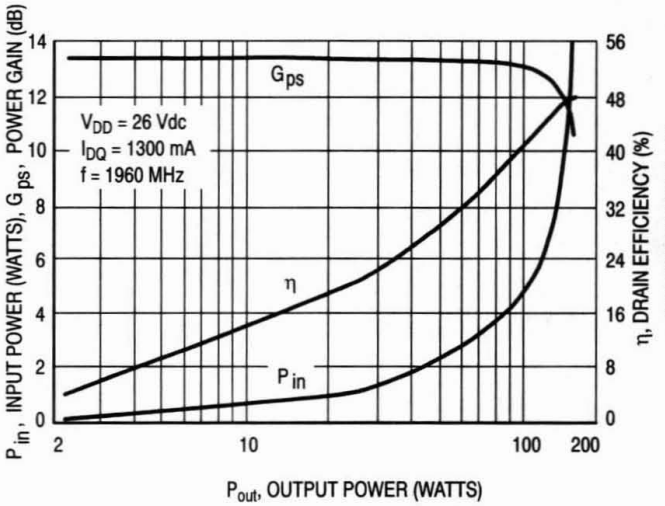


Figure 7. CW Performance

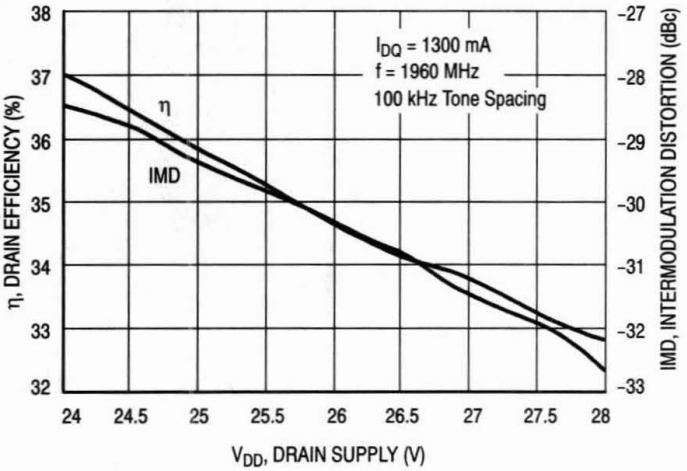


Figure 8. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

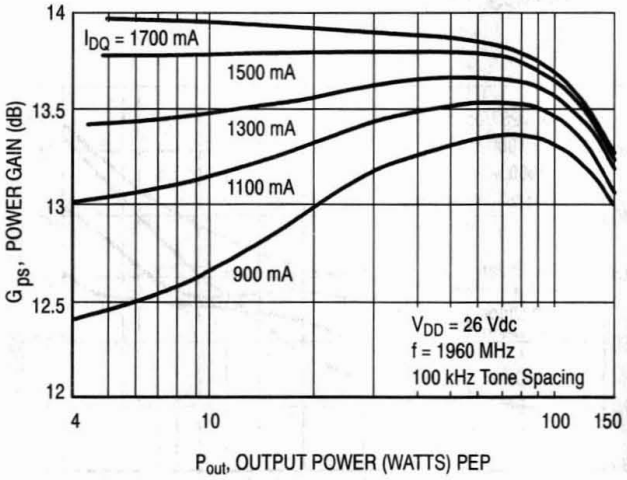


Figure 9. Two-Tone Power Gain versus Output Power

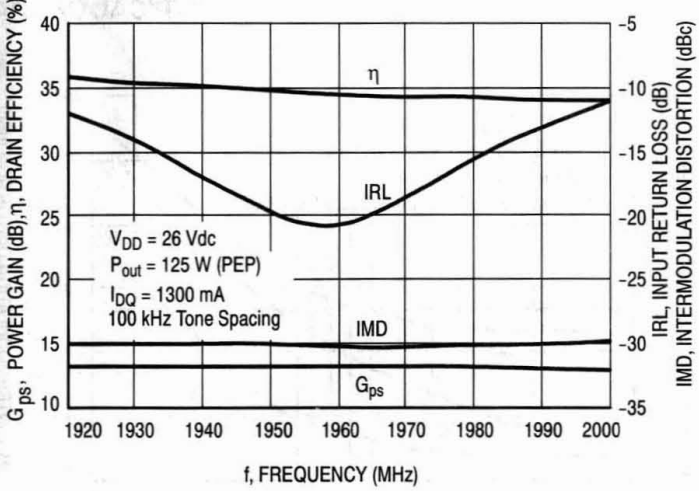


Figure 10. Two-Tone Broadband Performance

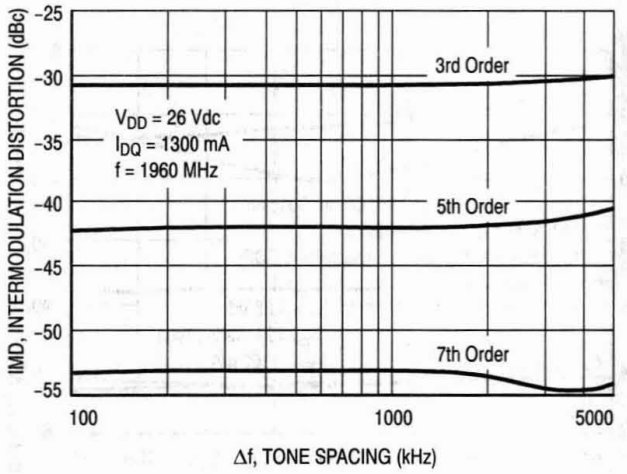


Figure 11. Intermodulation Distortion Products versus Two–Tone Tone Spacing

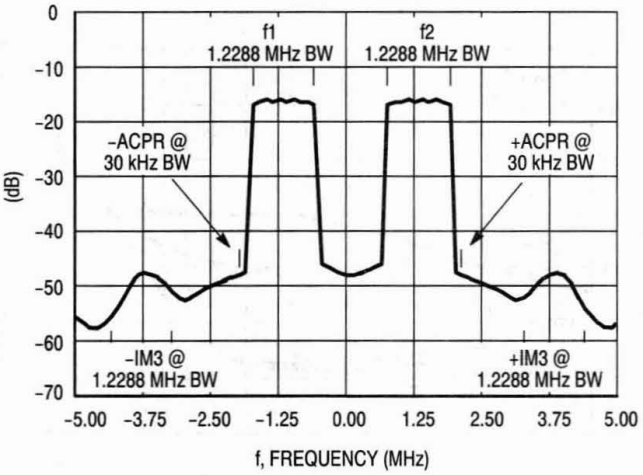
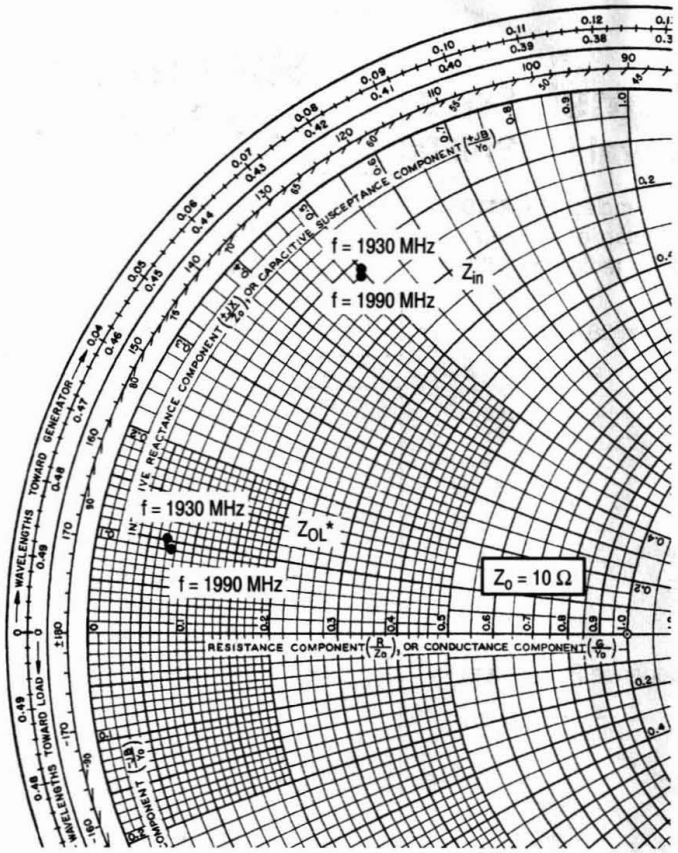


Figure 12. 2-Carrier N-CDMA Spectrum



V_{DD} = 26 V, I_{DQ} = 1300 mA, P_{out} = 24 W (Avg.)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	1.43 + j5.01	0.75 + j0.93
1960	1.51 + j4.88	0.71 + j0.89
1990	1.56 + j4.93	0.68 + j1.02

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

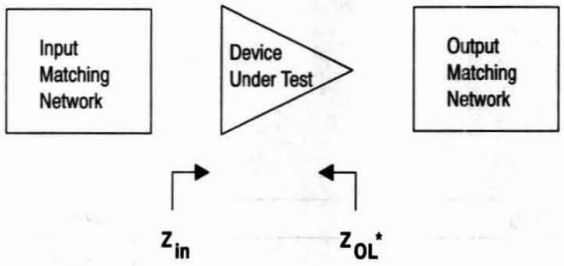


Figure 13. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

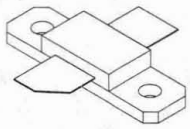
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21010
MRF21010S

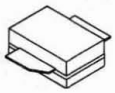
2170 MHz, 10 W, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Typical W–CDMA Performance: –45 dBc ACPR, 2140 MHz, 28 Volts, 5 MHz Offset/4.096 MHz BW, 15 DTCH
  - Output Power — 2.1 Watts
  - Power Gain — 13.5 dB
  - Efficiency — 21%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR @ 28 Vdc, 2170 MHz, 10 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 360B–05, STYLE 1
(NI–360)
(MRF21010)



CASE 360C–05, STYLE 1
(NI–360S)
(MRF21010S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, – 0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	43.75 0.25	W W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

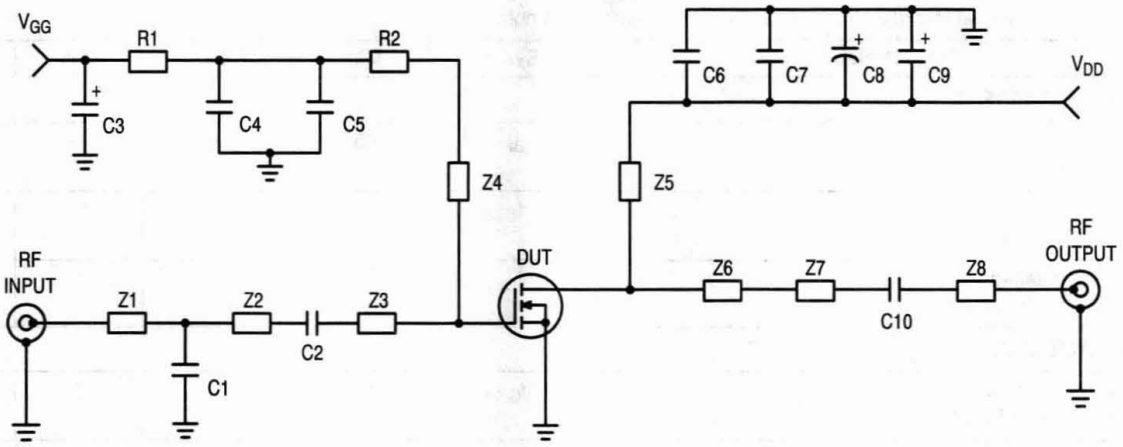
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.5	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D =10 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 μA)	$V_{GS(th)}$	2.5	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 100 mA)	$V_{GS(Q)}$	2.5	4	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 0.5 A)	$V_{DS(on)}$	—	0.4	0.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	g_{fs}	—	0.95	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 10 W PEP, I_{DQ} = 100 mA, f1 = 2110 MHz, f2 = 2170 MHz, Tone Spacing = 100 KHz)	G_{ps}	12	13.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 10 W PEP, I_{DQ} = 100 mA, f1 = 2110 MHz, f2 = 2170 MHz, Tone Spacing = 100 KHz)	η	31	35	—	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 10 W PEP, I_{DQ} = 100 mA, f1 = 2110 MHz, f2 = 2170 MHz, Tone Spacing = 100 KHz)	IMD	—	–35	–30	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 10 W PEP, I_{DQ} = 100 mA, f1 = 2110 MHz, f2 = 2170 MHz, Tone Spacing = 100 KHz)	IRL	—	–12	–10	dB
Output Power, 1 dB Compression Point, CW (V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 2170 MHz)	P1dB	—	11	—	W
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 10 W CW, I_{DQ} = 100 mA, f = 2170 MHz)	G_{ps}	—	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 10 W CW, I_{DQ} = 100 mA, f = 2170 MHz)	η	—	42	—	%
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 10 W CW, I_{DQ} = 100 mA, f = 2170 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			



Z1	0.964″ x 0.087″ Microstrip	Z5	0.752″ x 0.087″ Microstrip
Z2	0.905″ x 0.087″ Microstrip	Z6	0.453″ x 1.118″ Microstrip
Z3	0.433″ x 0.512″ Microstrip	Z7	0.921″ x 0.154″ Microstrip
Z4	1.068″ x 0.087″ Microstrip	Z8	0.925″ x 0.087″ Microstrip

Figure 1. MRF21010 Test Circuit Schematic

Table 1. MRF21010 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1 * (eared)	2.2 pF Chip Capacitor, B Case	100B2R2BW	ATC
(earless)	1.8 pF Chip Capacitor, B Case	100B1R8BW	ATC
C2	0.5 pF Chip Capacitor, B Case	100B0R5BW	ATC
C3, C9	10 μF, 35 V Tantalum Chip Capacitors	293D106X9035D2T	Sprague–Vishay
C4, C7	1 nF Chip Capacitors, B Case	100B102JW	ATC
C5, C6	5.6 pF Chip Capacitors, B Case	100B5R6BW	ATC
C8	470 μF, 63 V Electrolytic Capacitor		
C10	10 pF Chip Capacitor, B Case	100B100GW	ATC
N1, N2	Type N Connector Flange Mounts	3052–1648–10	Macom
R1	1.0 kΩ Chip Resistor (0805)		
R2	12 Ω Chip Resistor (0805)		
PCB	Etched Circuit Board	C–XM–00–001–01	Cibel
Raw PCB material	0.030" Glass Teflon® (ε_r = 2.55)	TLX8–0300	Taconic

* Piece part depending on eared / earless version of the device.

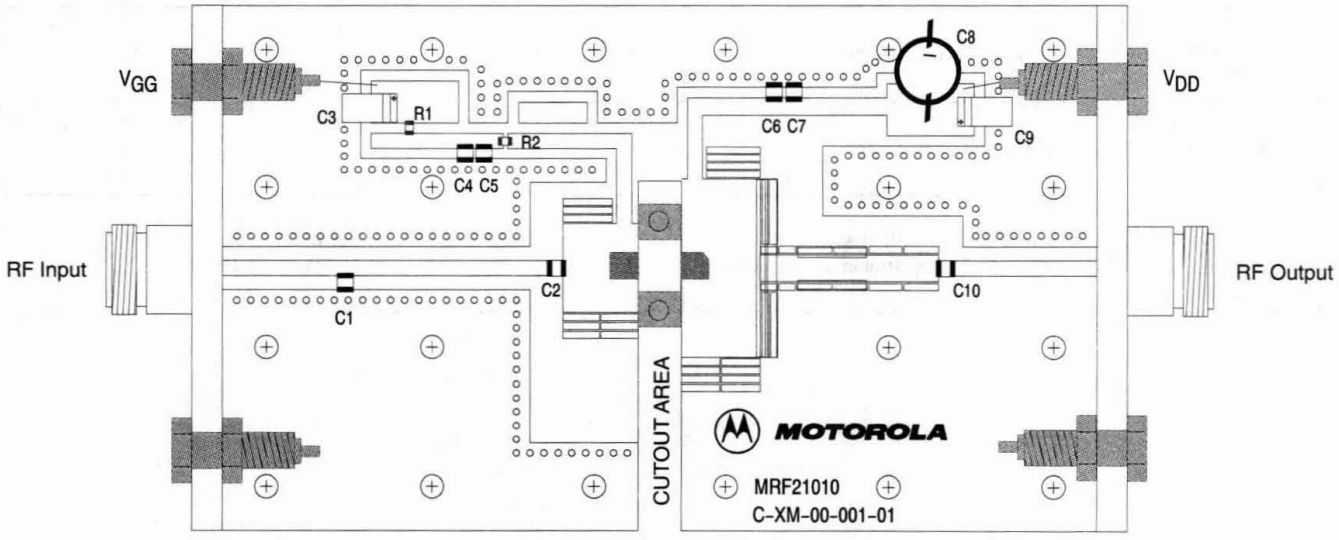


Figure 2. MRF21010 Test Circuit Component Layout

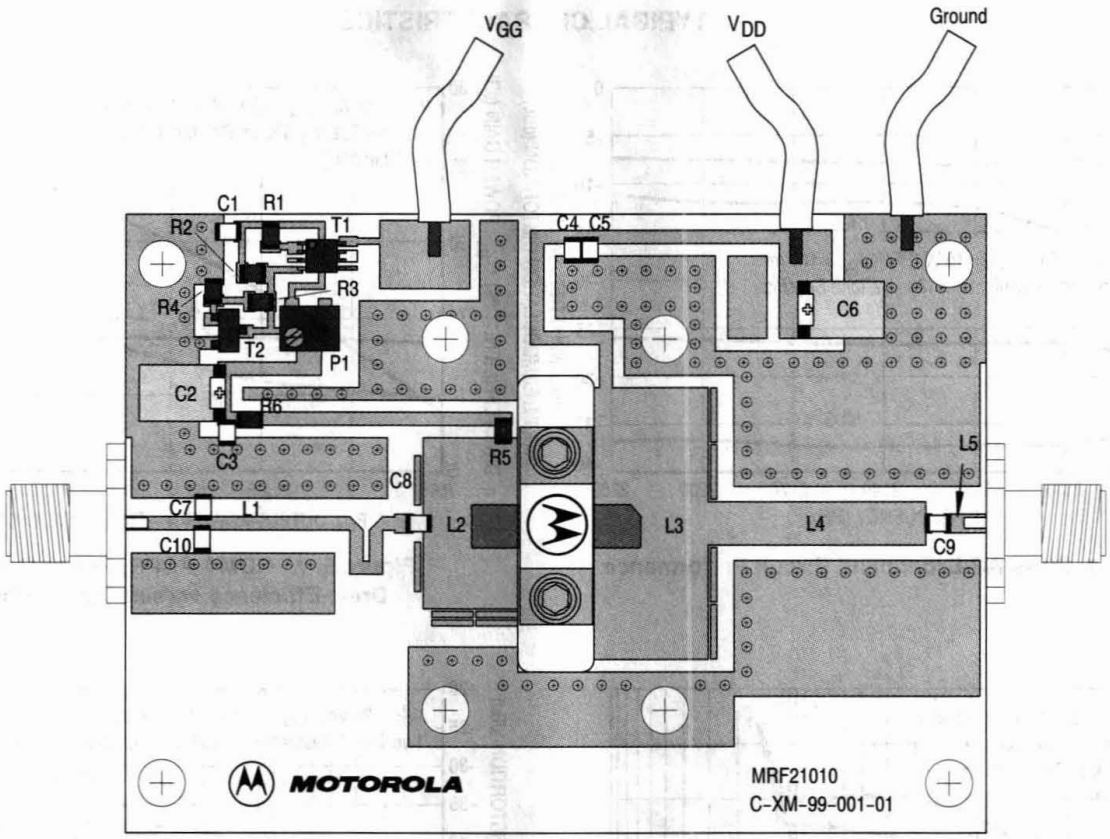


Figure 3. MRF21010 Demonstration Board Component Layout

Table 2. MRF21010 Demonstration Board Component Designations and Values

Designators	Description
C1	1 μF Chip Capacitor (0805), AVX #08053G105ZATEA
C2, C6	10 μF, 35 V Tantalum Capacitors, Vishay–Sprague #293D106X9035D
C3, C4	6.8 pF Chip Capacitors, ACCU–P (0805), AVX #08051J6R8CBT
C5	10 nF Chip Capacitor (0805), AVX #08055C103KATDA
C7	1.5 pF Chip Capacitor, ACCU–P (0805), AVX #08051J2R2BBT
C8, C10	0.5 pF Chip Capacitors, ACCU–P (0805), AVX #08051J0R5BBT
C9	10 pF Chip Capacitor, ACCU–P (0805), AVX #08055J100GBT
L1	19 mm × 1.07 mm
L2	7.7 mm × 13.8 mm
L3	9.3 mm × 22 mm
L4	17.7 mm × 3.5 mm
L5	3.4 mm × 1.5 mm
R1, R6	10 Ω, 1/8 W Chip Resistors (0805)
R2, R3	1 kΩ, 1/8 W Chip Resistors (0805)
R4	2.2 kΩ, 1/8 W Chip Resistor (0805)
R5	0 Ω, 1/8 W Chip Resistor (0805)
P1	5 kΩ Potentiometer CMS Cermet Multi–Turn, Bourns #3224W
T1	Voltage Regulator, Micro–8, Motorola #LP2951
T2	Bipolar NPN Transistor, SOT–23, Motorola #BC847
	RF Connectors Type SMA, Johnson #142–0701–631
	Substrate: Rogers RO4350, Thickness 0.5 mm, ε_r = 3.53

TYPICAL CHARACTERISTICS

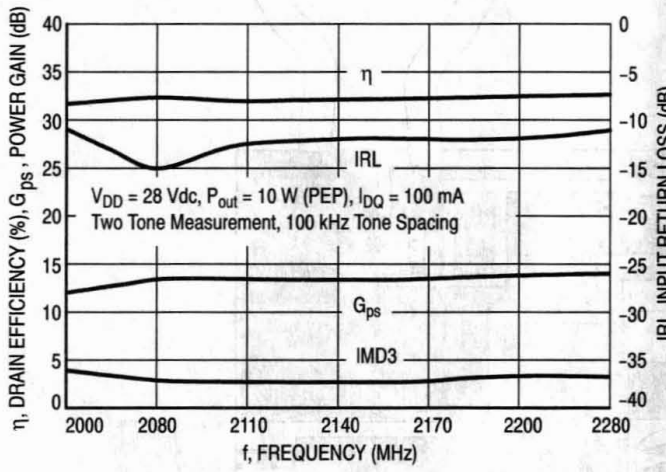


Figure 4. Class AB Broadband Circuit Performance

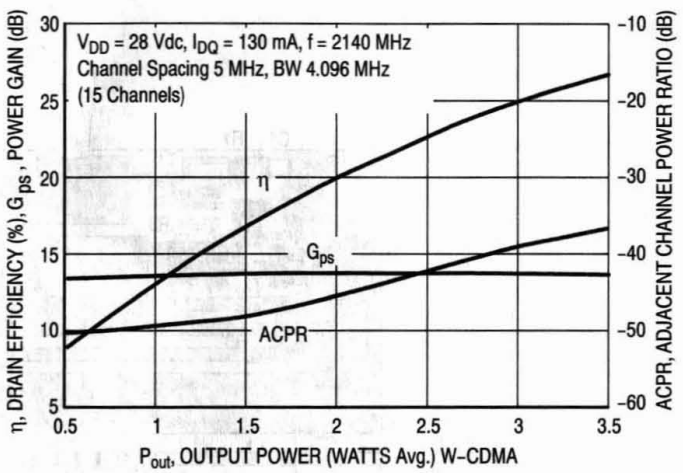


Figure 5. W–CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

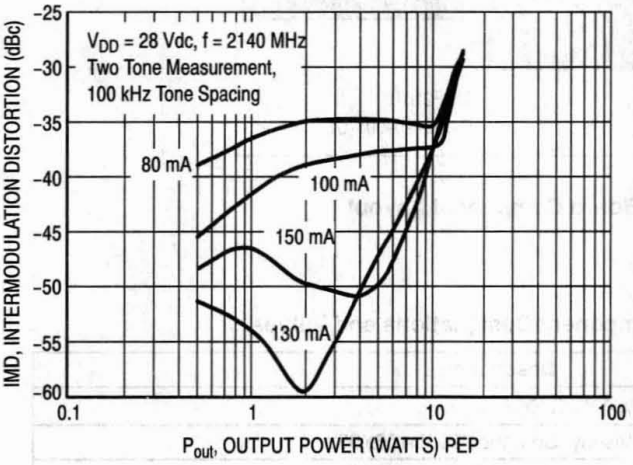


Figure 6. Intermodulation Distortion versus Output Power

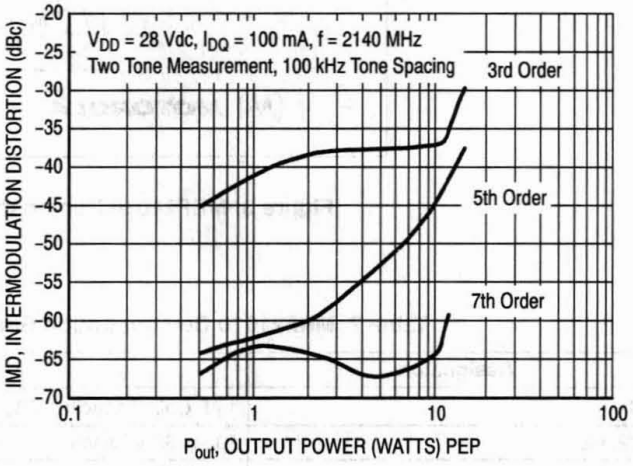


Figure 7. Intermodulation Distortion Products versus Output Power

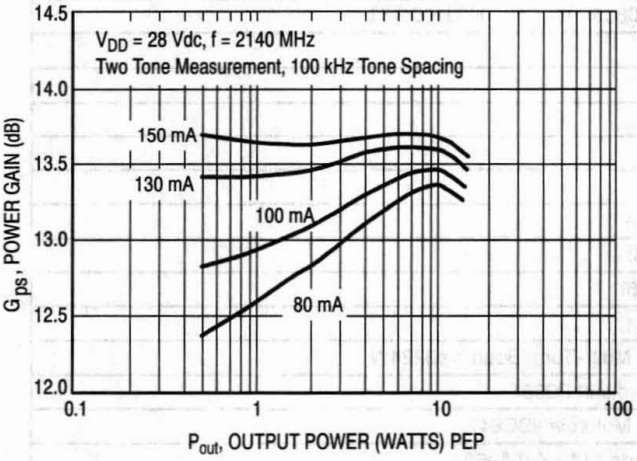


Figure 8. Power Gain versus Output Power

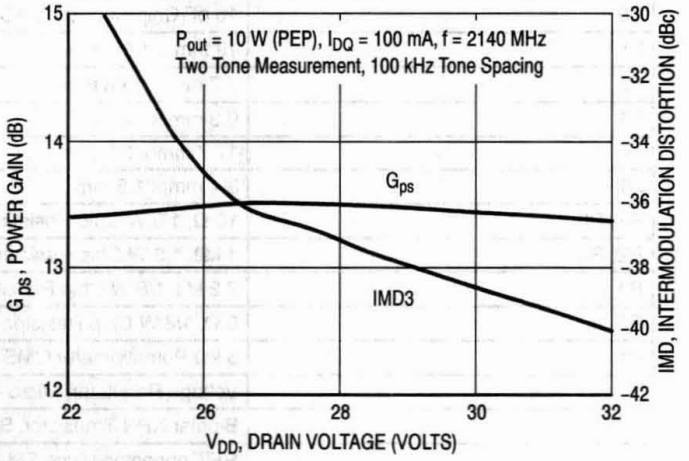
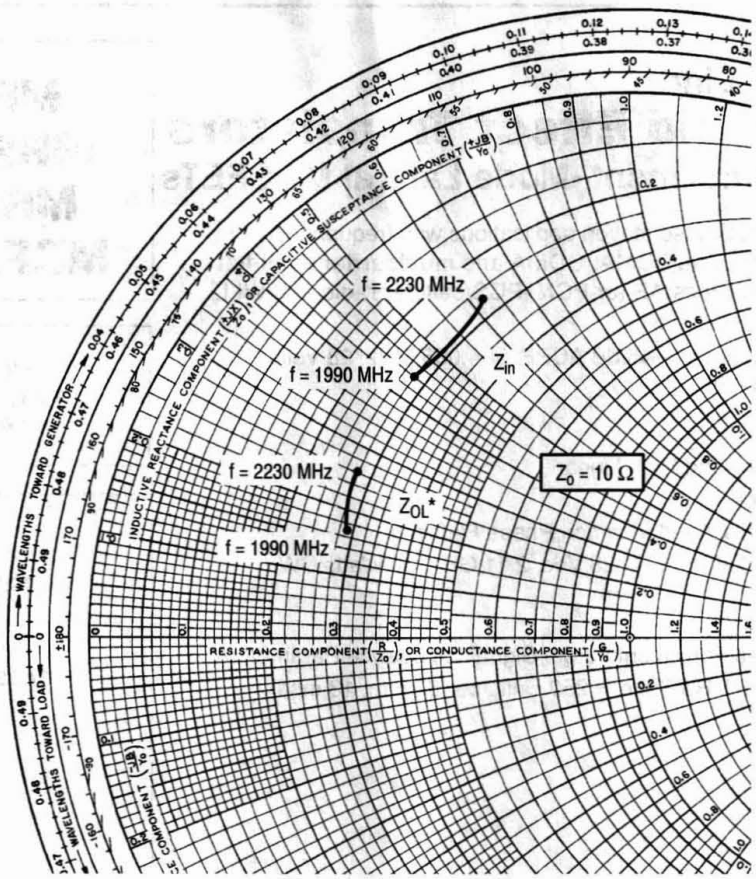


Figure 9. Intermodulation and Gain versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 100 mA, P_{out} = P1dB (CW)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1990	2.85 + j4.38	2.93 + j1.71
2110	2.89 + j5.04	2.76 + j2.28
2230	2.73 + j6.19	2.83 + j2.59

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

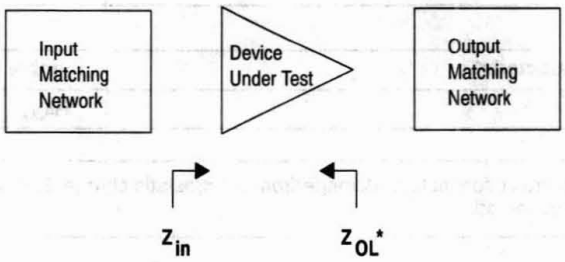


Figure 10. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

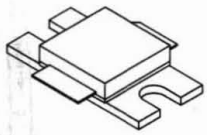
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21030
MRF21030R3
MRF21030S
MRF21030SR3

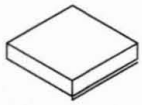
2.2 GHz, 30 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 2.0 to 2.2 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Wideband CDMA Performance: –45 dB ACPR @ 4.096 MHz, 28 Volts
  Output Power — 3.5 Watts
  Power Gain — 14 dB
  Efficiency — 15%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.



CASE 465E–03, STYLE 1
(NI–400)
(MRF21030)



CASE 465F–03, STYLE 1
(NI–400S)
(MRF21030S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83.3 0.48	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

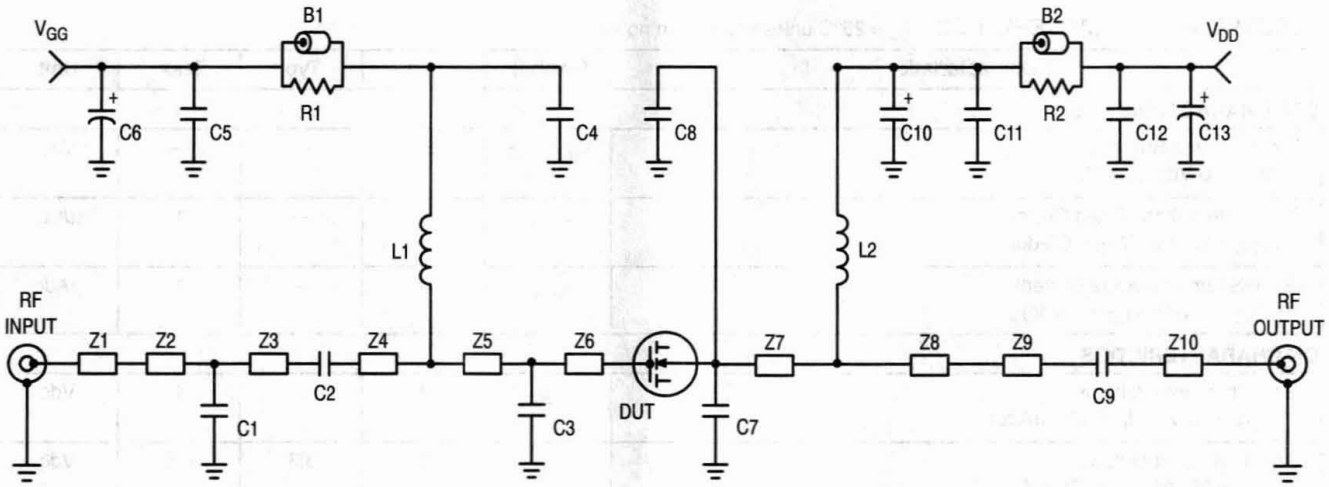
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 250 mA)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	98.5	—	pF
Output Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)	η	—	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)	IMD	—	–30	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)	IRL	—	–13	—	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	G_{ps}	12	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	η	31	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IMD	—	–30	–27.5	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 30 W CW, I_{DQ} = 250 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1, B2	Short Ferrite Beads	Z1	0.153″ x 0.087″ Microstrip
C1	1 pF Chip Capacitor	Z2	0.509″ x 0.156″ Microstrip
C2	4.7 pF Chip Capacitor	Z3	0.572″ x 0.087″ Microstrip
C3	0.5 pF Chip Capacitor	Z4	0.509″ x 0.232″ Microstrip
C4	3.9 pF Chip Capacitor	Z5	0.277″ x 0.143″ Microstrip
C5, C12	0.1 μF Chip Capacitors	Z6	0.200″ x 0.305″ Microstrip
C6, C13	470 μF, 63 V Electrolytic Chip Capacitors	Z7	0.200″ x 0.511″ Microstrip
C7, C8	0.3 pF Chip Capacitors	Z8	0.510″ x 0.328″ Microstrip
C9	3.6 pF Chip Capacitor	Z9	0.608″ x 0.081″ Microstrip
C10	22 μF Tantalum Chip Capacitor	Board	0.030″ Glass Teflon®, TLX8-0300
C11	5.1 pF Chip Capacitor		Taconix (ε_r = 2.55)
L1, L2	12.5 nH Inductors		
R1, R2	12 Ω Chip Resistors (1206)		

Figure 1. MRF21030 Test Circuit Schematic

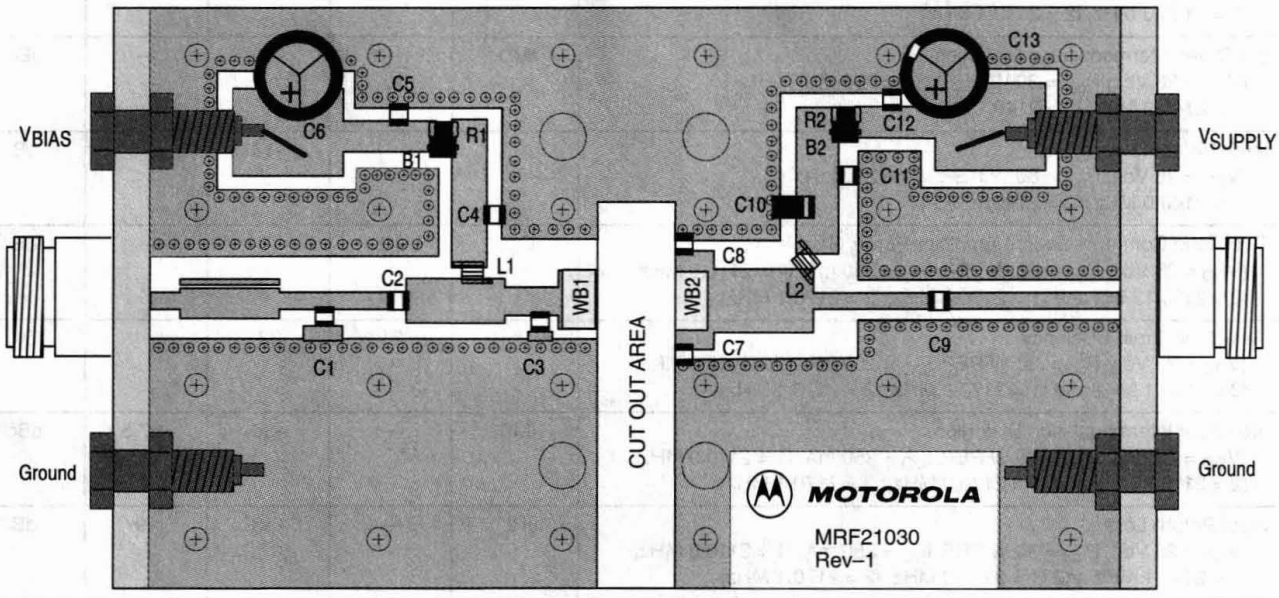


Figure 2. MRF21030 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

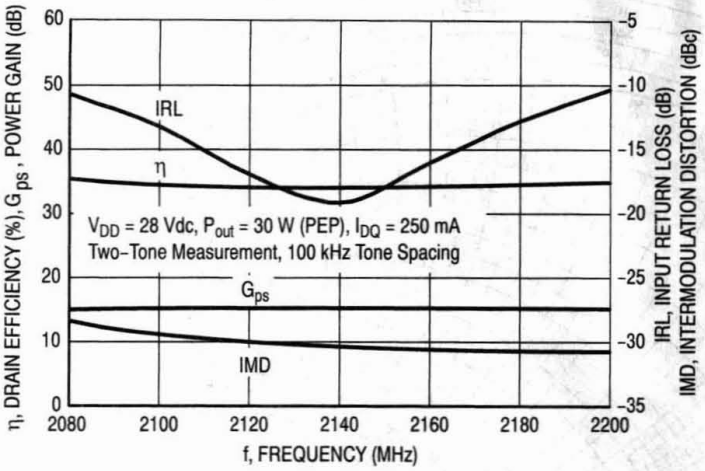


Figure 3. Class AB Broadband Circuit Performance

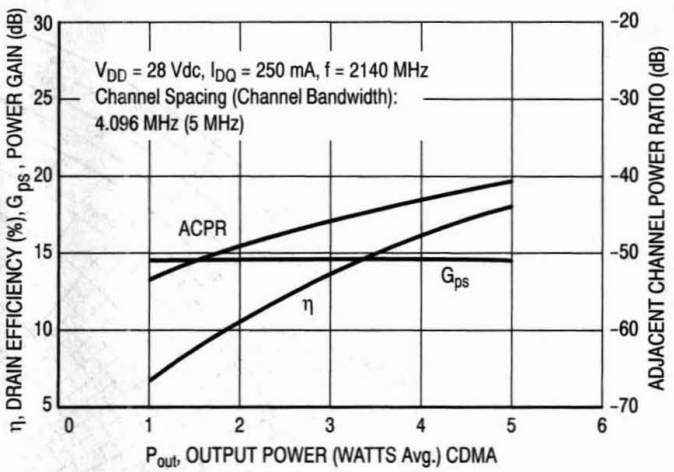


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

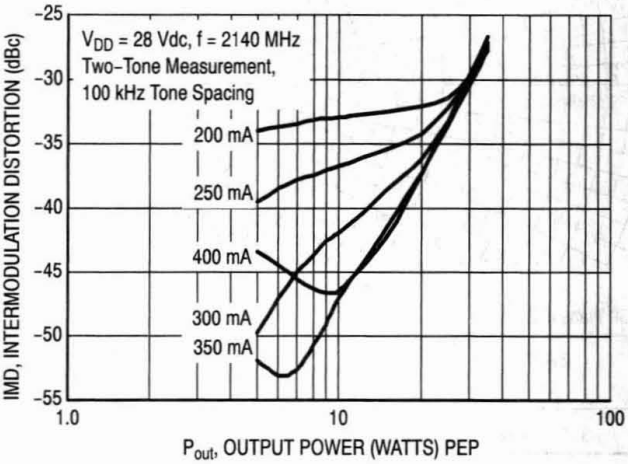


Figure 5. Intermodulation Distortion versus Output Power

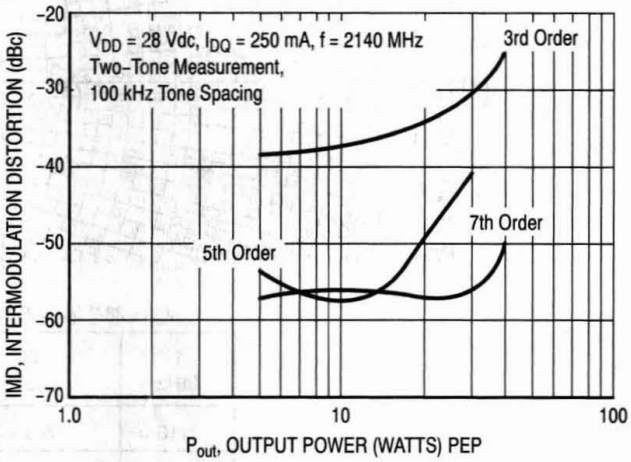


Figure 6. Intermodulation Distortion Products versus Output Power

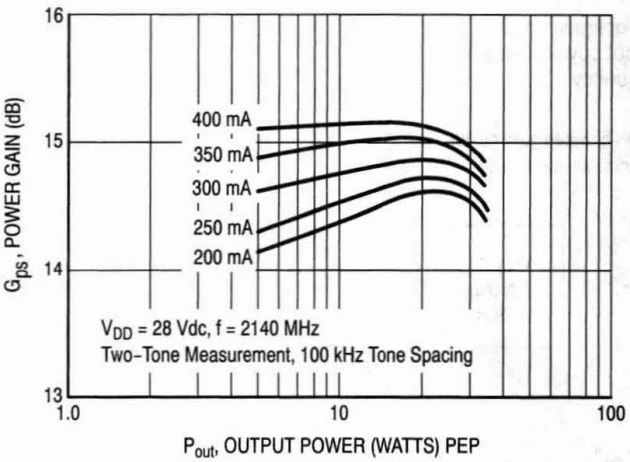


Figure 7. Power Gain versus Output Power

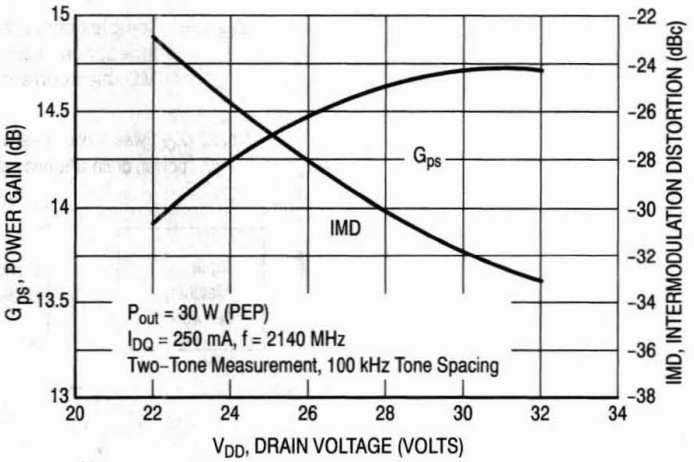
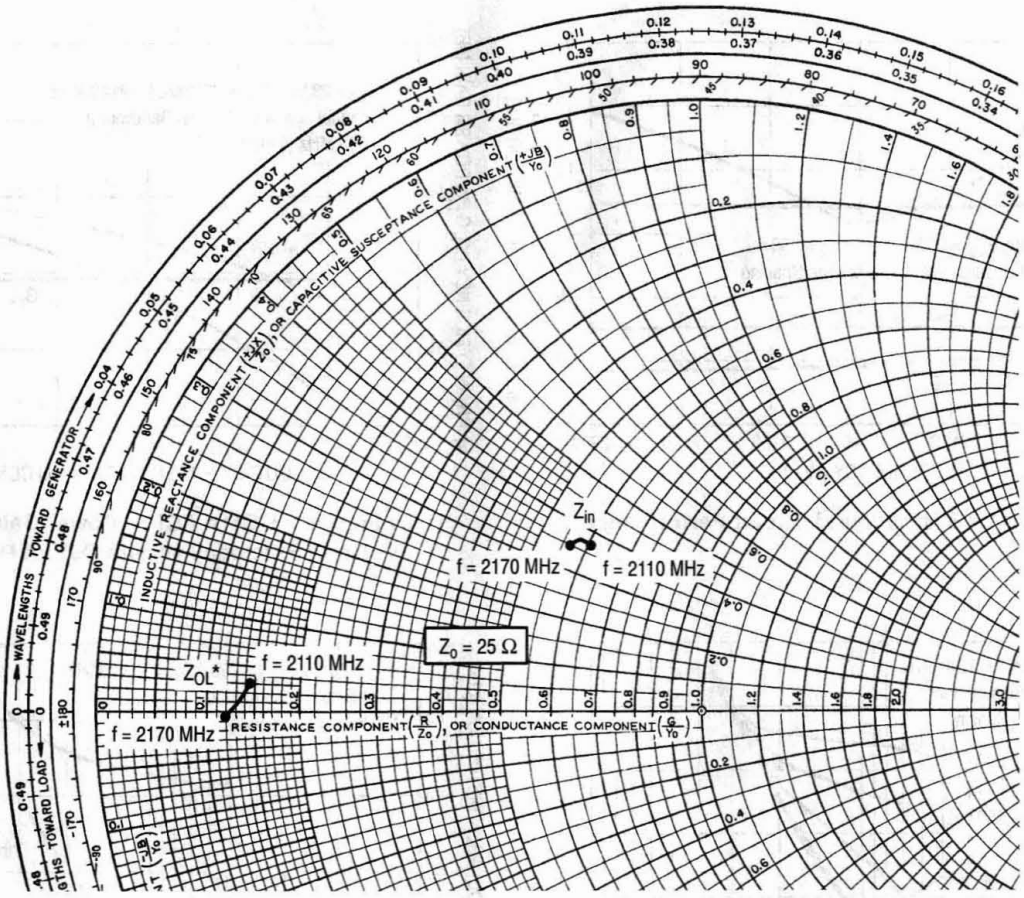


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 250 mA, P_{out} = 30 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	15.3 + j9.4	3.7 + j0.78
2140	14.6 + j9.4	3.4 + j0.37
2170	14.3 + j8.8	3.0 – j0.13

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

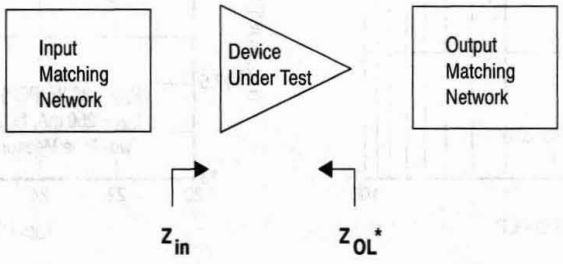


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

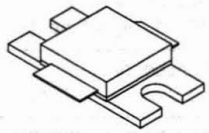
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21045
MRF21045R3
MRF21045S
MRF21045SR3

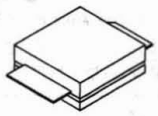
2170 MHz, 45 W, 28 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Typical 2–carrier W–CDMA Performance for V_{DD} = 28 Volts, I_{DQ} = 500 mA, f1 = 2135 MHz, f2 = 2145 MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels measured over 3.84 MHz Bandwidth at f1 –5 MHz and f2 +5 MHz, Distortion Products measured over a 3.84 MHz Bandwidth at f1 –10 MHz and f2 +10 MHz, Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
  Output Power — 10 Watts Avg.
  Efficiency — 23.5%
  Gain — 15 dB
  IM3 — –37.5 dBc
  ACPR — –41 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.



CASE 465E–03, STYLE 1
(NI–400)
(MRF21045)



CASE 465F–03, STYLE 1
(NI–400S)
(MRF21045S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	105 0.60	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

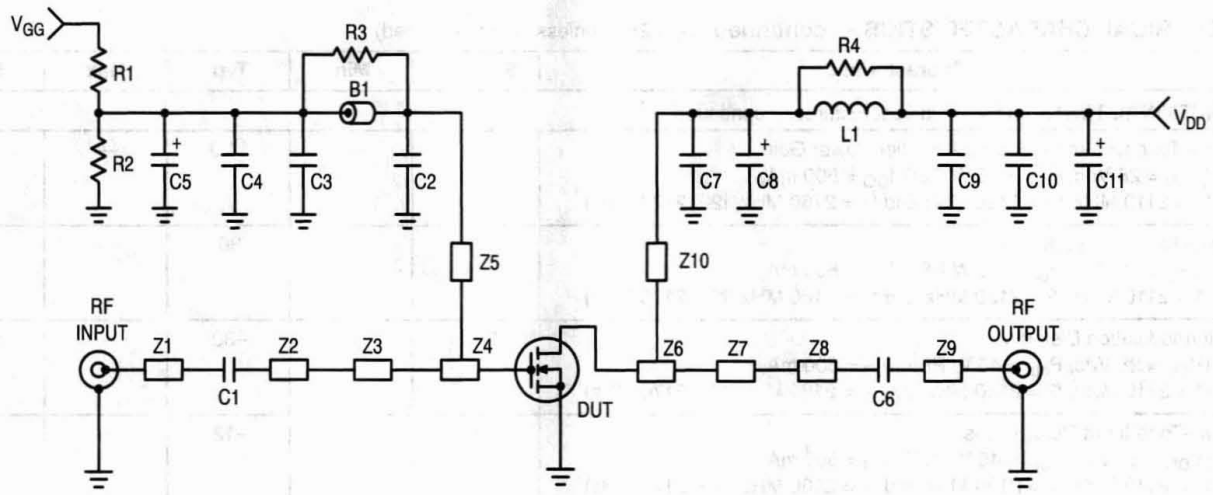
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (DC)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	3	3.9	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.19	0.21	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	3	—	S
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) 2–carrier W–CDMA. Peak/Avg. ratio = 8.3 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	G_{ps}	13.5	15	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	η	21	23.5	—	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; IM3 measured over 3.84 MHz Bandwidth at f1 –10 MHz and f2 +10 MHz.)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; ACPR measured over 3.84 MHz Bandwidth at f1 –5 MHz and f2 +5 MHz.)	ACPR	—	–41	–38	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 45 W CW, I_{DQ} = 500 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture) — continued					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	G_{ps}	—	14.9	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	η	—	36	—	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IMD	—	–30	—	dBc
Two–Tone Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f = 2170 MHz)	P1dB	—	50	—	W



Z1, Z9	0.750″ x 0.084″ Transmission Line	Board	0.030″ Glass Teflon®,
Z2	0.160″ x 0.084″ Transmission Line		Keene GX–0300–55–22, ε_r = 2.55
Z3	1.195″ x 0.176″ Transmission Line	PCB	Etched Circuit Boards
Z4	0.125″ x 0.320″ Transmission Line		MRF21045 Rev. 3, CMR
Z5	1.100″ x 0.045″ Transmission Line		
Z6	0.442″ x 0.650″ Transmission Line		
Z7	0.490″ x 0.140″ Transmission Line		
Z8	0.540″ x 0.084″ Transmission Line		
Z10	0.825″ x 0.055″ Transmission Line		

Figure 1. MRF21045 Test Circuit Schematic

Table 1. MRF21045 Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite, #2743019447
C1, C2, C6	43 pF Chip Capacitors, ATC #100B430JCA500X
C7	5.6 pF Chip Capacitor, ATC #100B5R6JCA500X
C3, C9	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C10	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C5	1.0 μF Tantalum Chip Capacitor, Kemet #T491C105M050
C8	10 μF Tantalum Chip Capacitor, Kemet #T495X106K035AS4394
C11	22 μF Tantalum Chip Capacitor, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100″ ID, Motorola
N1, N2	Type N Flange Mounts, Omni Spectra #3052–1648–10
R1	1.0 kΩ, 1/8 W Chip Resistor
R2	180 kΩ, 1/8 W Chip Resistor
R3, R4	10 Ω, 1/8 W Chip Resistors

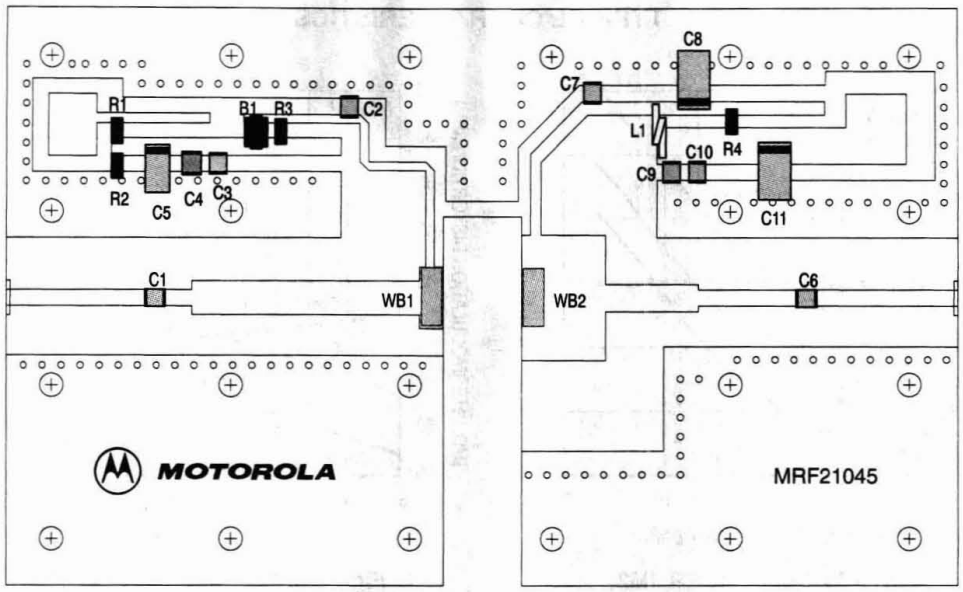


Figure 2. MRF21045 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

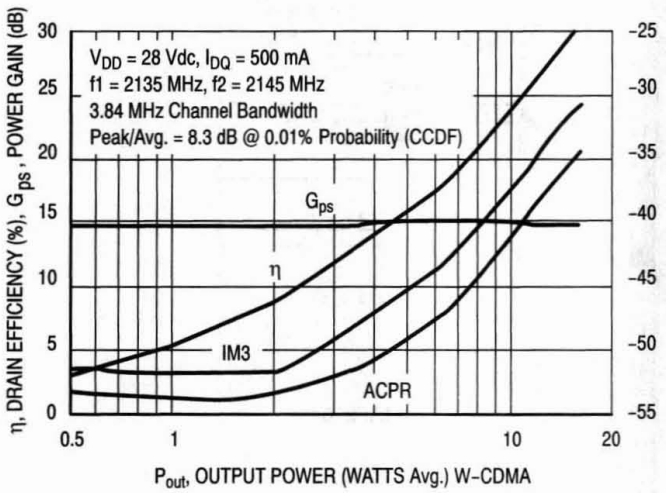


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

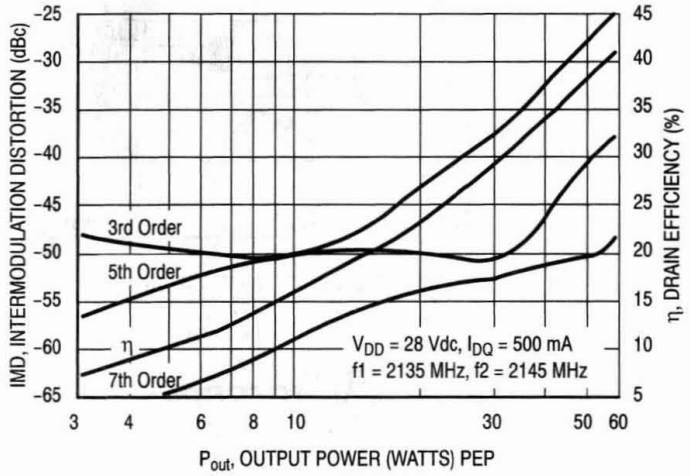


Figure 4. Intermodulation Distortion Products versus Output Power

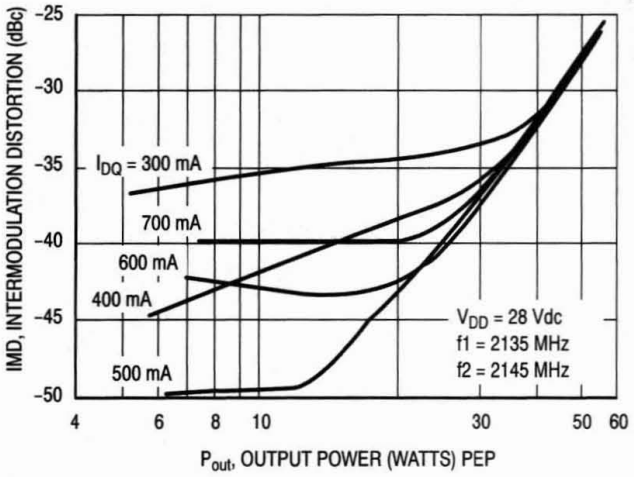


Figure 5. Intermodulation Distortion versus Output Power

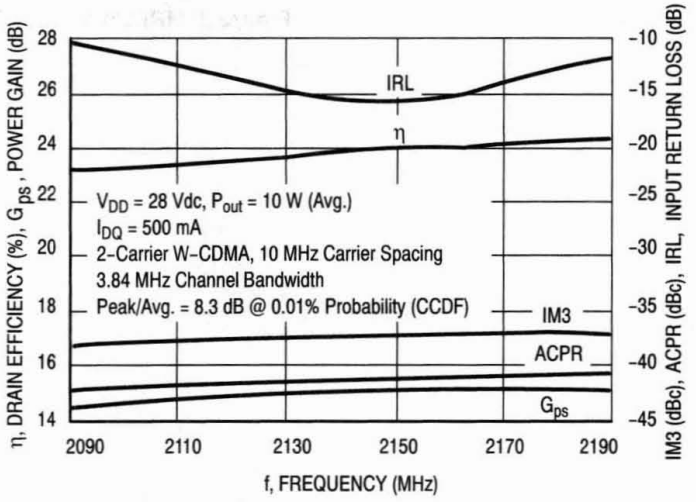


Figure 6. 2–Carrier W–CDMA Broadband Performance

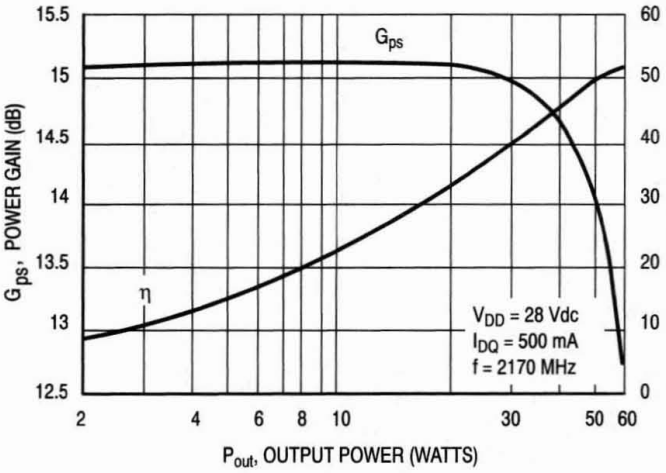


Figure 7. CW Performance

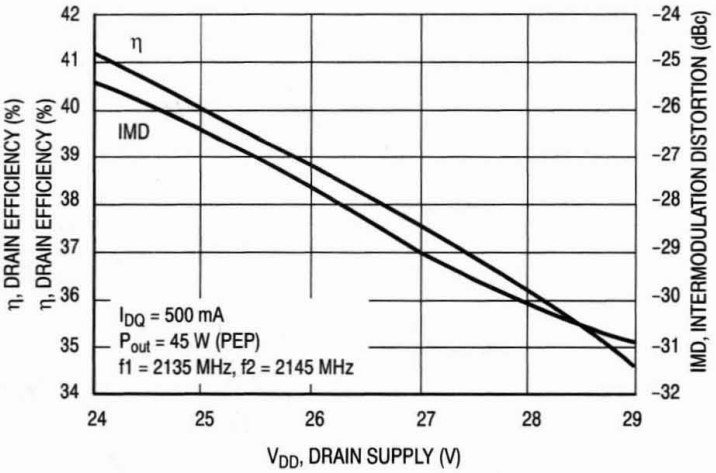


Figure 8. Two–Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

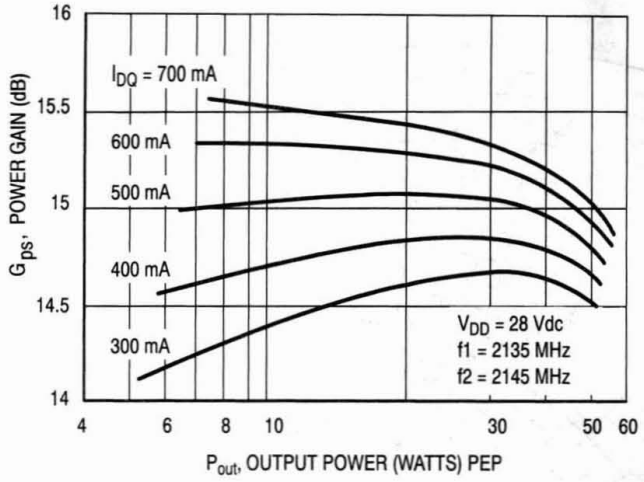


Figure 9. Two-Tone Power Gain versus Output Power

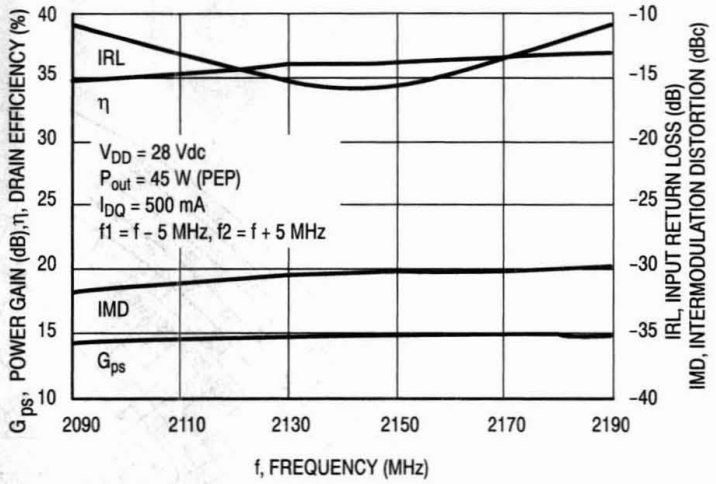


Figure 10. Two-Tone Broadband Performance

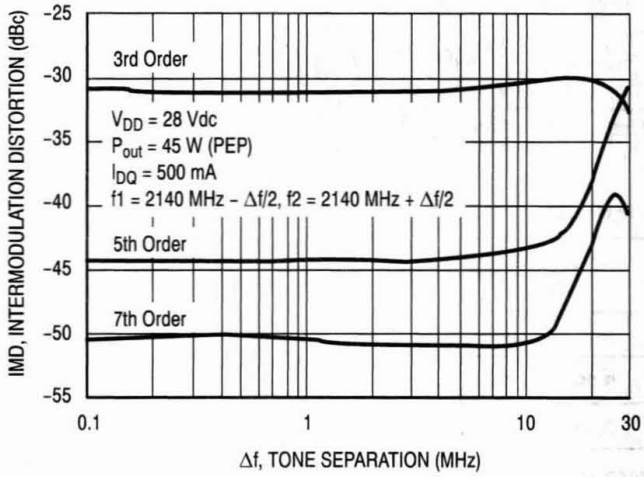


Figure 11. Intermodulation Distortion Products versus Two–Tone Spacing

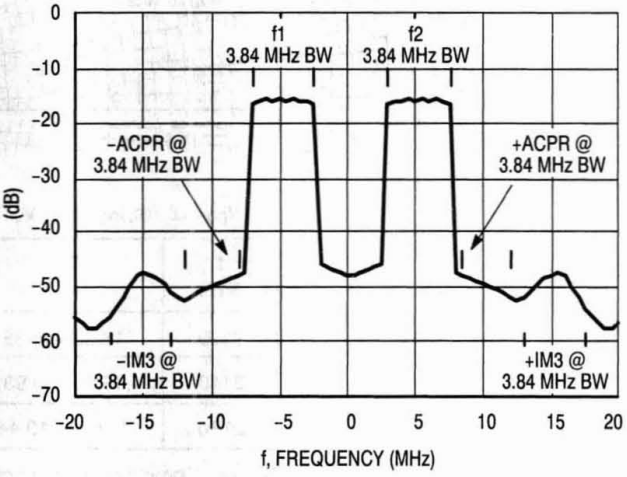
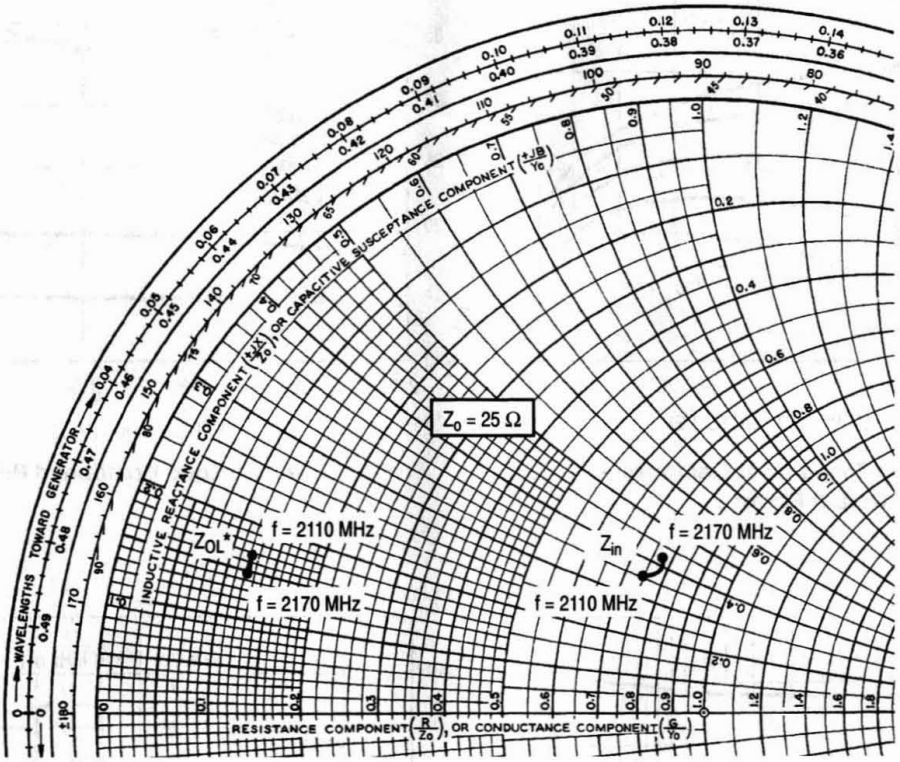


Figure 12. 2-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 10 W (Avg.)

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	18.88 + j8.86	3.11 + j4.18
2140	19.80 + j9.93	3.09 + j3.87
2170	19.68 + j10.44	3.12 + j3.72

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

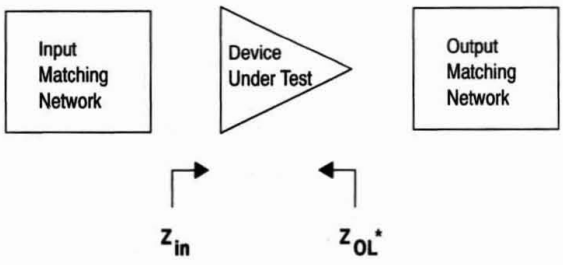


Figure 13. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

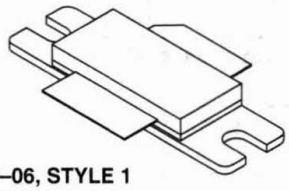
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21060
MRF21060R3
MRF21060S
MRF21060SR3

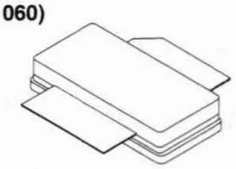
2170 MHz, 60 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 2.1 to 2.2 GHz. Suitable for W–CDMA, CDMA, TDMA, GSM and multicarrier amplifier applications.

- Typical W–CDMA Performance: 2140 MHz, 28 Volts
  5 MHz Offset @ 4.096 MHz BW, 15 DTCH
  Output Power — 6.0 Watts
  Power Gain — 12.5 dB
  Drain Efficiency — 15%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.



CASE 465–06, STYLE 1
(NI–780)
(MRF21060)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF21060S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	180 0.98	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

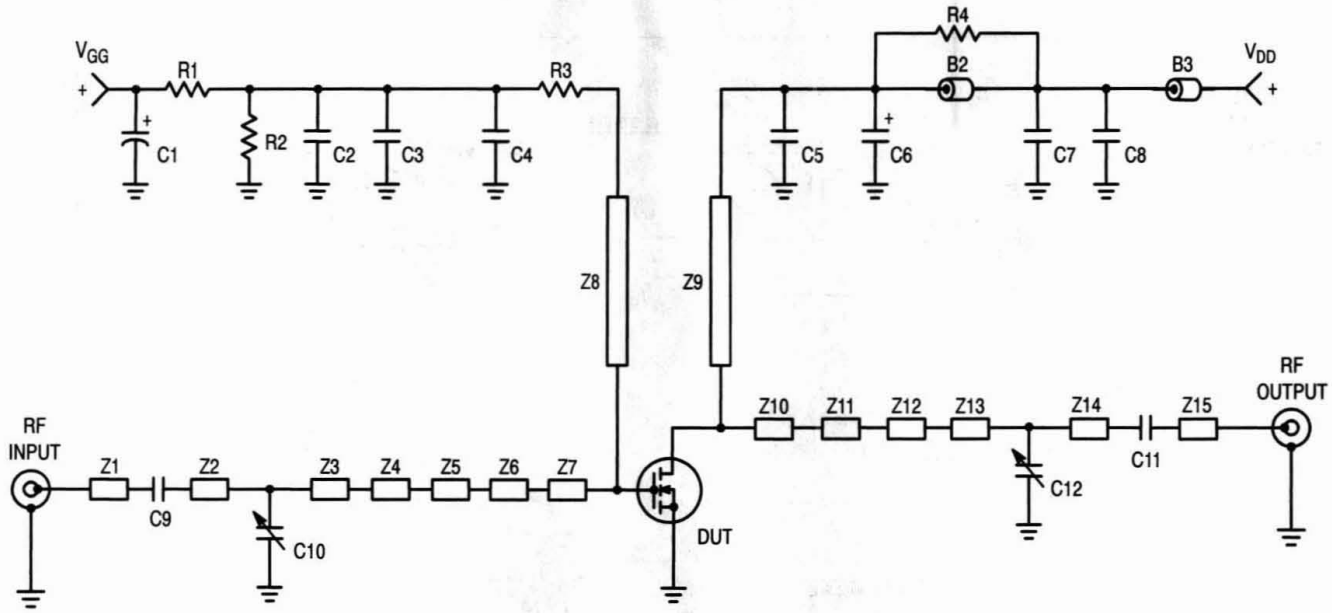
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.02	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.27	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	G_{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	η	31	34	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	–28	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 60 W PEP, I_{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 28 Vdc, P_{out} = 60 W CW, f = 2170 MHz)	P1dB	—	60	—	W
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 60 W CW, I_{DQ} = 500 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Beads, Fair Rite #2743019447	Z3	0.180″ x 0.100″ Microstrip
C1	10 μF, 50 V Electrolytic Chip Capacitor, Panasonic #ECEV1HV100R	Z4	0.152″ x 0.293″ Microstrip
C2, C7	1000 pF Chip Capacitors, ATC #100B102JCA500X	Z5	0.216″ x 0.100″ Microstrip
C3, C8	0.10 μF Chip Capacitors, Kemet #CDR33BX104AKWS	Z6	0.114″ x 0.410″ Microstrip
C4, C5	4.7 pF Chip Capacitors, ATC #100B4R7JCA500X	Z7	0.626″ x 0.872″ Microstrip
C6	22 μF, 35 V Tantalum Surface Mount Chip Capacitor, Sprague	Z8	1.050″ x 0.050″ Microstrip
C9, C11	9.1 pF Chip Capacitors, ATC #100B9R1JCA500X	Z9	0.830″ x 0.050″ Microstrip
C10	0.8 pF – 8.0 pF Variable Capacitor, Johanson Gigatrim	Z10	0.596″ x 1.040″ Microstrip
C12	0.4 pF – 4.5 pF Variable Capacitor, Johanson Gigatrim	Z11	0.186″ x 0.315″ Microstrip
R1	1 kΩ, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″	Z12	0.097″ x 0.525″ Microstrip
R2	560 kΩ, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″	Z13	0.353″ x 0.138″ Microstrip
R3	10 Ω, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″	Z14	0.112″ x 0.080″ Microstrip
R4	10 Ω, 1/4 W Fixed Film Chip Resistor, 0.08″ x 0.13″	Z15	0.722″ x 0.080″ Microstrip
Z1	0.743″ x 0.080″ Microstrip	Board	0.030″ Glass Teflon®, Arlon GX–0300–55–22, 2 oz Cu
Z2	0.070″ x 0.100″ Microstrip		

Figure 1. MRF21060 Test Circuit Schematic

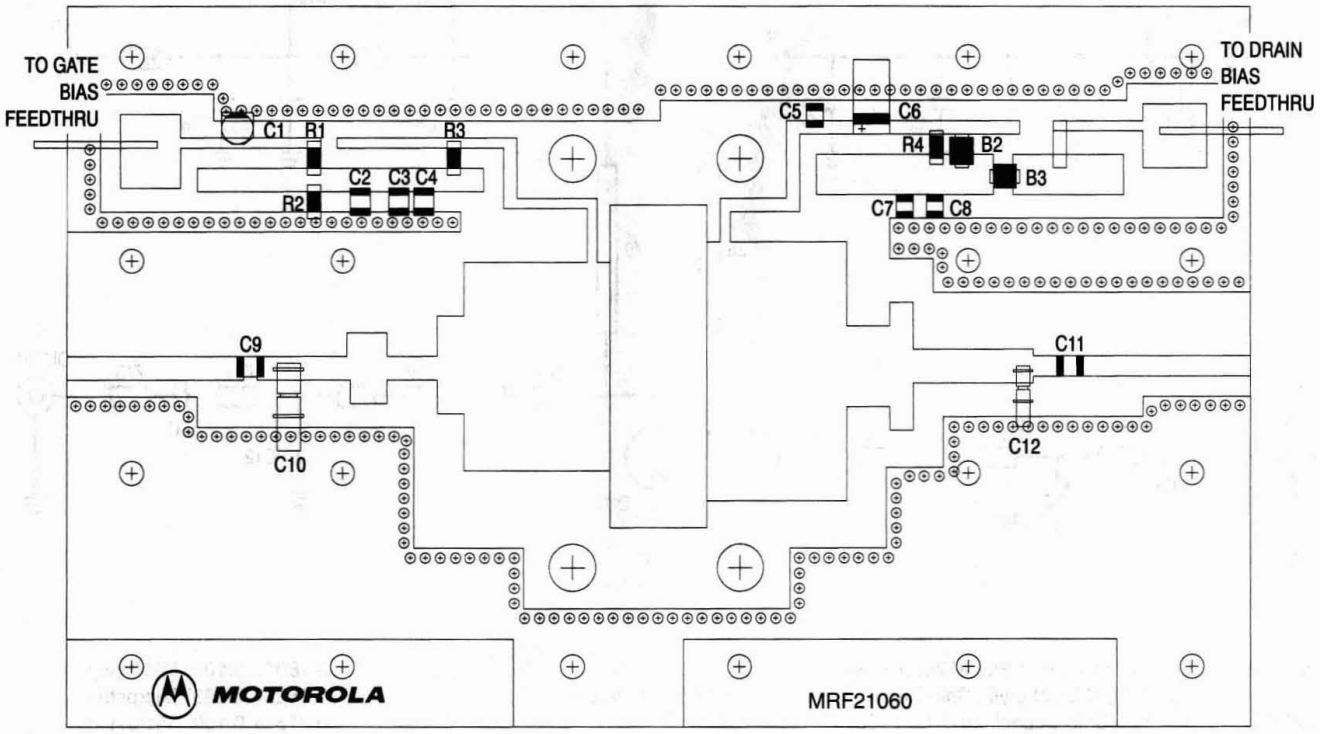


Figure 2. MRF21060 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

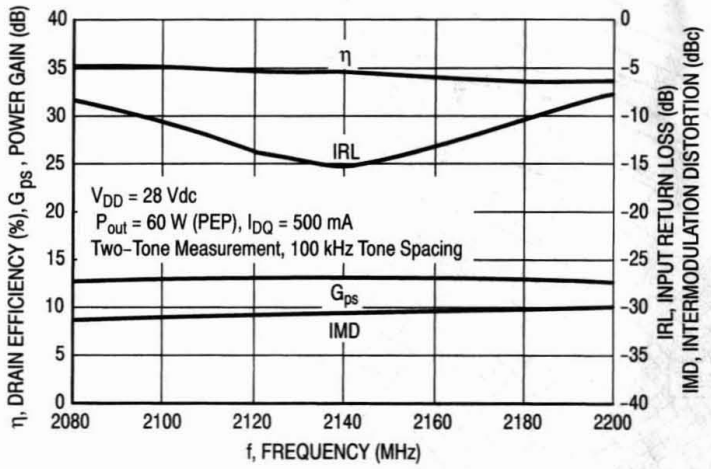


Figure 3. Class AB Broadband Circuit Performance

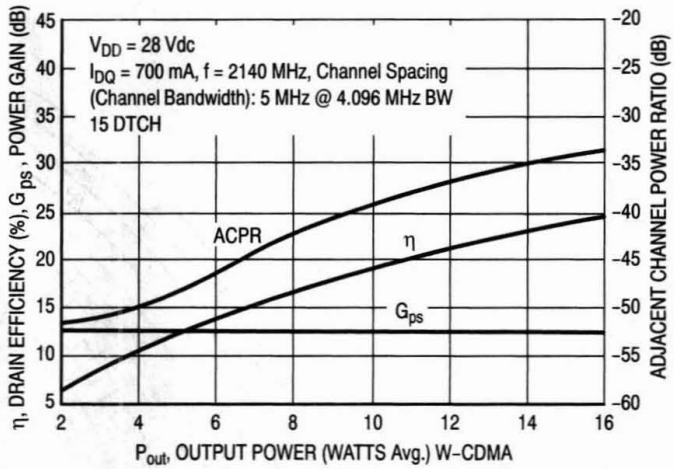


Figure 4. W–CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

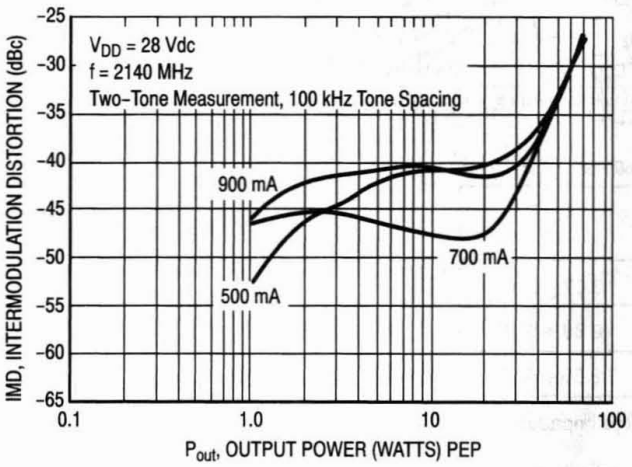


Figure 5. Intermodulation Distortion versus Output Power

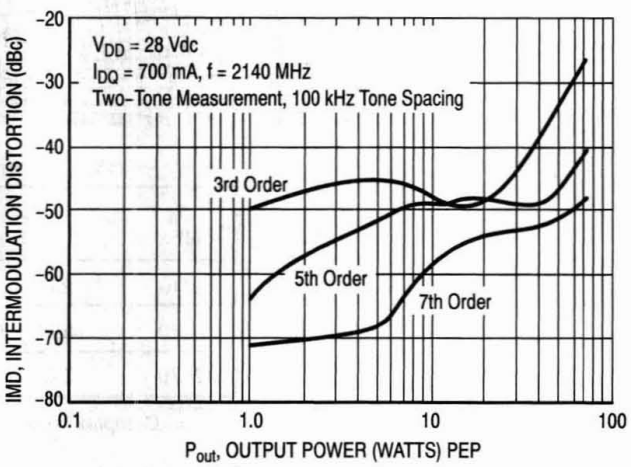


Figure 6. Intermodulation Distortion Products versus Output Power

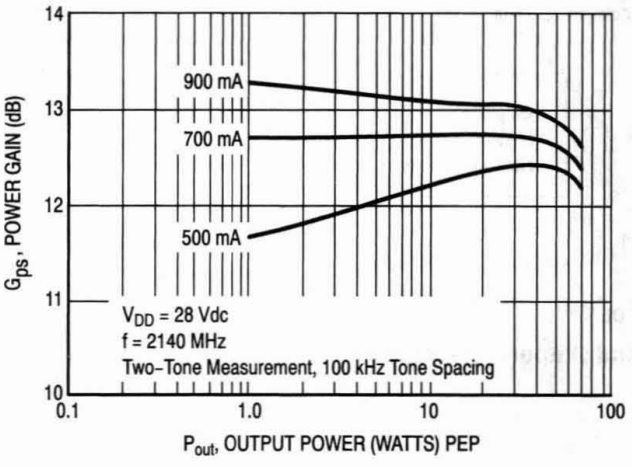


Figure 7. Power Gain versus Output Power

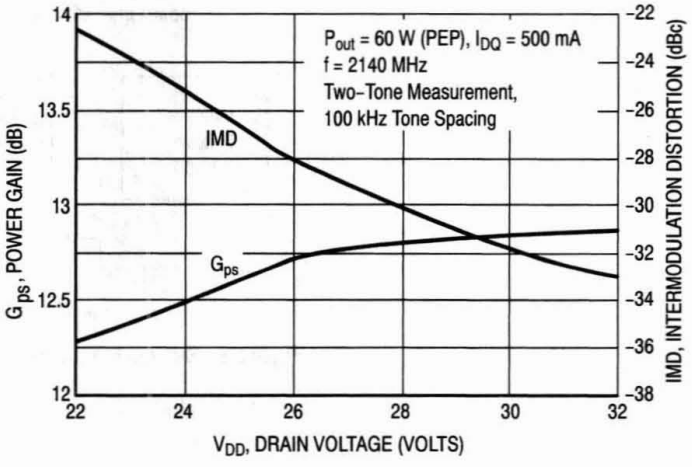
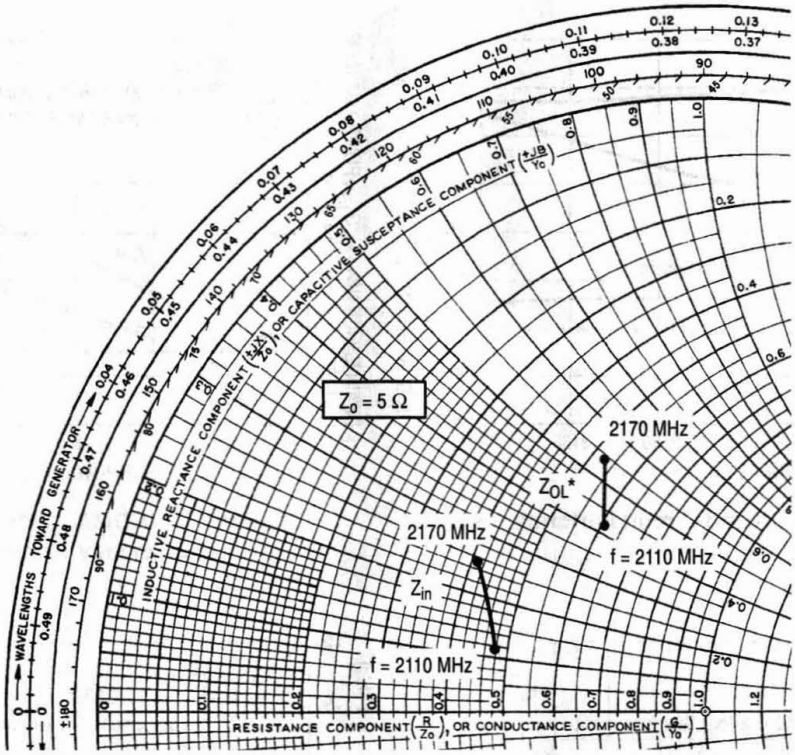


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 500 mA, P_{out} = 60 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	2.40 + j0.55	3.07 + j2.05
2140	2.26 + j0.87	2.89 + j2.38
2170	2.08 + j1.23	2.66 + j2.71

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

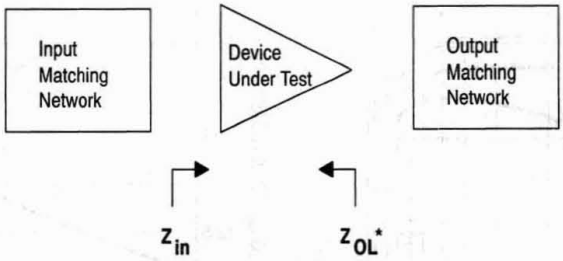


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

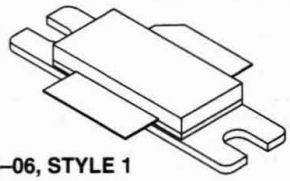
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21085
MRF21085S
MRF21085SR3
MRF21085LS
MRF21085LSR3

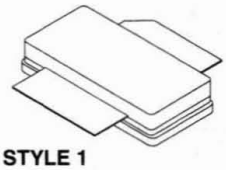
2170 MHz, 90 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Typical 2–carrier W–CDMA Performance for V_{DD} = 28 Volts, I_{DQ} = 1000 mA, f1 = 2135 MHz, f2 = 2145 MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ f1 –5 MHz and f2 +5 MHz, Distortion Products Measured over a 3.84 MHz BW @ f1 –10 MHz and f2 +10 MHz, Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
  Output Power — 19 Watts Avg.
  Power Gain — 13.6 dB
  Efficiency — 23%
  IM3 — –37.5 dBc
  ACPR — –41 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ″ Nominal.



CASE 465–06, STYLE 1
(NI–780)
(MRF21085)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF21085S, MRF21085LS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	224 1.28	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

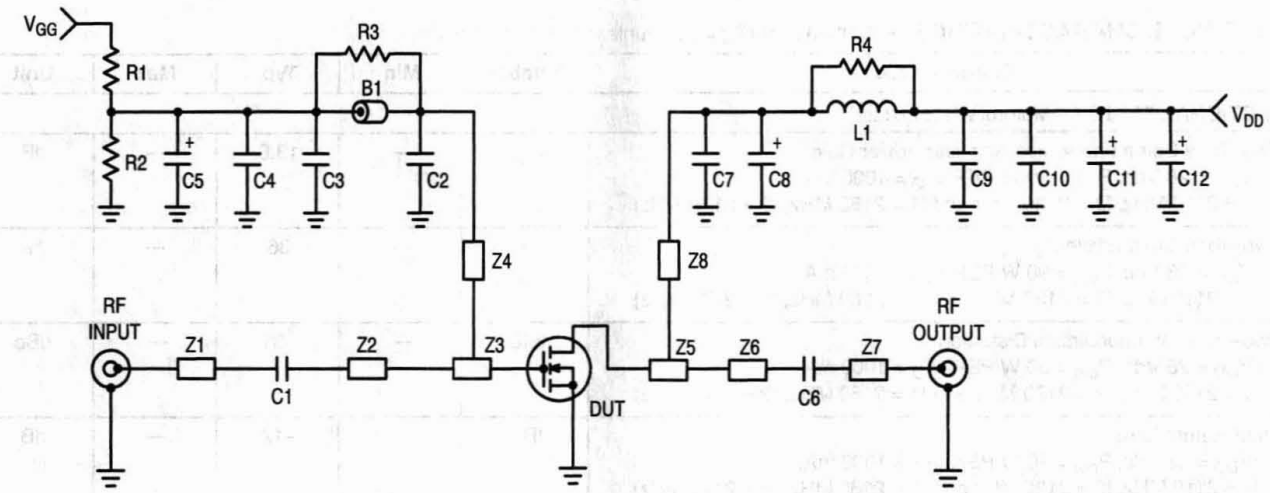
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (DC)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 1000 mAdc)	$V_{GS(Q)}$	3	3.9	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.18	0.21	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	6	—	S
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	3.6	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 19 W Avg., I_{DQ} = 1000 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	G_{ps}	12	13.6	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 19 W Avg., I_{DQ} = 1000 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	η	20	23	—	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 19 W Avg., I_{DQ} = 1000 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; IM3 measured over 3.84 MHz BW at f1 –10 MHz and f2 +10 MHz referenced to carrier channel power.)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{out} = 19 W Avg., I_{DQ} = 1000 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; ACPR measured over 3.84 MHz at f1 –5 MHz and f2 +5 MHz.)	ACPR	—	–41	–38	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 19 W Avg., I_{DQ} = 1000 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 90 W CW, I_{DQ} = 1000 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 1000 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	G_{ps}	—	13.6	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 1000 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	η	—	36	—	%
Two–Tone Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 1000 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 1000 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 2170 MHz)	P1dB	—	100	—	W



Z1	0.750″ x 0.084″ Microstrip	Board	0.030″ Glass Teflon®, Keene GX–0300–55–22, ε_r = 2.55
Z2	1.015″ x 0.084″ Microstrip		
Z3	0.480″ x 0.800″ Microstrip	PCB	Etched Circuit Boards MRF21085 Rev. 3, CMR
Z4	0.750″ x 0.050″ Microstrip		
Z5	0.610″ x 0.800″ Microstrip		
Z6	0.885″ x 0.084″ Microstrip		
Z7	0.720″ x 0.084″ Microstrip		
Z8	0.800″ x 0.070″ Microstrip		

Figure 1. MRF21085 Test Circuit Schematic

Table 1. MRF21085 Test Circuit Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite, #2743019447
C1, C6	43 pF Chip Capacitors, ATC #100B430JCA500X
C2	10 pF Chip Capacitor, ATC #100B100JCA500X
C3, C9	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C10	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C5	1.0 μF Tantalum Chip Capacitor, Kemet #T491C105M050
C7	2.7 pF Chip Capacitor, ATC #100B2R7JCA500X
C8	10 μF Tantalum Chip Capacitor, Kemet #T495X106K035AS4394
C11, C12	22 μF Tantalum Chip Capacitors, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100″ ID, Motorola
N1, N2	Type N Flange Mounts, Omni Spectra #3052–1648–10
R1	1.0 kΩ, 1/8 W Chip Resistor
R2	180 kΩ, 1/8 W Chip Resistor
R3, R4	10 Ω, 1/8 W Chip Resistors

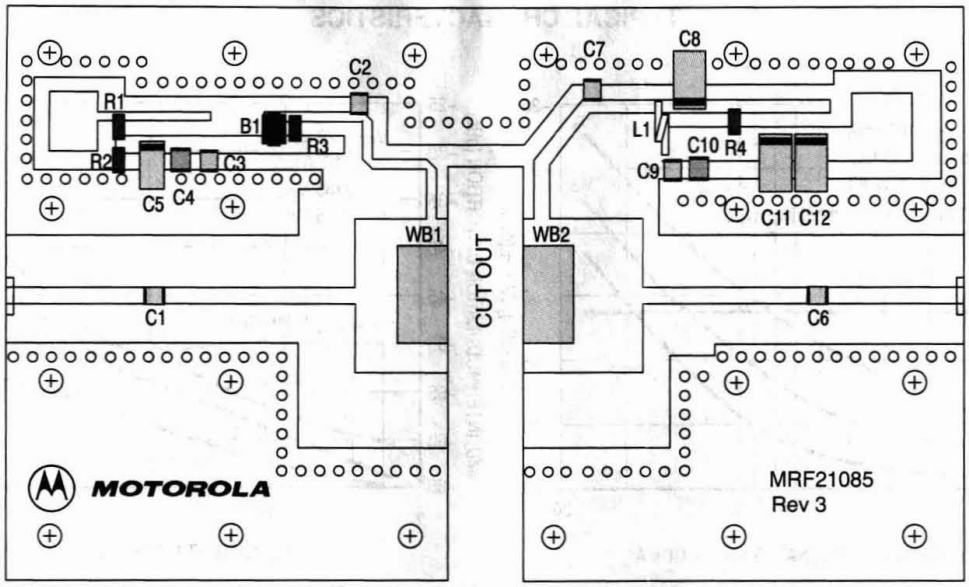


Figure 2. MRF21085 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

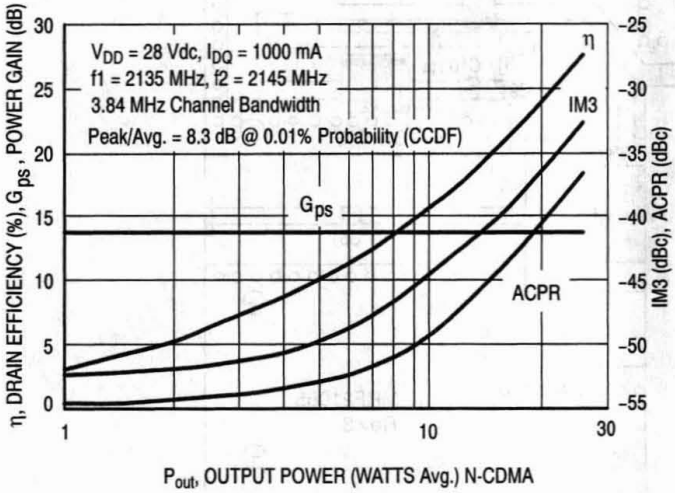


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

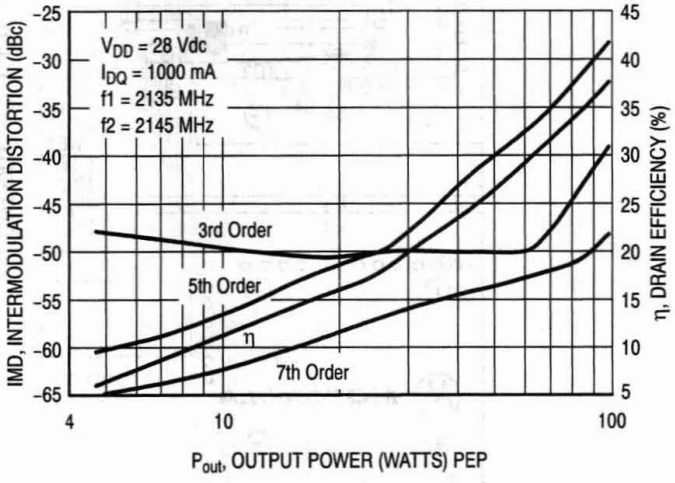


Figure 4. Intermodulation Distortion Products versus Output Power

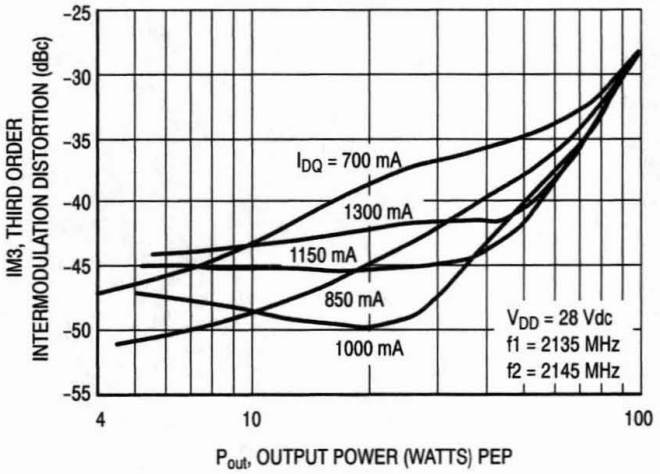


Figure 5. Third Order Intermodulation Distortion versus Output Power

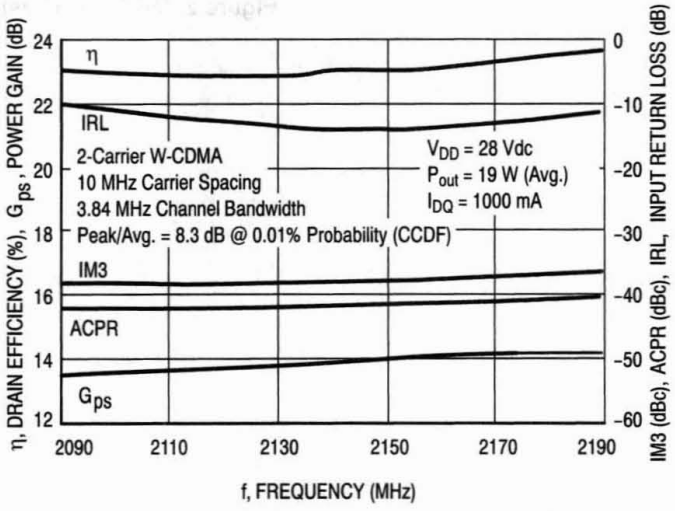


Figure 6. 2-Carrier W-CDMA Broadband Performance

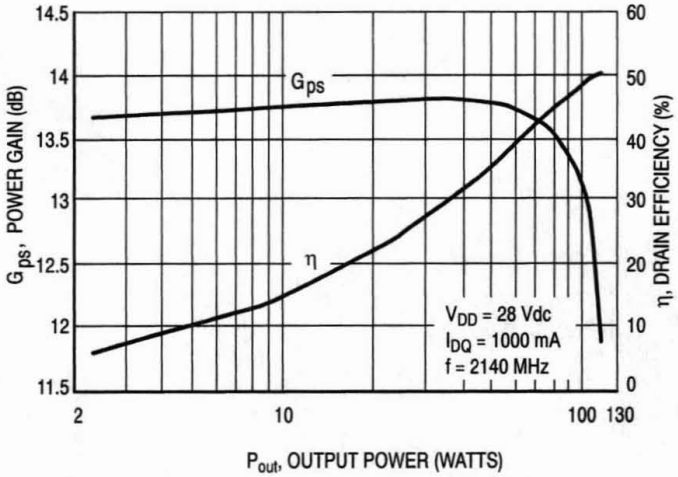


Figure 7. CW Performance

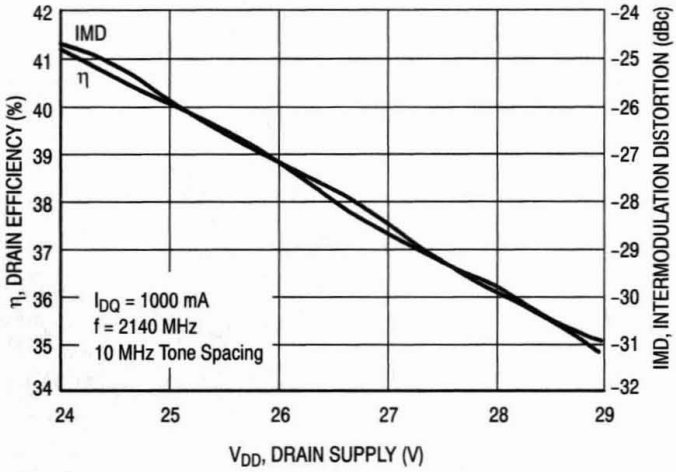


Figure 8. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

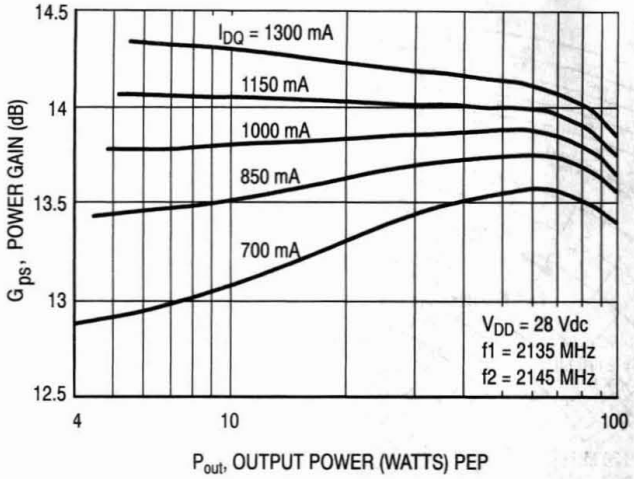


Figure 9. Two-Tone Power Gain versus Output Power

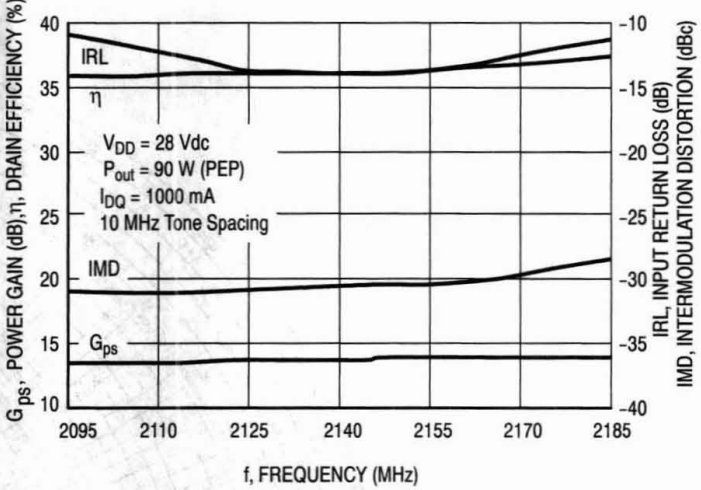


Figure 10. Two-Tone Broadband Performance

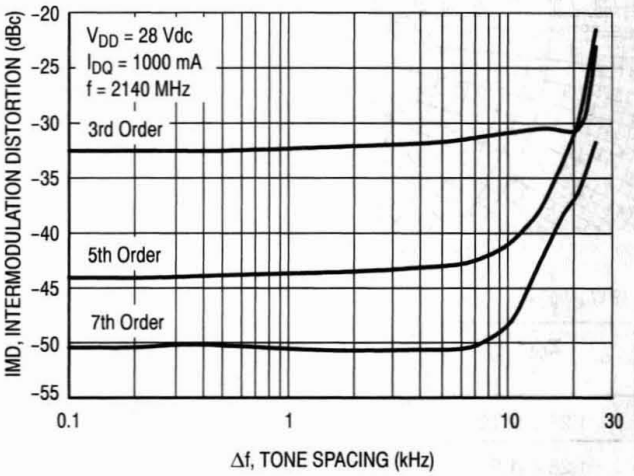


Figure 11. Intermodulation Distortion Products versus Two–Tone Spacing

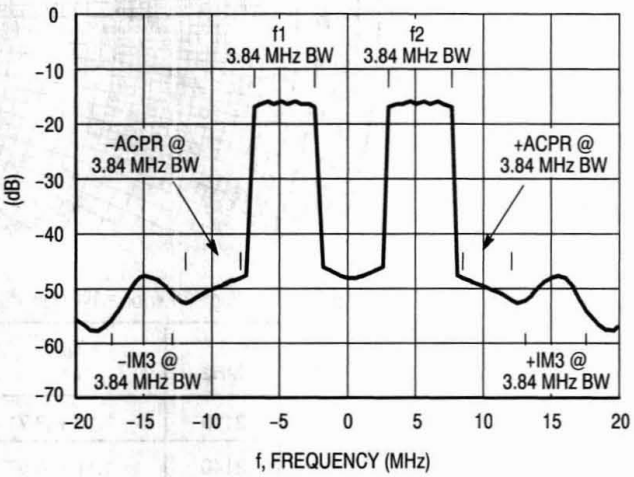
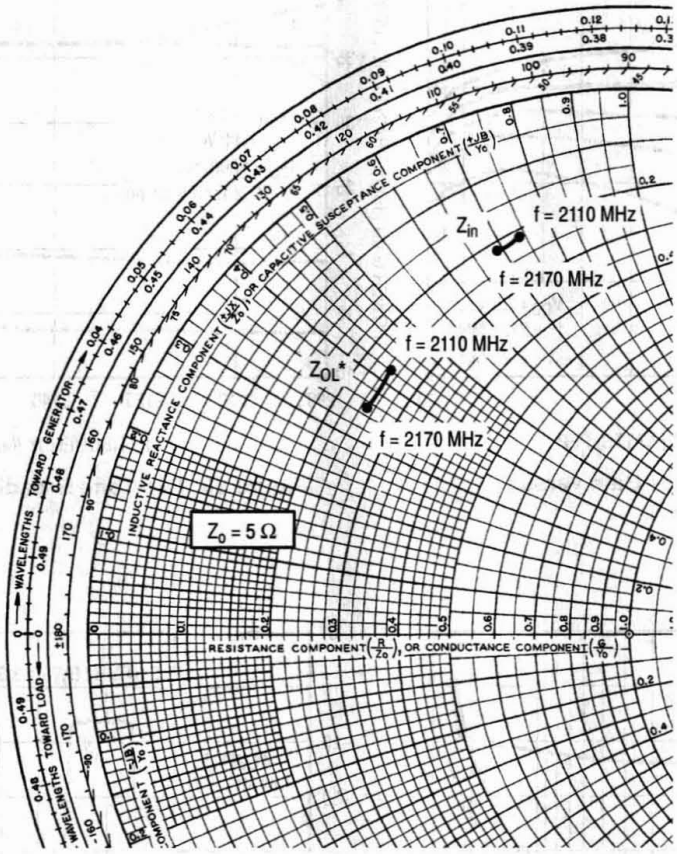


Figure 12. 2-Carrier W-CDMA Spectrum



V_{DD} = 28 V, I_{DQ} = 1000 mA, P_{out} = 19 W (Avg.)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
2110	1.10 + j3.71	1.23 + j2.10
2140	1.11 + j3.57	1.26 + j1.92
2170	1.12 + j3.40	1.25 + j1.76

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

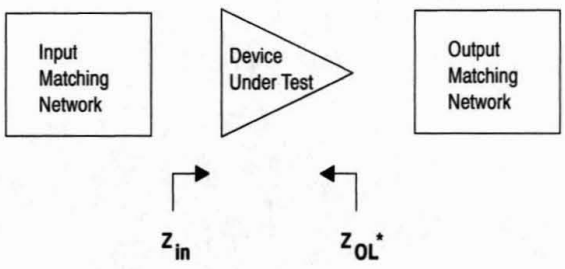


Figure 13. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

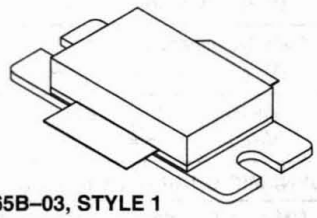
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21090
MRF21090S

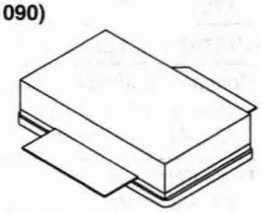
Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

- Typical W–CDMA Performance for 2140 MHz, 28 Volts
  4.096 MHz BW @ 5 MHz offset, 1 PERCH 15 DTCH:
  Output Power — 11.5 Watts
  Efficiency — 16%
  Gain — 12.2 dB
  ACPR — –45 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2110 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters

2170 MHz, 90 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465B–03, STYLE 1
(NI–880)
(MRF21090)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF21090S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions		Class
Human Body Model	MRF21090 MRF21090S	2 (Minimum) 1 (Minimum)
Machine Model	MRF21090 MRF21090S	M3 (Minimum) M4 (Minimum)

THERMAL CHARACTERISTICS

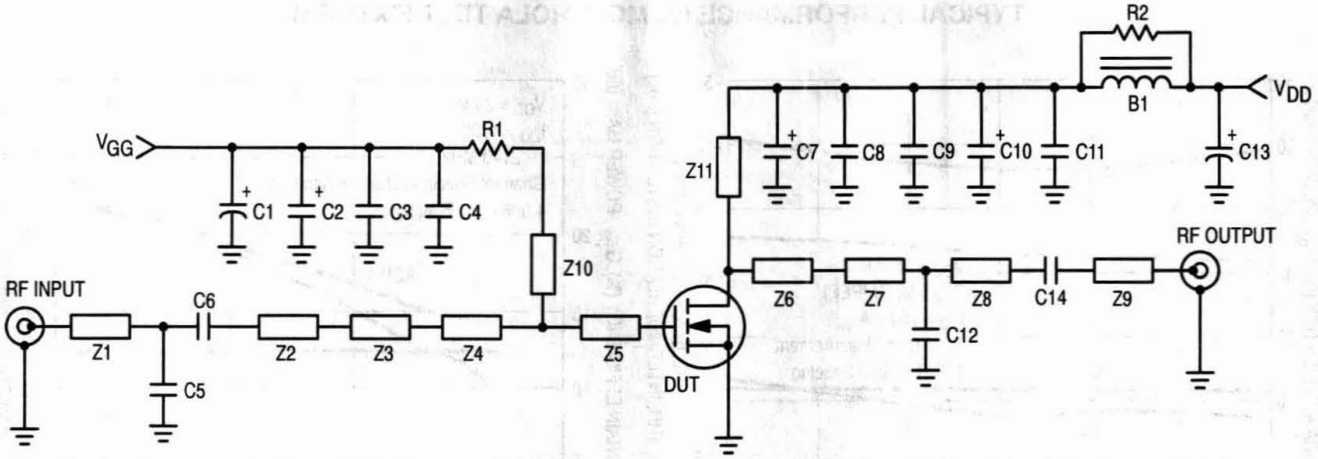
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 300 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 750 mA)	$V_{GS(Q)}$	3	3.8	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(on)}$	—	0.1	0.6	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	G_{ps}	10	11.7	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	η	30	33	—	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IMD	—	–30	–27.5	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IRL	—	–12	–9.0	dB
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 75 W CW, I_{DQ} = 750 mA, f = 2170 MHz)	G_{ps}	—	11.7	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 75 W CW, I_{DQ} = 750 mA, f = 2170 MHz)	η	—	41	—	%
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1	Ferrite Bead, Fair Rite #2743019447
C1, C13	470 μF, 50 V Electrolytic Capacitors
C2, C10	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
C3, C9	20 nF Chip Capacitors, ATC #100B203MCA500X
C4, C8	5.1 pF Chip Capacitors, ATC #100B5R1CCA500X
C5, C12	0.4 – 2.5 pF Variable Capacitors, Johanson Gigatrim
C6	10 pF Chip Capacitor, ATC #100B100JCA500X
C7	1 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet
C11	1 nF Chip Capacitor, ATC #100B102JCA500X
C14	8.2 pF Chip Capacitor, ATC #100B8R2CCA500X
R1	13 Ω, 1/4 W Chip Resistor, Garret Instrument #RM73B2B130JT,
R2	12 Ω, 1/4 W Chip Resistor, Garret Instrument #RM73B2B120JT
Z1	30.7 x 2.09 mm Microstrip
Z2	5.99 x 2.09 mm Microstrip
Z3	7.55 x 9.89 mm Microstrip
Z4	3.77 x 15.71 mm Microstrip
Z5	6.89 x 26.17 mm Microstrip
Z6	14.93 x 32.05 mm Microstrip
Z7	10.23 x 2.09 mm Microstrip
Z8	6.03 x 2.09 mm Microstrip
Z9	23.98 x 2.09 mm Microstrip
Z10	29.82 x 1.15 mm Microstrip
Z11	17.08 x 1.15 mm Microstrip
WS1, WS2	Beryllium Copper Wear Blocks 5 mils Thick
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type N Jack Connectors, 3052–1648–10, Omni Specra
	4–40 Head Screws 0.125″ Long
	4–40 Head Screws 0.188″ Long
	4–40 Head Screws 0.312″ Long
	4–40 Head Screws 0.438″ Long
Endplates Brass	Endplates for Copper Bedstead
Bedstead	Copper Bedstead/Heatsink
Insert	Copper Bedstead Insert
Raw PCB	0.030″ Glass Teflon®, 2 oz Copper Clad 3″ x 5″ Arion
RF Circuit	3″ x 5″ Copper Clad PCB Teflon®, MRF21090, CMR

Figure 1. MRF21090 Test Circuit Schematic

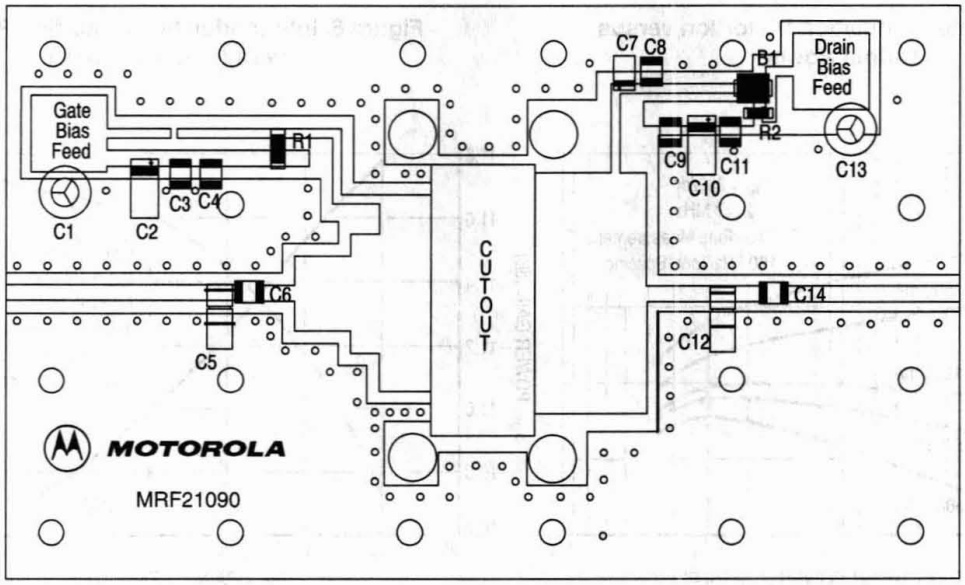


Figure 2. MRF21090 Test Circuit Component Layout

TYPICAL PERFORMANCE (IN MOTOROLA TEST FIXTURE)

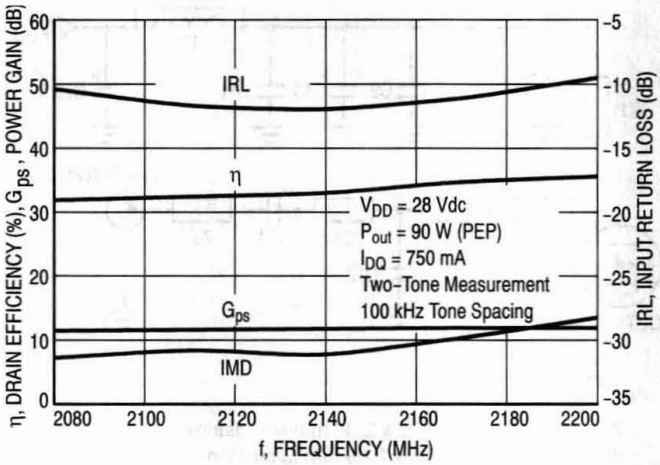


Figure 3. Class AB Broadband Circuit Performance

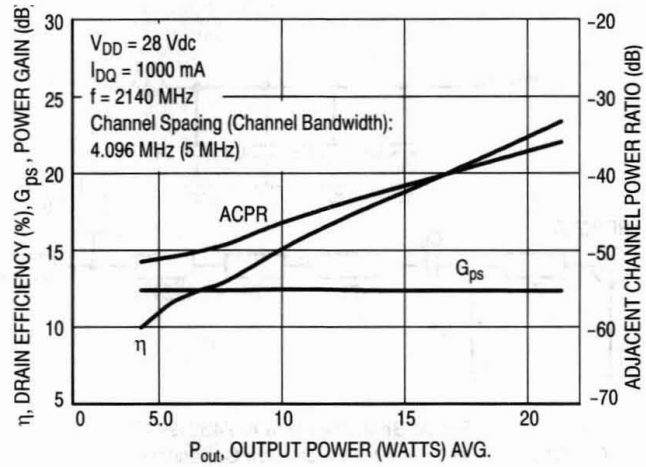


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

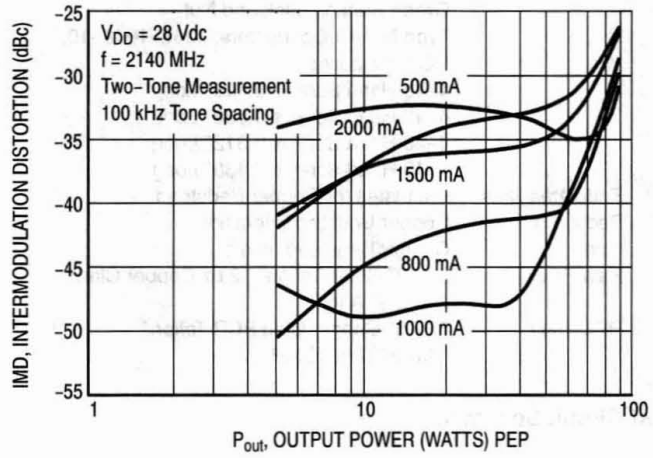


Figure 5. Intermodulation Distortion versus Output Power

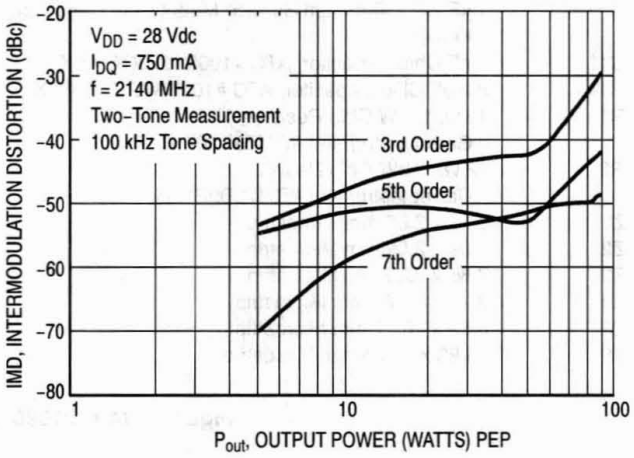


Figure 6. Intermodulation Distortion Products versus Output Power

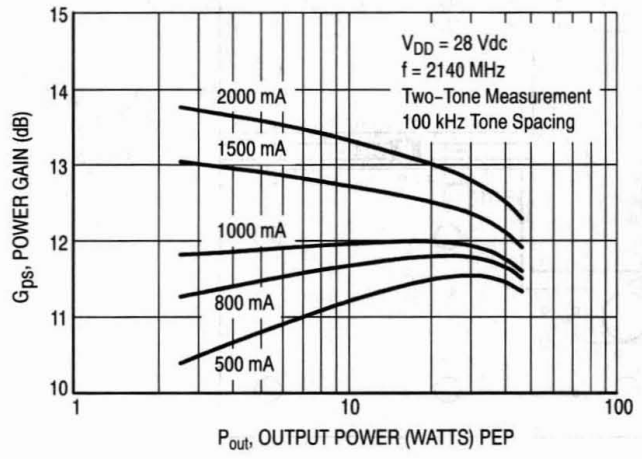


Figure 7. Power Gain versus Output Power

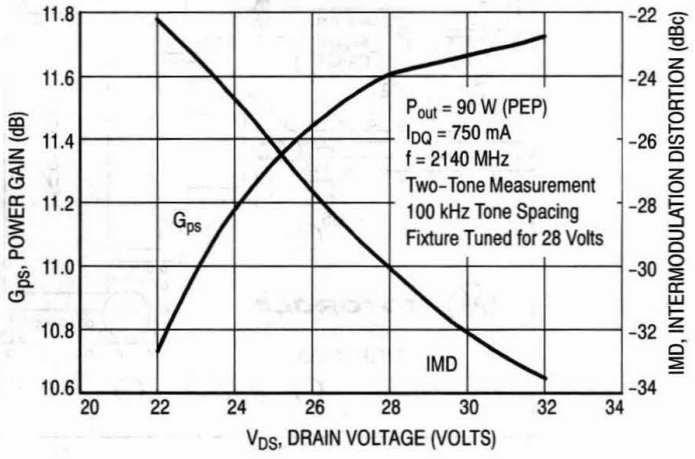
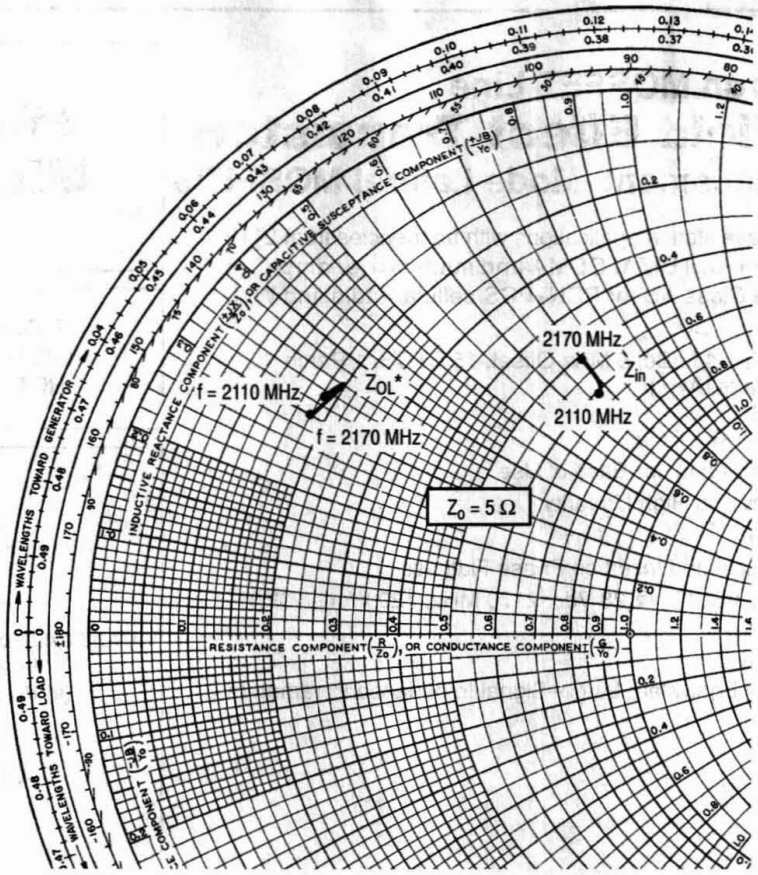


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 750 mA, P_{out} = 90 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	3.03 + j3.40	0.92 + j1.67
2140	3.02 + j3.46	0.97 + j1.80
2170	2.60 + j3.50	0.90 + j1.52

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given power, voltage, IMD, bias current and frequency.

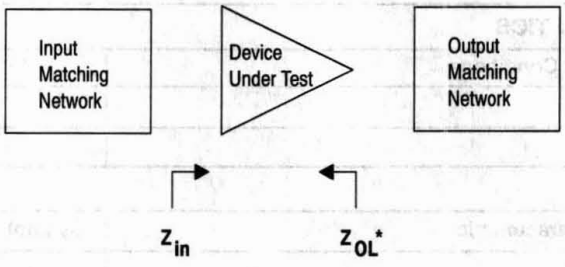


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

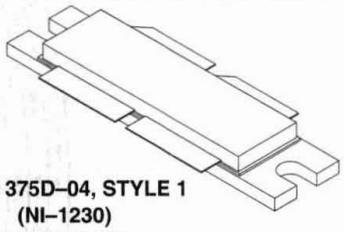
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21120
MRF21120S

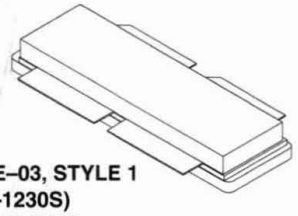
2170 MHz, 120 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- W–CDMA Performance @ –45 dBc, 5 MHz Offset, 15 DTCH, 1 Perch
  Output Power — 14 Watts (Avg.)
  Power Gain — 11.5 dB
  Efficiency — 16%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2170 MHz, 120 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 375D–04, STYLE 1
(NI–1230)
(MRF21120)



CASE 375E–03, STYLE 1
(NI–1230S)
(MRF21120S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	389 2.22	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

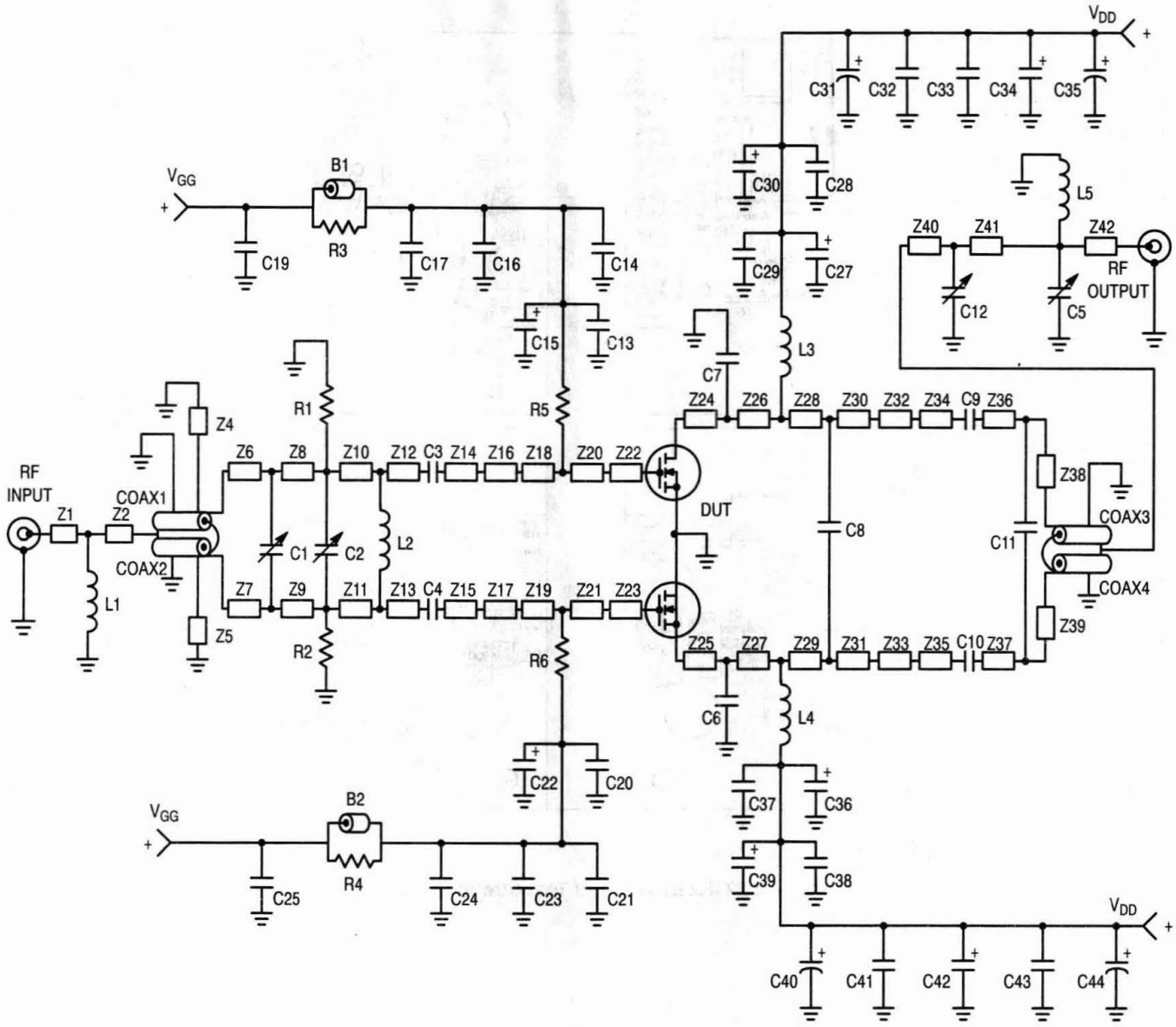
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μAdc)		$V_{(BR)DSS}$	65	—	—	Vdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
ON CHARACTERISTICS (1)						
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)		g_{fs}	—	4.8	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)		$V_{GS(th)}$	2.5	3	3.8	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 500 mA)		$V_{GS(Q)}$	3	3.9	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 2 A)		$V_{DS(on)}$	—	0.38	0.5	Vdc
DYNAMIC CHARACTERISTICS (1)						
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	2.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2)						
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2170.0 MHz, f2 = 2170.1 MHz)	MRF21120 MRF21120S	G_{ps}	 10.5 10.4	 11.4 11.2	 — —	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2170.0 MHz, f2 = 2170.1 MHz)		η	30	34.5	—	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2170.0 MHz, f2 = 2170.1 MHz)	MRF21120 MRF21120S	IMD	 — —	 –31 –31	 –28 –27	dB
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2170.0 MHz, f2 = 2170.1 MHz)		IRL	—	–12	–9	dB
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)		G_{ps}	—	11.5	—	dB
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz)		G_{ps}	—	11.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz)		η	—	34.5	—	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz)		IMD	—	–31	—	dB
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 120 W PEP, I_{DQ} = 2 × 500 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz)		IRL	—	–12	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 28 Vdc, CW, I_{DQ} = 2 × 500 mA, f1 = 2170.0 MHz)		P1dB	—	120	—	Watts

(1) Each side of device measured separately.
(2) Device measured in push–pull configuration.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture) (2) (continued)					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 × 500 mA, f1 = 2170.0 MHz)	G_{ps}	—	10.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 × 500 mA, f1 = 2170.0 MHz)	η	—	42	—	%
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 120 W CW, I_{DQ} = 2 × 500 mA, f = 2.17 GHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(2) Device measured in push–pull configuration.



B1, B2	Ferrite Beads, Fair Rite
C1, C2, C12	0.6 – 4.5 pF Variable Capacitors, Johanson Gigatrim
C3, C4, C9, C10	10 pF Chip Capacitors, B Case, ATC
C5	0.4 – 2.5 pF Variable Capacitor, Johanson Gigatrim
C6, C7	2.0 pF Chip Capacitors, B Case, ATC
C8	0.5 pF Chip Capacitor, B Case, ATC
C11	0.2 pF Chip Capacitor, B Case, ATC
C13, C20, C29, C37	5.1 pF Chip Capacitors, B Case, ATC
C14, C21, C28, C38	91 pF Chip Capacitors, B Case, ATC
C15, C22, C27, C34, C36, C42	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
C16, C23, C33, C43	0.039 μF Chip Capacitors, B Case, ATC
C17, C24, C32, C41	1000 pF Chip Capacitors, B Case, ATC
C19, C25	0.022 μF Chip Capacitors, B Case, ATC
C30, C39	1.0 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
C31, C40	100 μF, 50 V Electrolytic Capacitors, Sprague
C35, C44	470 μF, 63 V Electrolytic Capacitors, Sprague
Coax1, Coax2	25 Ω Semi Rigid Coax, 70 mil OD, 1.05″ Long
Coax3, Coax4	50 Ω Semi Rigid Coax, 85 mil OD, 1.05″ Long
L1, L5	5.0 nH Minispring Inductors, Coilcraft
L2	8.0 nH Minispring Inductor, Coilcraft
L3, L4	7.15 nH Microspring Inductors, Coilcraft
R1, R2	1 kΩ, 1/4 W Fixed Metal Film Resistors, Dale
R3, R4	270 Ω, 1/8 W Fixed Film Chip Resistors, Dale
R5, R6	1.2 kΩ, 1/8 W Fixed Film Chip Resistors, Dale
Z1	0.150″ x 0.080″ Microstrip
Z2	0.320″ x 0.080″ Microstrip
Z4, Z5	1.050″ x 0.080″ Microstrip
Z6, Z7	0.120″ x 0.080″ Microstrip
Z8, Z9	0.140″ x 0.080″ Microstrip
Z10, Z11	0.610″ x 0.080″ Microstrip
Z12, Z13	0.135″ x 0.080″ Microstrip
Z14, Z15	0.130″ x 0.080″ Microstrip
Z16, Z17	0.300″ x 0.350″ Microstrip
Z18, Z19	0.150″ x 0.500″ Microstrip
Z20, Z21	0.075″ x 0.500″ Microstrip
Z22, Z23	0.330″ x 0.500″ Microstrip
Z24, Z25	0.100″ x 0.550″ Microstrip
Z26, Z27	0.175″ x 0.550″ Microstrip
Z28, Z29	0.045″ x 0.550″ Microstrip
Z30, Z31	0.190″ x 0.325″ Microstrip
Z32, Z33	0.080″ x 0.325″ Microstrip
Z34, Z35	0.515″ x 0.080″ Microstrip
Z36, Z37	0.020″ x 0.080″ Microstrip
Z38, Z39	0.565″ x 0.080″ Microstrip
Z40	0.100″ x 0.080″ Microstrip
Z41	0.470″ x 0.080″ Microstrip
Z42	0.100″ x 0.080″ Microstrip
Board Material	0.03″ Teflon®, ε_r = 2.55 Copper Clad, 2 oz. Cu
Connectors	N–Type Panel Mount, Stripline

Figure 1. 2.1 – 2.2 GHz Broadband Test Circuit Schematic

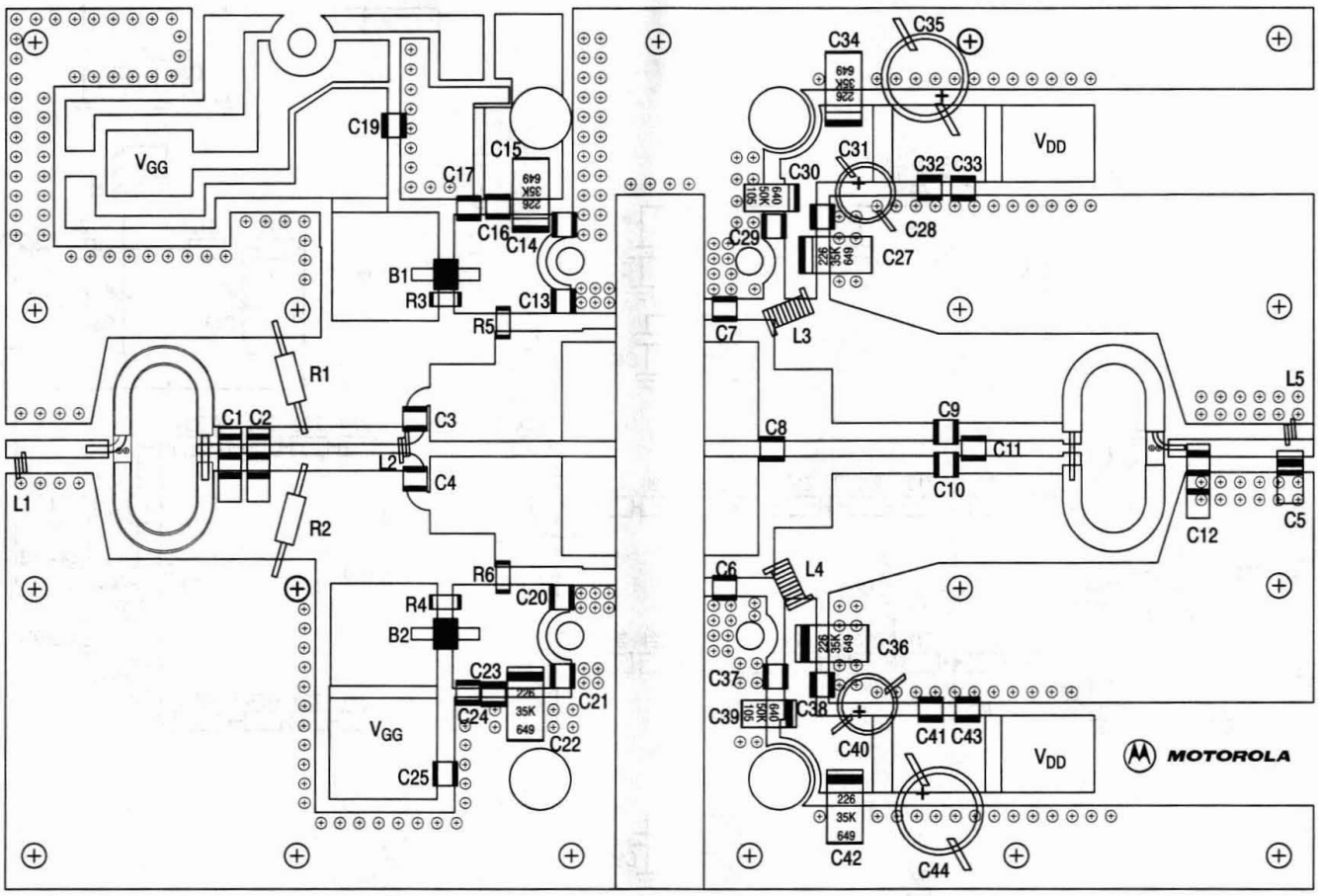


Figure 2. 2.1 – 2.2 GHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

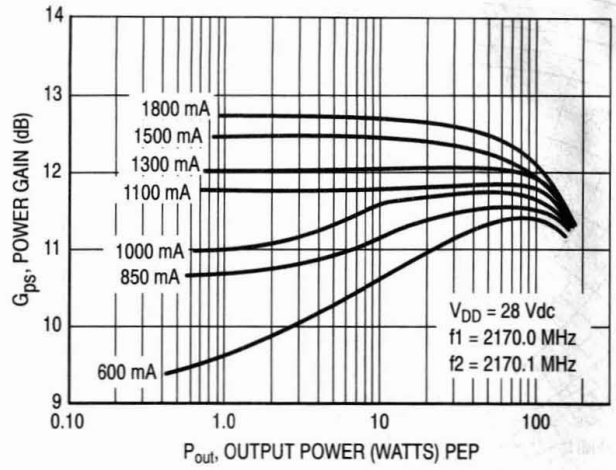


Figure 3. Power Gain versus Output Power

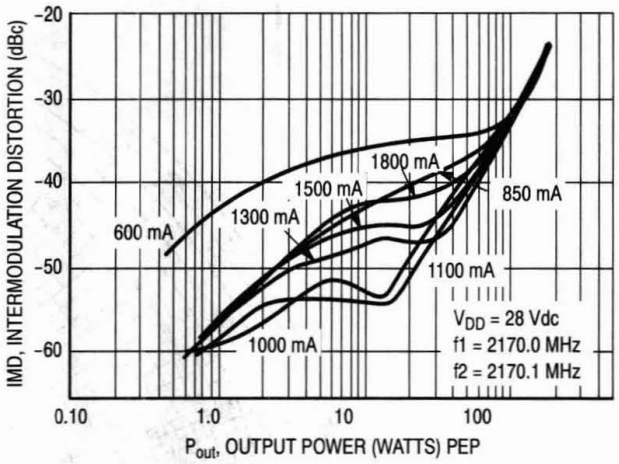


Figure 4. Intermodulation Distortion versus Output Power

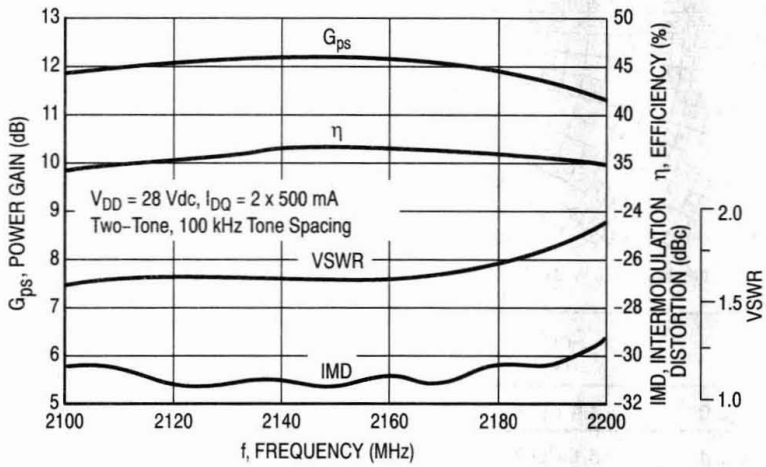


Figure 5. Class AB Broadband Circuit Performance

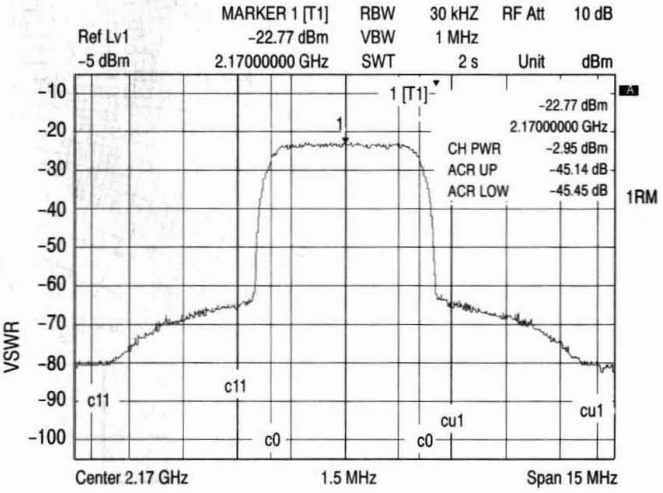


Figure 6. 2.17 GHz W–CDMA Mask at 14 Watts (Avg.), 5 MHz Offset, 15 DTCH, 1 Perch

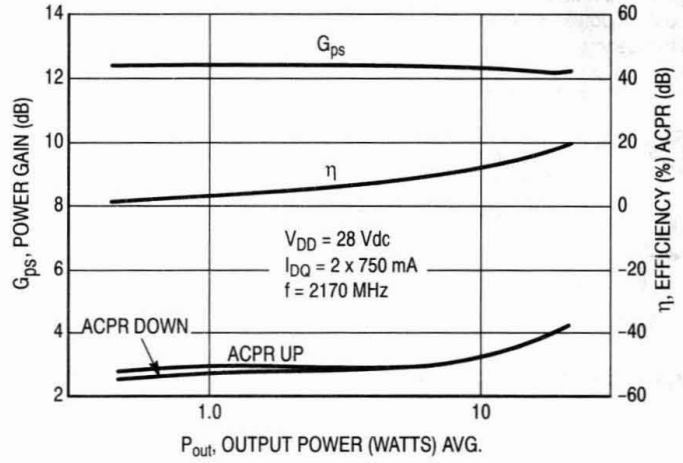


Figure 7. Power Gain, Efficiency, ACPR versus Output Power (W–CDMA)

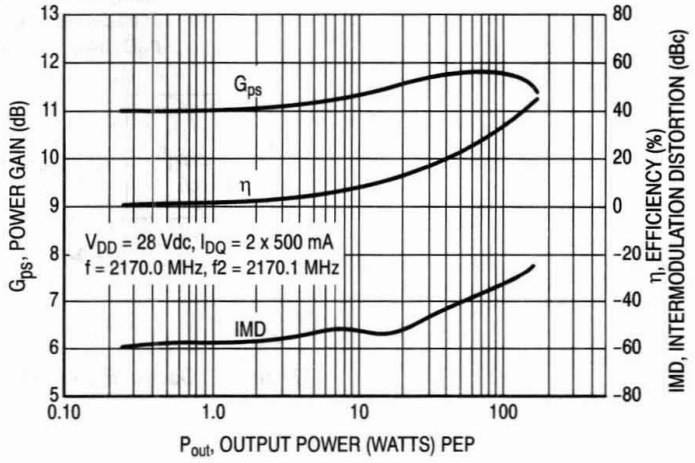
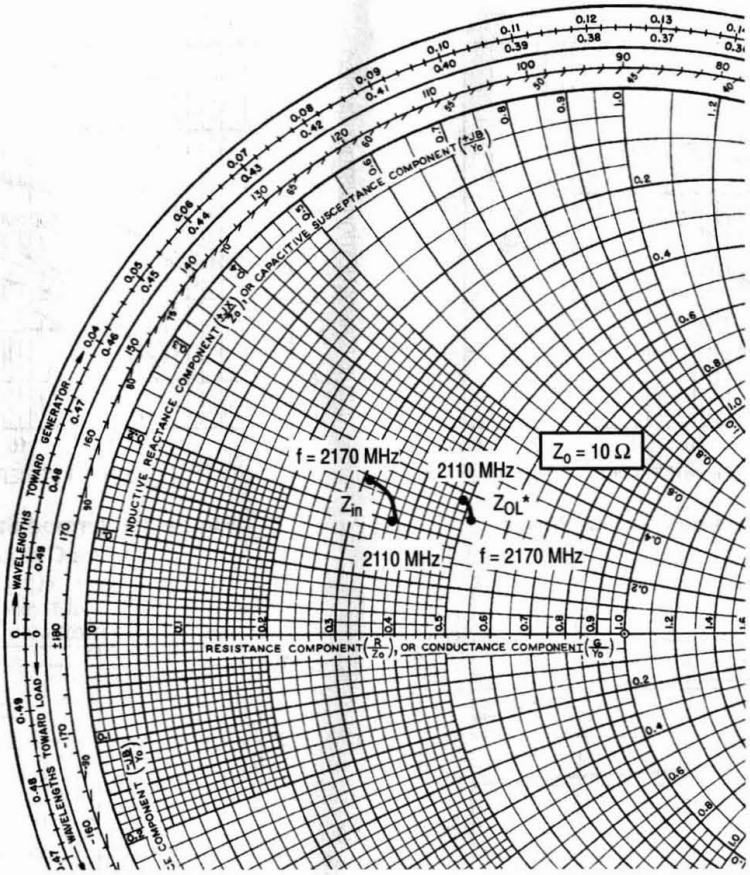


Figure 8. Power Gain, Efficiency, IMD versus Output Power



V_{DD} = 28 V, I_{DQ} = 2 × 500 mA, P_{out} = 120 Watts PEP

f MHz	Z_{in} Ω	Z_{OL}^* Ω
2110	3.7 + j2.0	4.9 + j2.8
2140	3.5 + j2.4	5.1 + j2.7
2170	3.1 + j2.5	5.2 + j2.5

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

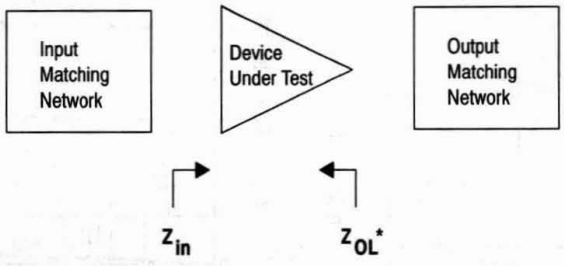


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

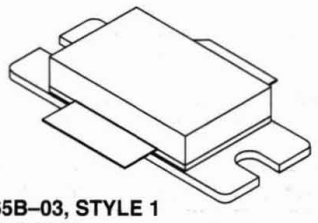
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21125
MRF21125S
MRF21125SR3

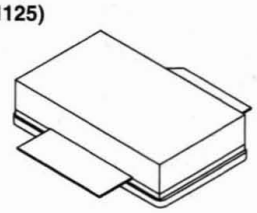
2170 MHz, 125 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Typical 2–carrier W–CDMA Performance for V_{DD} = 28 Volts, I_{DQ} = 1600 mA, f1 = 2.1125 GHz, f2 = 2.1225 GHz, Channel bandwidth = 3.84 MHz, adjacent channels at ± 5 MHz , ACPR and IM3 measured in 3.84 MHz bandwidth. Peak/Avg = 8.5 dB @ 0.01% probability on CCDF.
  Output Power — 20 Watts
  Efficiency — 18%
  Gain — 13 dB
  IM3 — –43 dBc
  ACPR — –45 dBc
- 100% Tested under 2–carrier W–CDMA
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 125 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465B–03, STYLE 1
(NI–880)
(MRF21125)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF21125S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	330 1.89	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.53	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

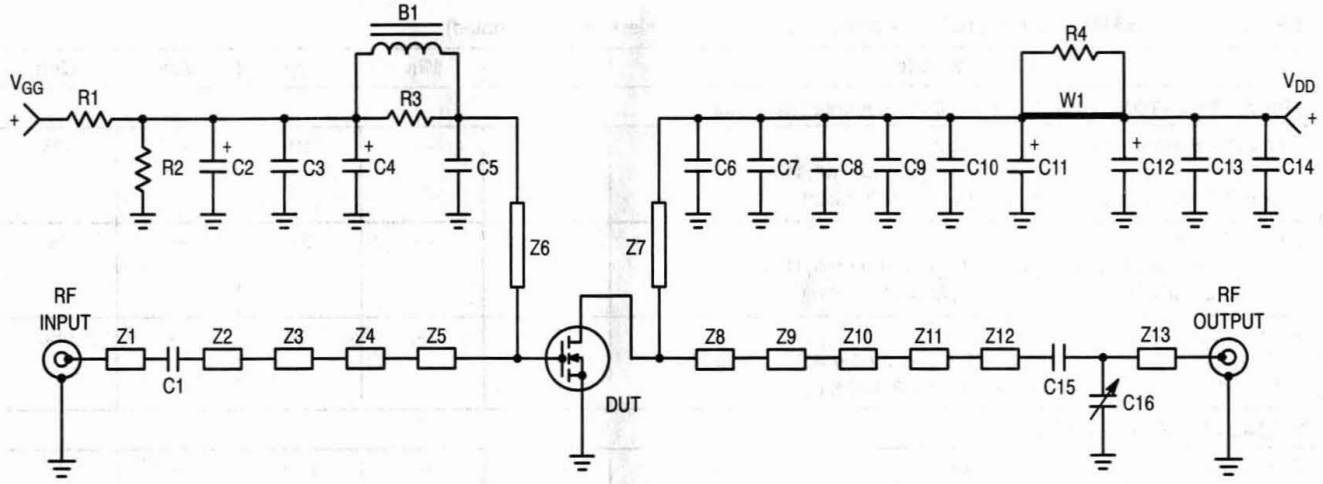
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	10.8	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 300 μA)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 1300 mA)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(on)}$	—	0.12	—	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	5.4	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth, IM3 measured in 3.84 MHz Bandwidth. Peak/Avg = 8.5 dB @ 0.01% probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	G_{ps}	12	13	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	η	17	18	—	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; IM3 measured at f1 –15 MHz and f2 +15 MHz referenced to carrier channel power.)	IM3	—	–43	–40	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; ACPR measured at f1 –10 MHz and f2 +10 MHz referenced to carrier channel power.)	ACPR	—	–45	–40	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 20 W Avg, 2–carrier W–CDMA, I_{DQ} = 1600 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	IRL	—	–12	–9.0	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 125 W CW, I_{DQ} = 1600 mA, f = 2170 MHz, VSWR = 5:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
TYPICAL TWO–TONE PERFORMANCE (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1600 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	G_{ps}	—	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1600 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	η	—	34	—	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 125 W PEP, I_{DQ} = 1600 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IMD	—	–30	—	dBc
TYPICAL CW PERFORMANCE					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W CW, I_{DQ} = 1600 mA, f1 = 2170.0 MHz)	G_{ps}	—	11.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W CW, I_{DQ} = 1600 mA, f = 2170.0 MHz)	η	—	46	—	%



Z1	1.212″ x 0.082″ Microstrip	Z9	0.179″ x 0.219″ Microstrip
Z2	0.236″ x 0.082″ Microstrip	Z10	0.100″ x 0.336″ Microstrip
Z3	0.086″ x 0.254″ Microstrip	Z11	0.534″ x 0.142″ Microstrip
Z4	0.357″ x 0.082″ Microstrip	Z12	0.089″ x 0.080″ Microstrip
Z5	0.274″ x 1.030″ Microstrip	Z13	0.620″ x 0.080″ Microstrip
Z6	0.466″ x 0.050″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z7	0.501″ x 0.050″ Microstrip		
Z8	0.600″ x 1.056″ Microstrip		

Figure 1. MRF21125 Test Circuit Schematic

Table 1. MRF21125 Test Circuit Component Designations and Values

Designators	Description
B1	Ferrite Bead (Square), Fair Rite #2743019447
C1	9.1 pF Chip Capacitor, B Case, ATC #100B9R1CCA500X
C2, C4, C11, C12	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T491X226K035AS4394
C3, C7	20000 pF Chip Capacitors, B Case, ATC #100B203JCA50X
C5, C14	5.1 pF Chip Capacitors, B Case, ATC #100B5R1CCA500X
C6	100000 pF Chip Capacitor, B Case, ATC #100B104JCA50X
C8	10000 pF Chip Capacitor, B Case, ATC #100B103JCA50X
C9	7.5 pF Chip Capacitor, B Case, ATC #100B7R5CCA500X
C10	1.2 pF Chip Capacitor, B Case, ATC #100B1R2CCA500X
C13	0.1 μF Chip Capacitor, Kemet #CDR33BX104AKWS
C15	16 pF Chip Capacitor, B Case, ATC #100B160KP500X
C16	0.6 – 4.5 pF Variable Capacitor, Johanson Gigatrim #27271SL
R1	1.0 kΩ, 1/8 W Chip Resistor
R2	560 kΩ, 1/8 W Chip Resistor
R3	4.7 Ω, 1/8 W Chip Resistor
R4	12 Ω, 1/8 W Chip Resistor
W1	Solid Copper Buss Wire, 16 AWG

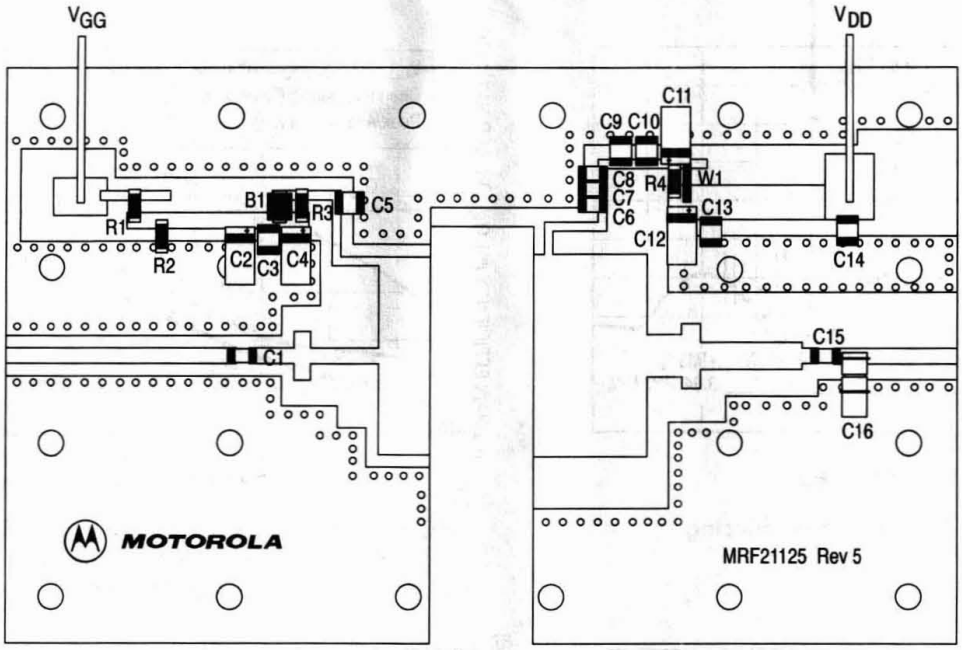


Figure 2. MRF21125 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

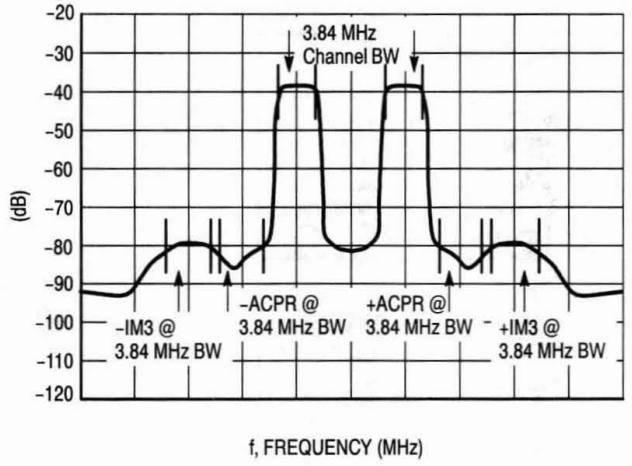


Figure 3. 2 Carrier (10 MHz spacing) W–CDMA Spectrum

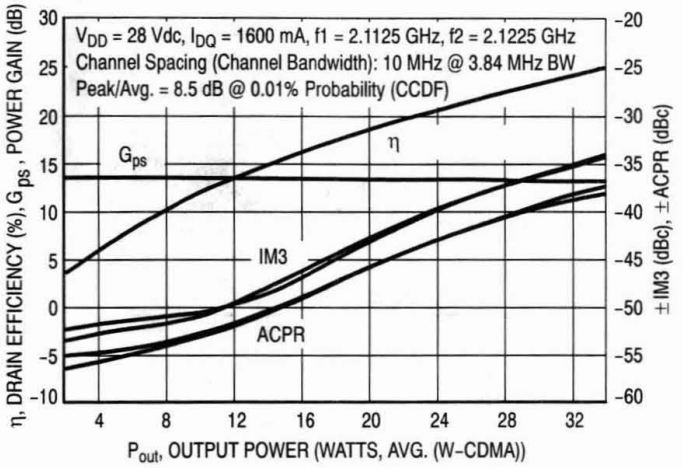


Figure 4. 2 Carrier W–CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

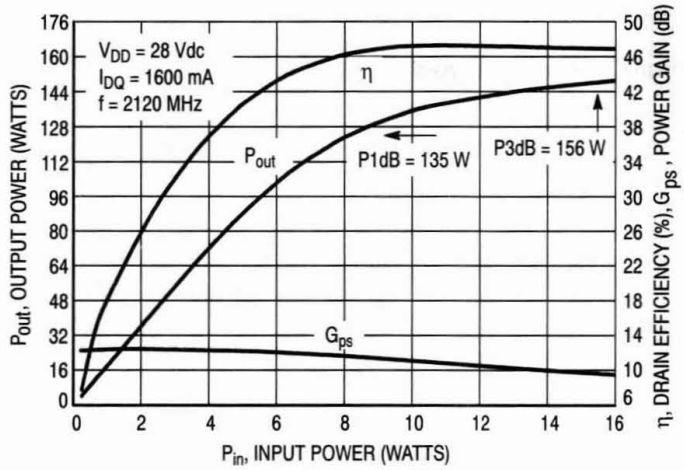


Figure 5. CW Performance

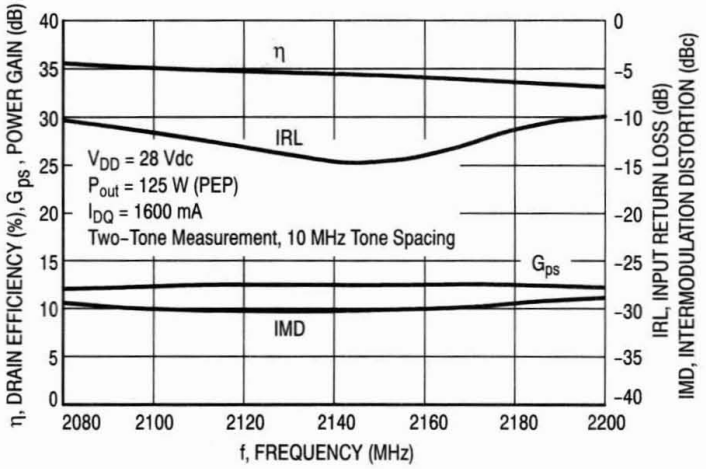


Figure 6. Broadband Linearity Performance

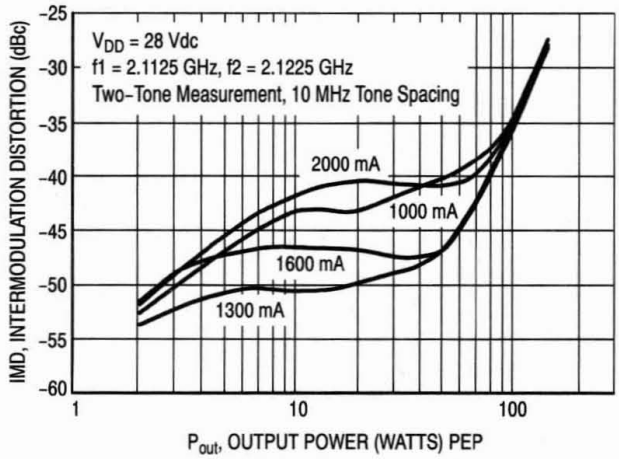


Figure 7. Intermodulation Distortion versus Output Power

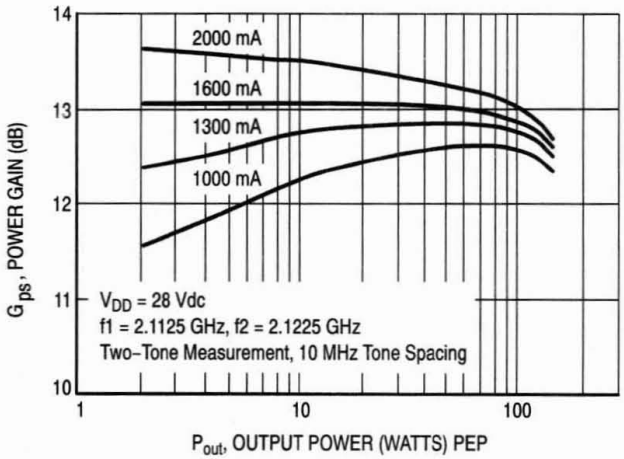
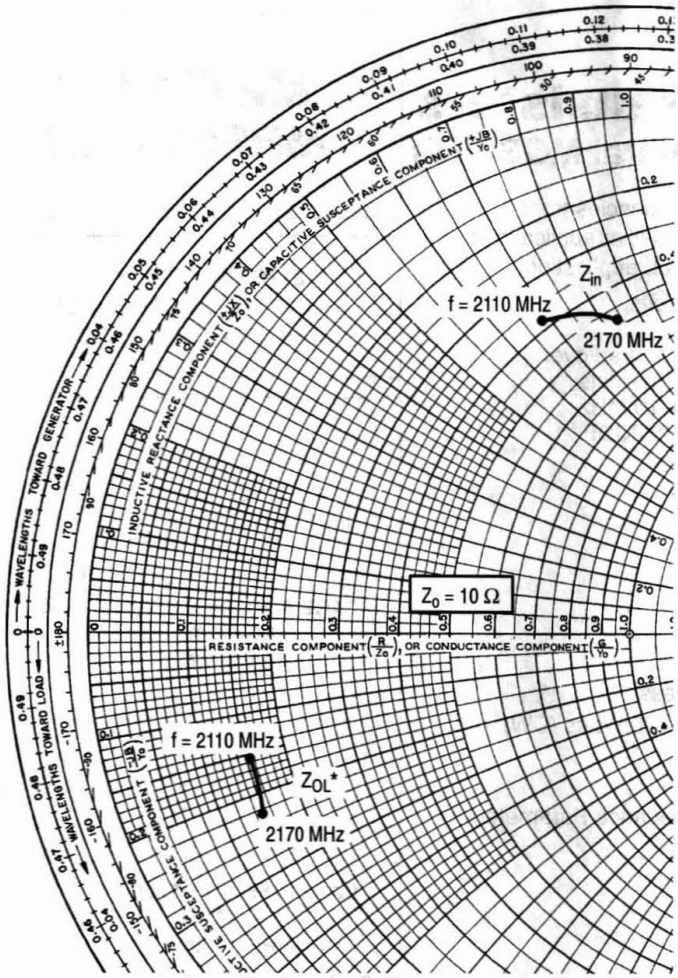


Figure 8. Power Gain versus Output Power



V_{DD} = 28 V, I_{DQ} = 1600 mA, P_{out} = 20 W (Avg.), 2-Carrier W-CDMA

f MHz	Z_{in} Ω	Z_{OL}^* Ω
2110	3.81 + j6.86	1.56 – j1.58
2140	4.33 + j7.90	1.53 – j1.90
2170	4.84 + j8.46	1.48 – j2.26

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note 1: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Note 2: Measurements were taken on the MRF21125 test circuit with SMA Launchers.

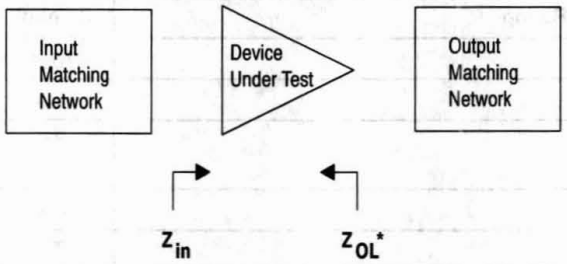


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub–Micron MOSFET Line

RF Power Field Effect Transistors

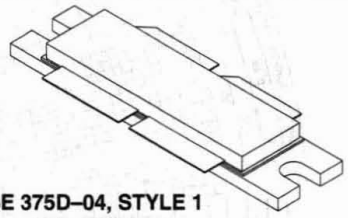
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21180
MRF21180S

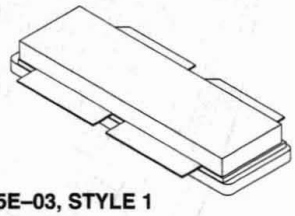
2170 MHz, 170 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Typical 2–carrier W–CDMA Performance for V_{DD} = 28 Volts, I_{DQ} = 2 x 850 mA, f1 = 2135 MHz, f2 = 2145 MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ f1 – 5 MHz and f2 + 5 MHz. Distortion Products Measured over a 3.84 MHz BW @ f1 – 10 MHz and f2 + 10 MHz, Each Carrier Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
  Output Power — 38 Watts (Avg.)
  Power Gain — 12.1 dB
  Efficiency — 22%
  IM3 — 37.5 dBc
  ACPR — –41 dBc
- Internally Input and Output Matched, for Ease of Use
- High Gain, High Efficiency, and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2110 MHz, 170 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 375D–04, STYLE 1
(NI–1230)
(MRF21180)



CASE 375E–03, STYLE 1
(NI–1230S)
(MRF21180S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	380 2.17	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.46	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 850 mAdc)	$V_{GS(Q)}$	3	3.9	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.18	0.22	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	6	—	S
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.6	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture) (2) 2–Carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers. Each carrier has Peak/Avg. ratio = 8.3 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	G_{ps}	11	12.1	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	η	19	22	—	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; IM3 measured over 3.84 MHz BW @ f1 –10 MHz and f2 +10 MHz)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; ACPR measured over 3.84 MHz BW @ f1 – 5 MHz and f2 +5 MHz.)	ACPR	—	–41	–39	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 170 W CW, I_{DQ} = 2 x 850 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Each side of device measured separately. Part is internally matched both on input and output.
(2) Measurements made with device in push–pull configuration.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture) (2) (continued)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 170 W, I_{DQ} = 2 x 850 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	G_{ps}	—	12	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 170 W, I_{DQ} = 2 x 850 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	η	—	33	—	%
Two–Tone Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 170 W, I_{DQ} = 2 x 850 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IMD	—	–30	—	dBc
Two–Tone Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 170 W, I_{DQ} = 2 x 850 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 28 Vdc, I_{DQ} = 2 x 850 mA, f = 2170 MHz)	P1dB	—	180	—	W

(2) Measurements made with device in push–pull configuration.

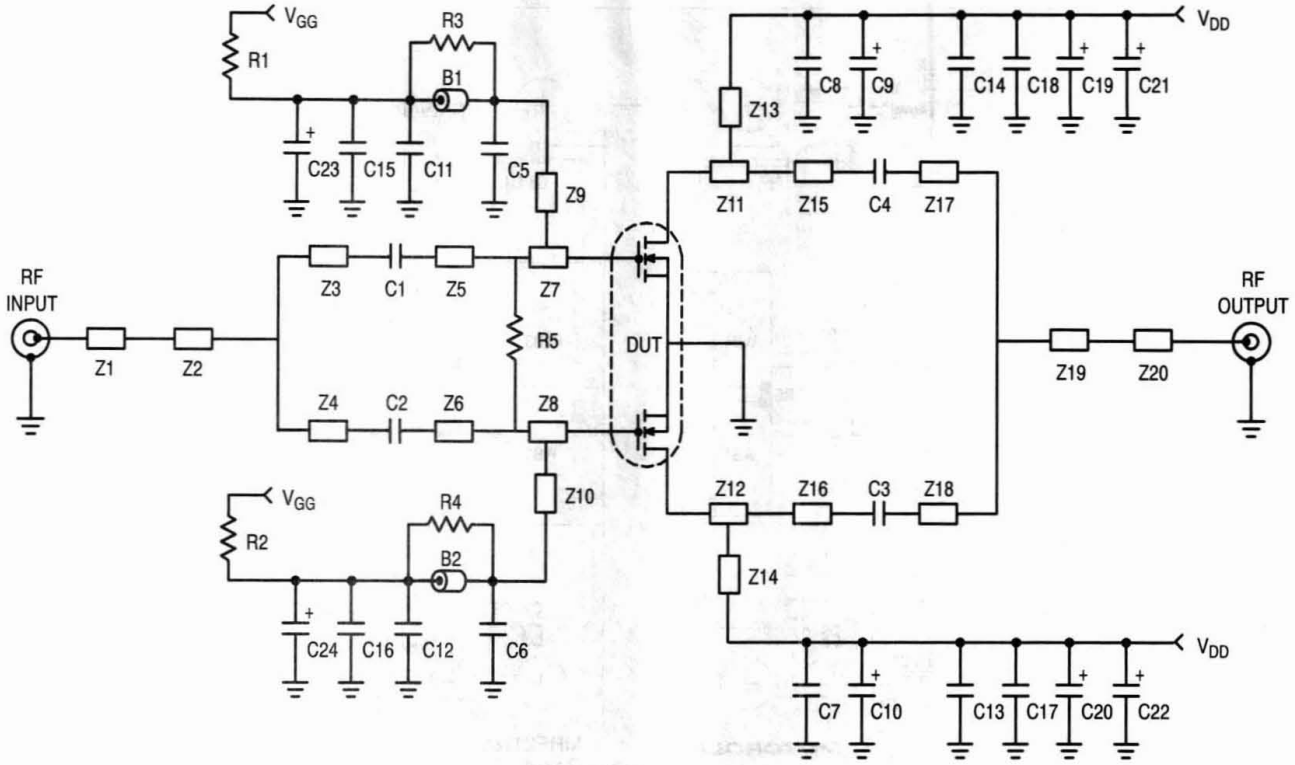


Figure 1. MRF21180 Test Circuit Schematic

Table 1. MRF21180 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1, B2	Short Ferrite Beads	2743019447	Fair Rite
C1, C2, C3, C4	30 pF Chip Capacitors	100B300JCA500X	ATC
C5, C6, C7, C8	5.6 pF Chip Capacitors	100B5R6JCA500X	ATC
C9, C10	10 μF Tantalum Capacitors	T495X106K035AS4394	Kemet
C11, C12, C13, C14	1000 pF Chip Capacitors	100B102JCA500X	ATC
C15, C16, C17, C18	0.1 μF Chip Capacitors	CDR33BX104AKWS	Kemet
C19, C20	1.0 μF Tantalum Capacitors	T491C105M050	Kemet
C21, C22, C23, C24	22 μF Tantalum Capacitors	T491X226K035AS4394	Kemet
N1, N2	Type N Flange Mounts	3052-1648-10	Omni Spectra
R1, R2, R3, R4	10 Ω, 1/8 W Chip Resistors		
R5	1.0 kΩ, 1/8 W Chip Resistor		
Z1, Z20	Microstrip	0.790″ x 0.065″	
Z2, Z19	Microstrip	0.830″ x 0.112″	
Z3, Z18	Microstrip	0.145″ x 0.065″	
Z4, Z17	Microstrip	1.700″ x 0.065″	
Z5, Z6	Microstrip	0.340″ x 0.065″	
Z7, Z8	Microstrip	0.455″ x 0.600″	
Z9, Z10	Microstrip	0.980″ x 0.035″	
Z11, Z12	Microstrip	0.510″ x 0.645″	
Z13, Z14	Microstrip	0.770″ x 0.058″	
Z15, Z16	Microstrip	0.280″ x 0.065″	
WB1, WB2, WB3, WB4	Wear Blocks		
Board	0.030″ Glass Teflon®	RF-35, ε_r = 3.50	Taconic
PCB	Etched Circuit Boards	MRF21180 Rev. 4	CMR

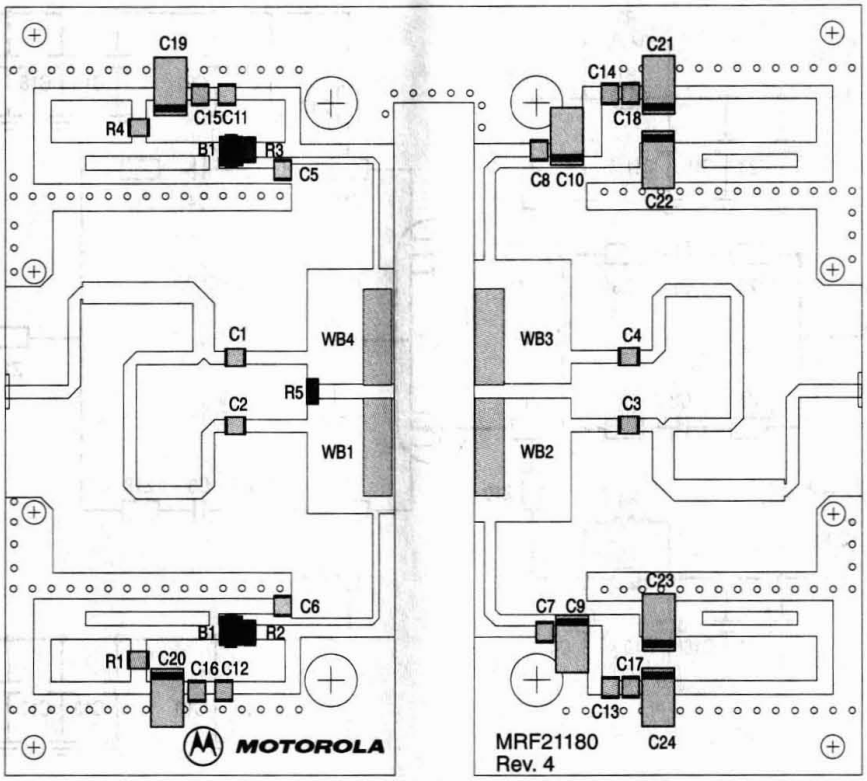


Figure 2. MRF21180 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

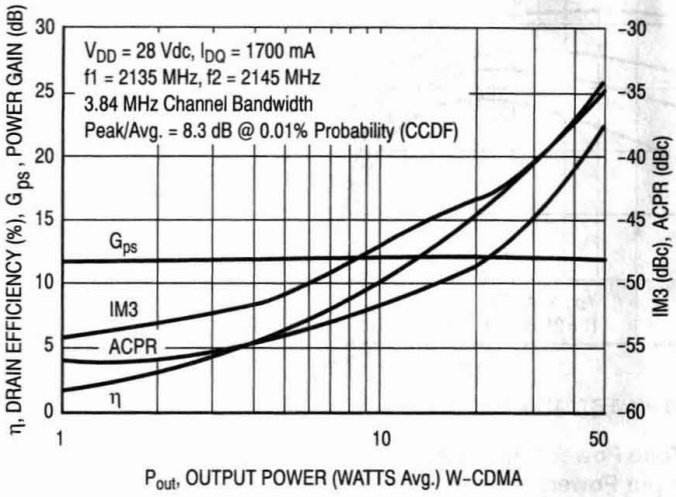


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

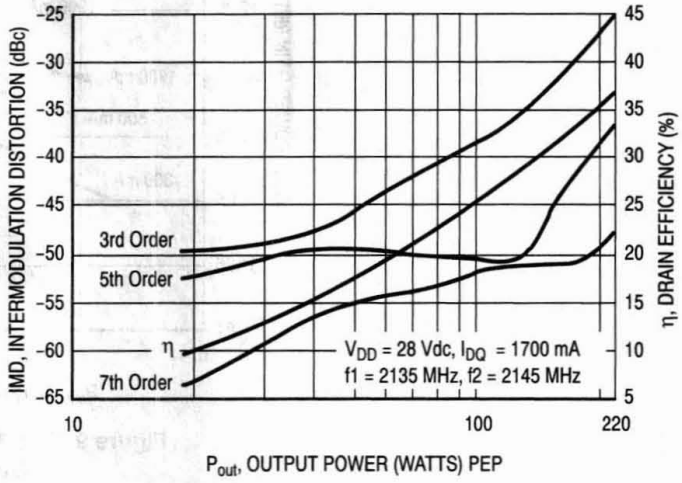


Figure 4. Intermodulation Distortion Products versus Output Power

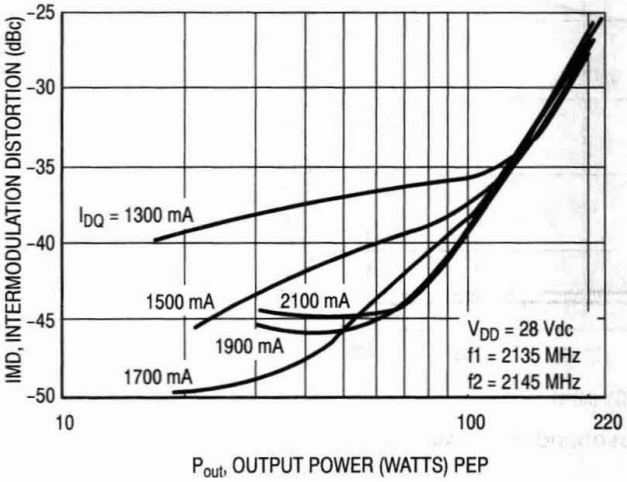


Figure 5. Intermodulation Distortion versus Output Power

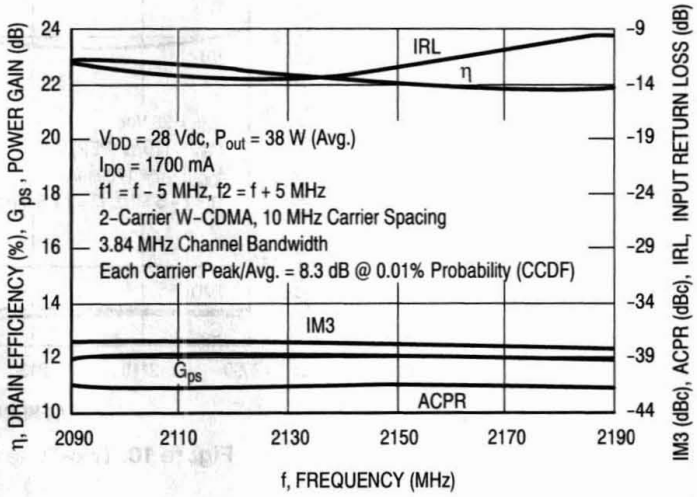


Figure 6. 2–Carrier W–CDMA Broadband Performance

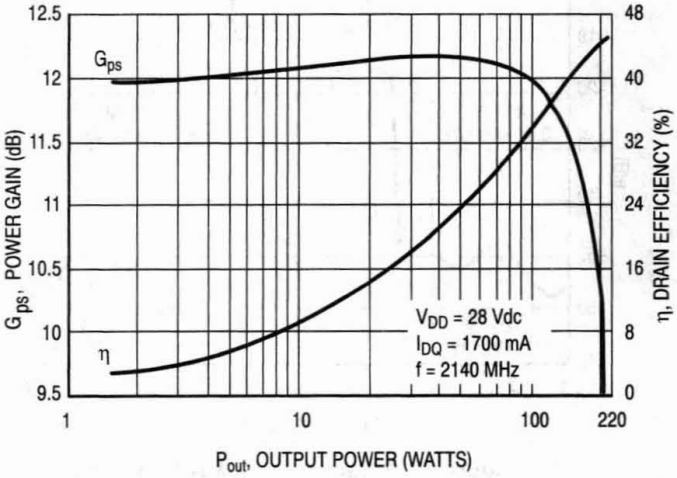


Figure 7. CW Performance

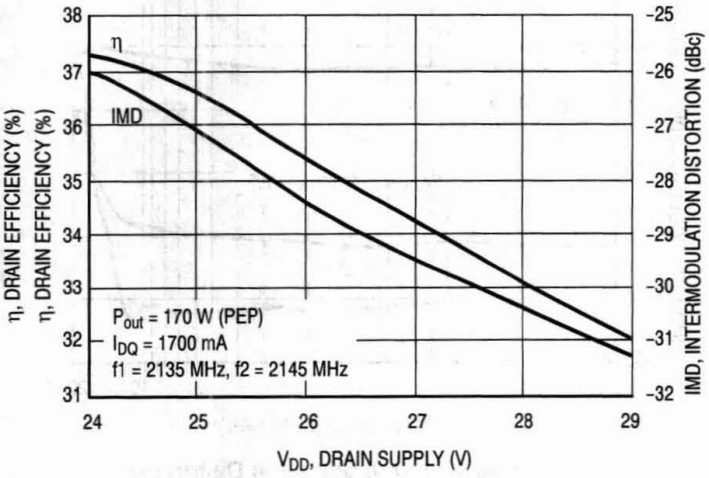


Figure 8. Two–Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

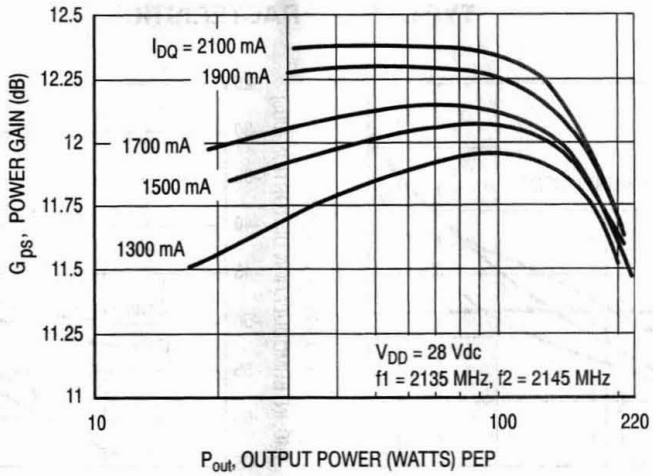


Figure 9. Two-Tone Power Gain versus Output Power

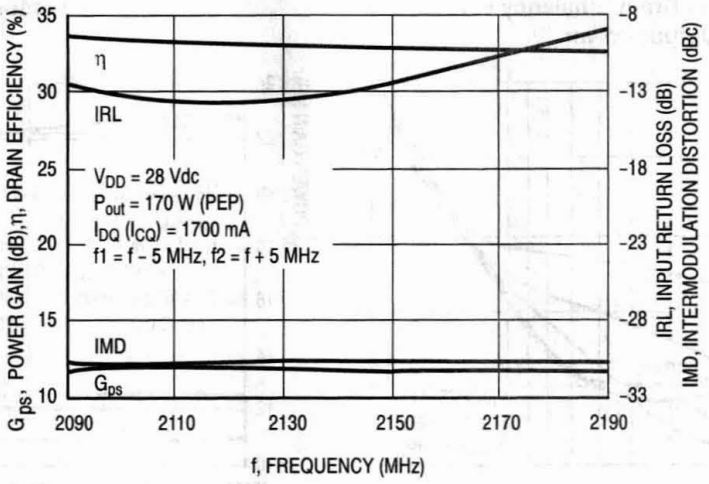


Figure 10. Two-Tone Broadband Performance

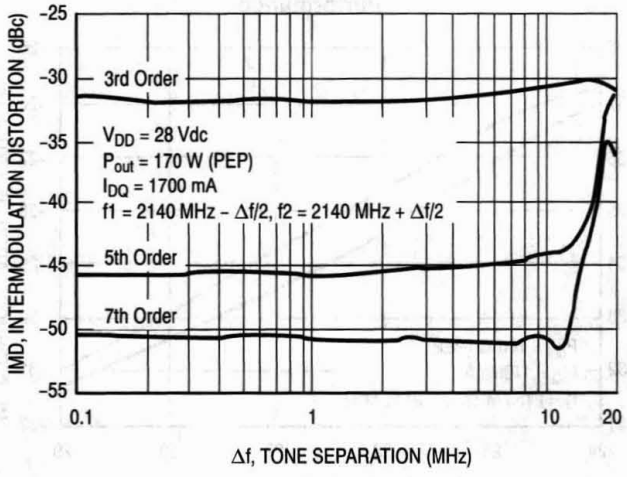


Figure 11. Intermodulation Distortion Products versus Two–Tone Spacing

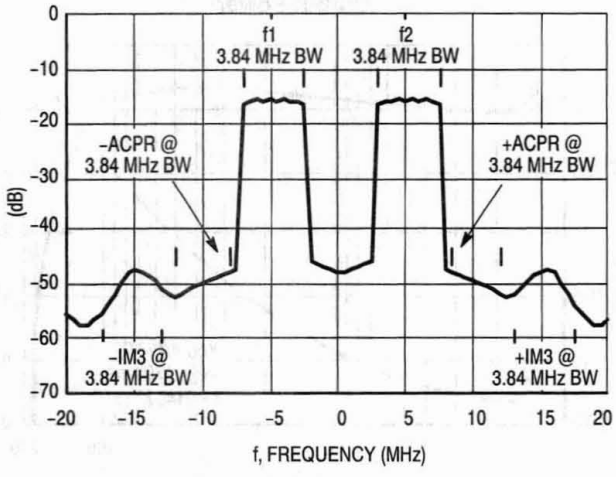
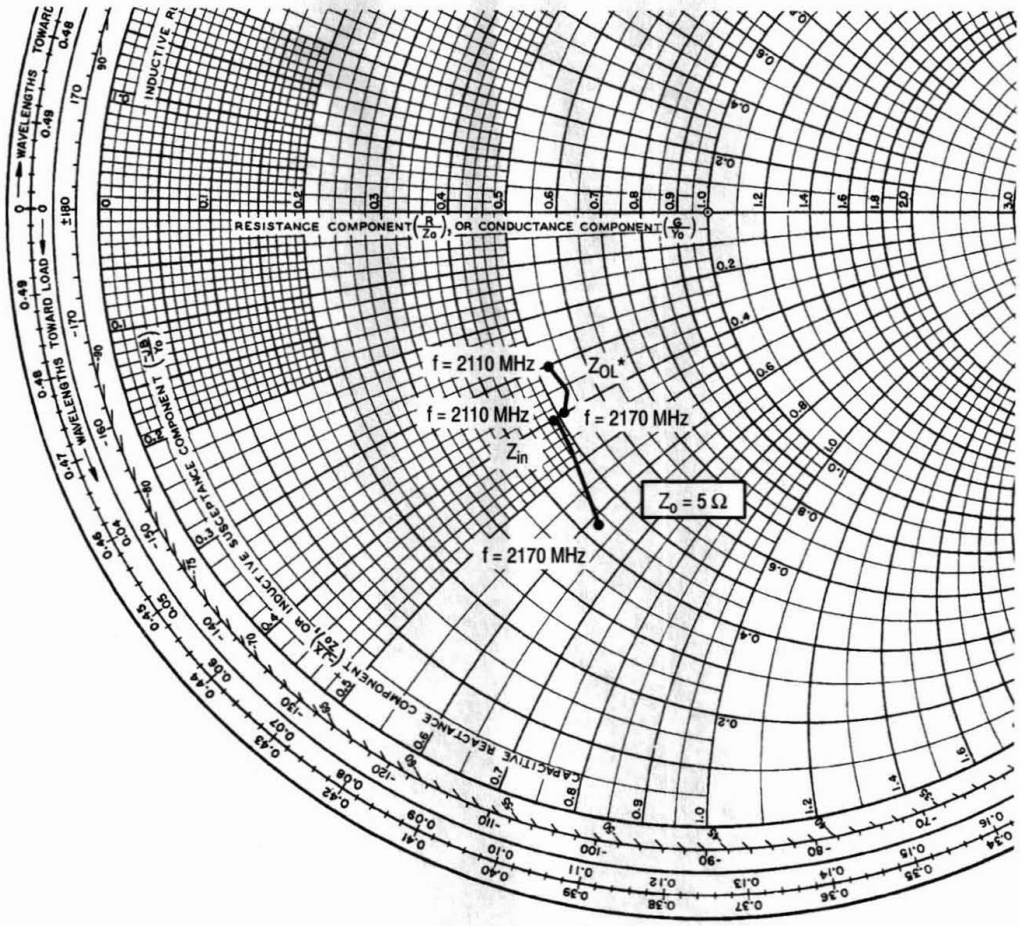


Figure 12. 2-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 2 X 850 mA, P_{out} = 38 W (Avg.)

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	2.45 – j2.08	2.65 – j1.52
2140	2.39 – j2.51	2.71 – j1.80
2170	2.16 – j3.14	2.64 – j2.04

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

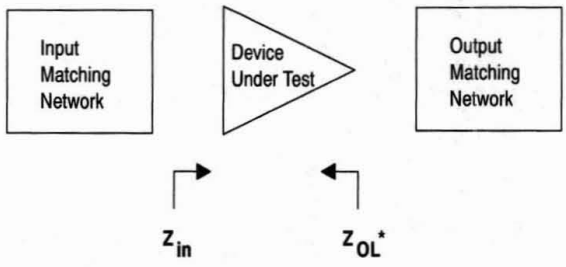


Figure 13. Series Equivalent Input and Output Impedance

Chapter Six
RF Amplifier Modules/ICs

Section One **6.1–0**
RF Amplifier Modules/ICs – Selector Guide

Section Two **6.2–0**
RF Amplifier Modules/ICs – Data Sheets

Section One
Selector Guide

Motorola RF Amplifier Modules/ICs

Motorola's RF portfolio includes many hybrid designs optimized to perform in narrowband base station transmitter applications. Motorola modules feature two or more active transistors (LDMOS or GaAs die technology) and their associated 50 ohm matching networks. Circuit substrate and metallization have been selected for optimum performance and reliability. For PA designers, hybrid modules offer the benefits of small and less complex system designs, in less time and at a lower overall cost.

Table of Contents

	Page
RF Amplifier Modules/ICs	6.1–1
Base Stations	6.1–2
Packages	6.1–3

Motorola RF Amplifier Modules/ICs

Complete amplifiers with 50 ohm input impedances are available for all popular base station transmitter systems, including GSM and CDMA, covering frequencies from 800 MHz up to 2.2 GHz.

Base Stations

Designed for applications such as macrocell drivers and microcell output stage, these class AB amplifiers are ideal for base station systems with power requirements up to 10 watts.

Table 1. Base Station Drivers

Product	Frequency MHz	P1dB Watts	Gain (Min) dB	Supply Voltage Volts	Class	System Application	Die Technology	Package/Style
MHVIC910HR2[18e]★	921–960	10	38	26	AB	GSM900	LDMOS–IC	978/–
MHW1810–1	1805–1880	10	24	26	AB	GSM1800	LDMOS	301AW/1
MHW1810–2	1805–1880	10	32	26	AB	GSM1800	LDMOS	301AW/1
MHW1910–1	1930–1990	10	24	26	AB	GSM1900	LDMOS	301AW/1
MHPA19010[46a]	1930–1990	10	24	28	AB	PCS1900	LDMOS	301AP/3
MHPA21010[46b]	2110–2170	10	24	28	AB	W–CDMA	LDMOS	301AP/3

Table 2. Base Station Pre–Drivers

These 50 ohm amplifiers are recommended for modern multi–tone CDMA, TDMA and UMTS base station pre–driver applications. Their high third–order intercept point, tight phase and gain control, and excellent group delay characteristics make these devices ideal for use in high–power feedforward loops.

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A (LDMOS Die) – Lateral MOSFETs

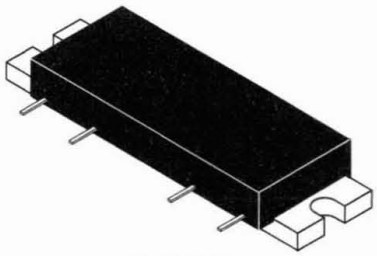
Product	Frequency Band MHz	V_{DD} (Nom.) Volts	I_{DD} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Pkg/ Style
MHL9838	800–925	28	770	31	.1	39	50	3.7	301AP/1
MHL9236	800–960	26	550	30.5	.1	34	47	3.5	301AP/1
MHL9236M	800–960	26	550	30.5	.1	34	47	3.5	301AP/2
MHL9318	860–900	28	500	17.5	.1	35.5	49	3.0	301AS/1
MHL18336★	1800–1900	26	500	30	.2	36	46	4.2	301AP/1
MHL18926★	1805–1880	26	1100	28.6	.3	40	50	4.2	301AY/1
MHL19338	1900–2000	28	500	30	.1	36	46	4.2	301AP/1
MHL19926★	1930–1990	26	1000	29.4	.3	40	50	4.2	301AY/1
MHL19936	1900–2000	26	1400	29	.2	41	49.5	4.2	301AY/1
MHL21336	2110–2170	26	500	31	.15	35	45	4.5	301AP/1

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units.

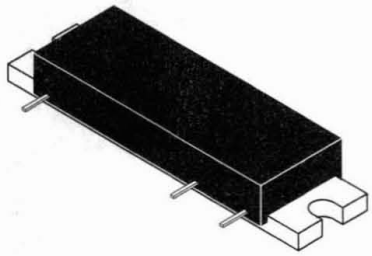
[46]To be introduced: a) 1Q02; b) 2Q02

★New Product

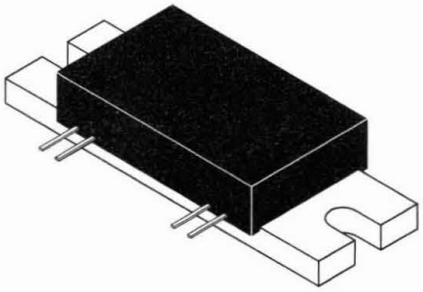
RF Amplifier Modules Packages



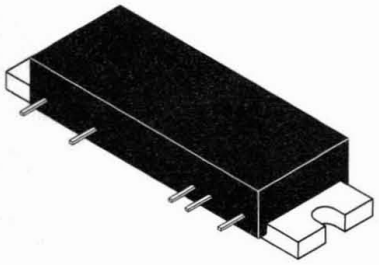
CASE 301AP
STYLE 1, 2, 3



CASE 301AS
STYLE 1



CASE 301AW
STYLE 1



CASE 301AY
STYLE 1

CASE 978
PLASTIC
(PFP–16)

SCALE 1:1

Section Two

Motorola RF Amplifier Modules/ICs – Data Sheets

Device Number	Page Number
MHL9236	6.2–3
MHL9236M	6.2–3
MHL9318	6.2–6
MHL9838	6.2–9
MHL18336	6.2–12
MHL18926	6.2–13
MHL19926	6.2–14
MHL19338	6.2–15
MHL19936	6.2–16
MHL21336	6.2–17
MHVIC910HR2	6.2–18
MHW1810–1	6.2–25
MHW1810–2	6.2–25
MHW1910–1	6.2–31

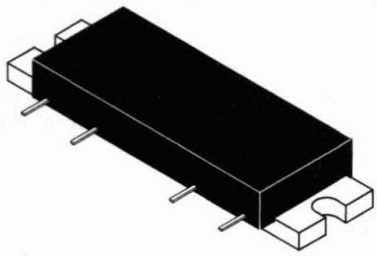
The RF Line
Cellular Band
RF Linear LDMOS Amplifiers

MHL9236
MHL9236M

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA, CDMA or QPSK.

- Third Order Intercept: 47 dBm Typ
- Power Gain: 30.5 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA, CDMA, QPSK or Analog Systems

800–960 MHz
2.5 W, 30.5 dB
RF LINEAR LDMOS AMPLIFIERS



CASE 301AP–02, STYLES 1, 2

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+10	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	550	620	mA
Power Gain	(f = 880 MHz)	G_p	29.5	30.5	31.5	dB
Gain Flatness	(f = 800–960 MHz)	G_F	—	0.1	0.3	dB
Power Output @ 1 dB Comp.	(f = 880 MHz)	P_{out} 1 dB	33.0	34.0	—	dBm
Input VSWR	(f = 800–960 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR	(f = 800–960 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	46.0	47.0	—	dBm
Noise Figure	(f = 800–960 MHz)	NF	—	3.5	4.5	dB

TYPICAL CHARACTERISTICS

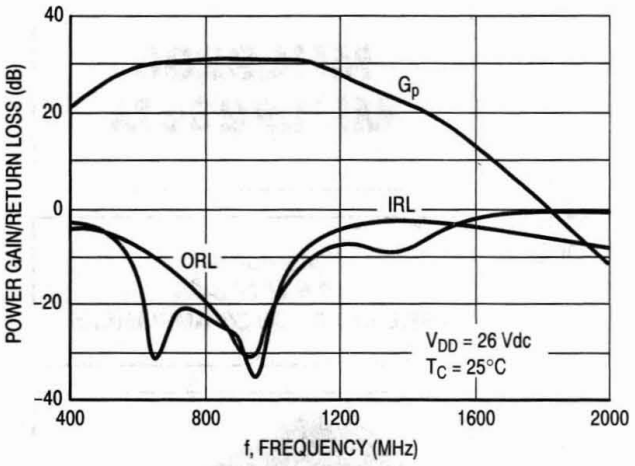


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

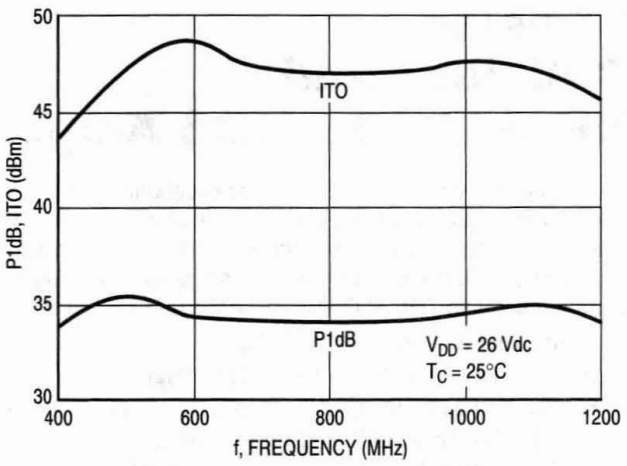


Figure 2. P1dB, ITO versus Frequency

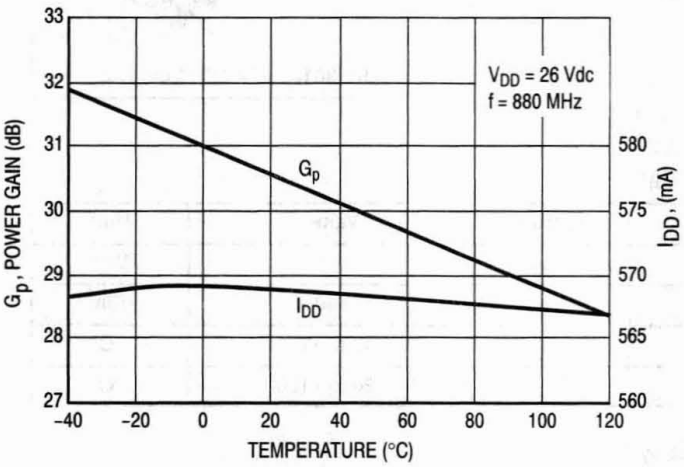


Figure 3. Power Gain, I_{DD} versus Temperature

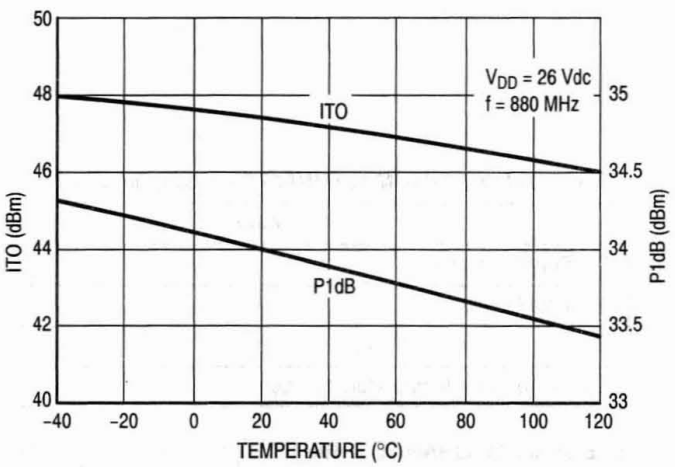


Figure 4. ITO, P1dB versus Temperature

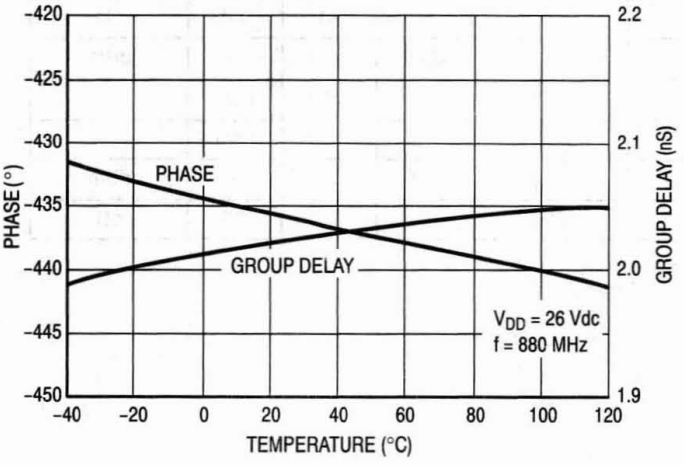


Figure 5. Phase(1), Group Delay(1) versus Temperature

(1)In Production Test Fixture

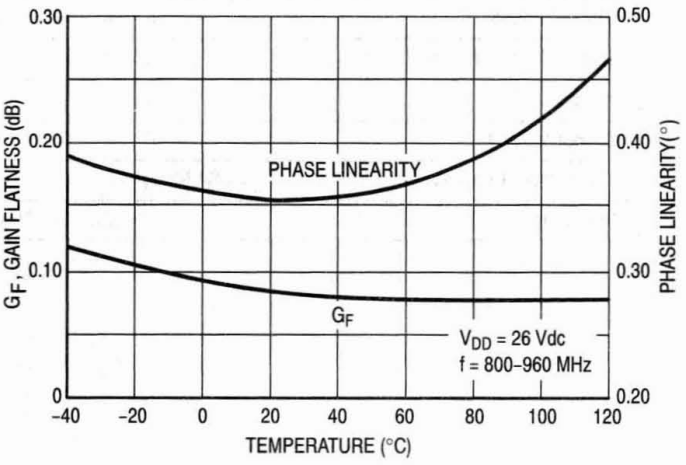


Figure 6. Gain Flatness, Phase Linearity versus Temperature

TYPICAL CHARACTERISTICS

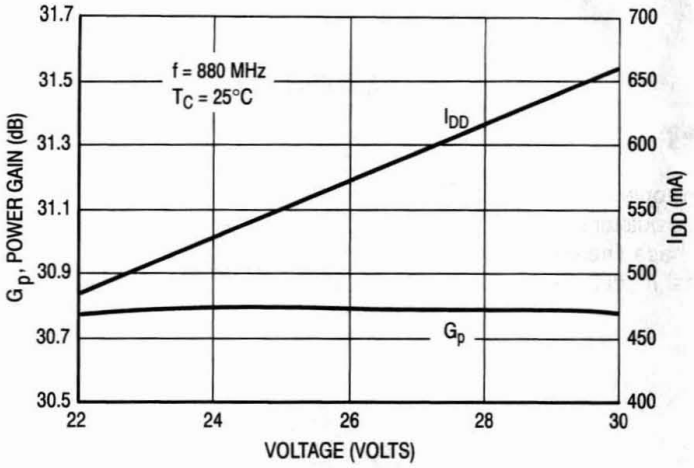


Figure 7. Power Gain, I_{DD} versus Voltage

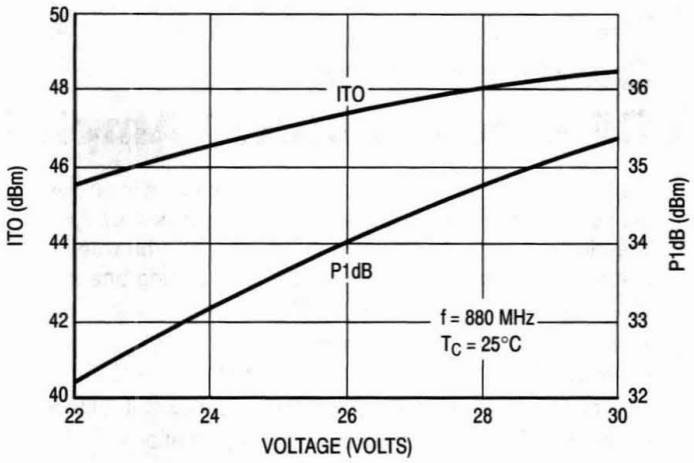


Figure 8. ITO, P1dB versus Voltage

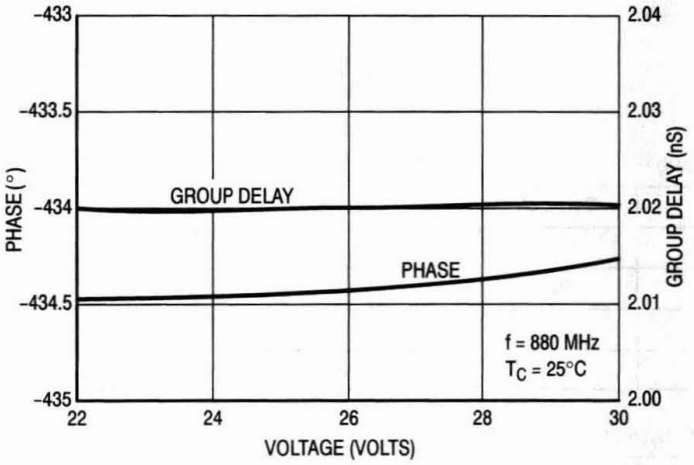


Figure 9. Phase(1), Group Delay(1) versus Voltage

(1)In Production Test Fixture

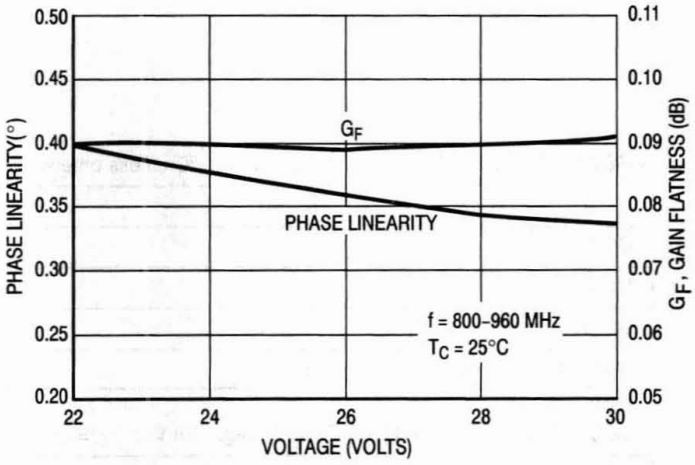


Figure 10. Phase Linearity, Gain Flatness versus Voltage

The RF Line

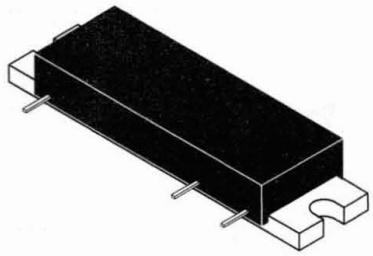
Cellular Band RF Linear LDMOS Amplifier

MHL9318

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 49 dBm Typ
- Power Gain: 17.5 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA and CDMA Multi–Carrier Applications

3.0 W, 17.5 dB
860–900 MHz
RF LINEAR LDMOS AMPLIFIER



CASE 301AS–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	500	560	mA
Power Gain	(f = 880 MHz)	G_p	17	17.5	18.5	dB
Gain Flatness	(f = 860–900 MHz)	G_F	—	0.1	0.2	dB
Power Output @ 1 dB Comp.	(f = 880 MHz)	P_{out} 1 dB	—	35.5	—	dBm
Input VSWR	(f = 860–900 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR	(f = 860–900 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	47	49	—	dBm
Noise Figure	(f = 960 MHz)	NF	—	3	4.5	dB

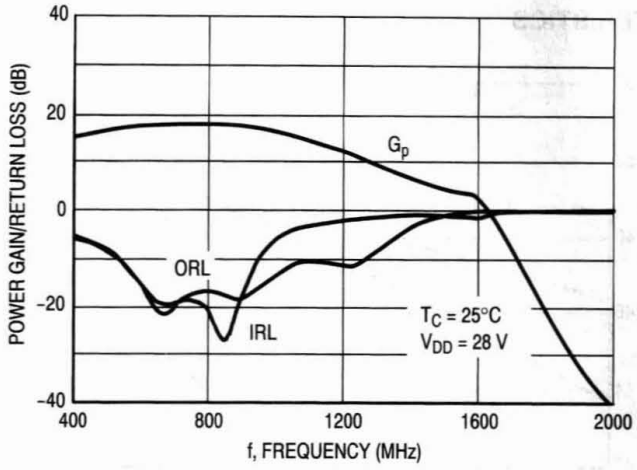


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

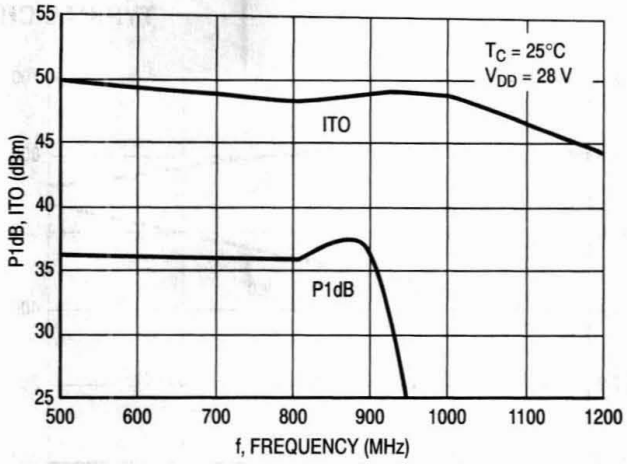


Figure 2. P1dB, ITO versus Frequency

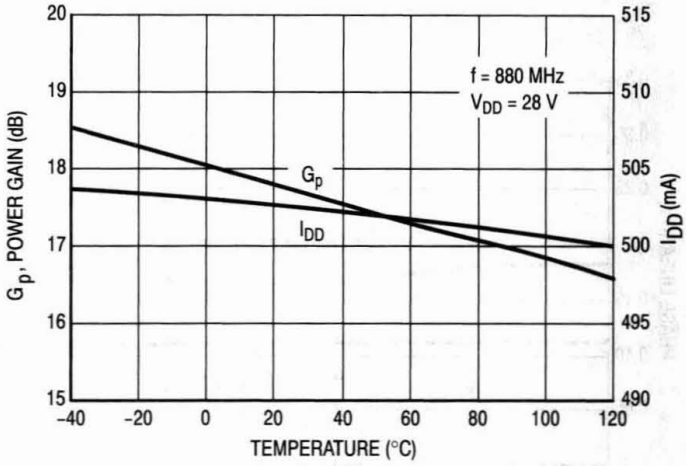


Figure 3. Power Gain, I_{DD} versus Temperature

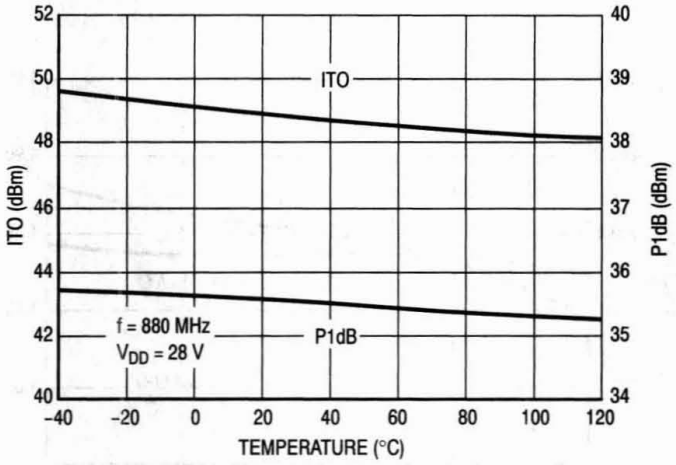


Figure 4. ITO, P1dB versus Temperature

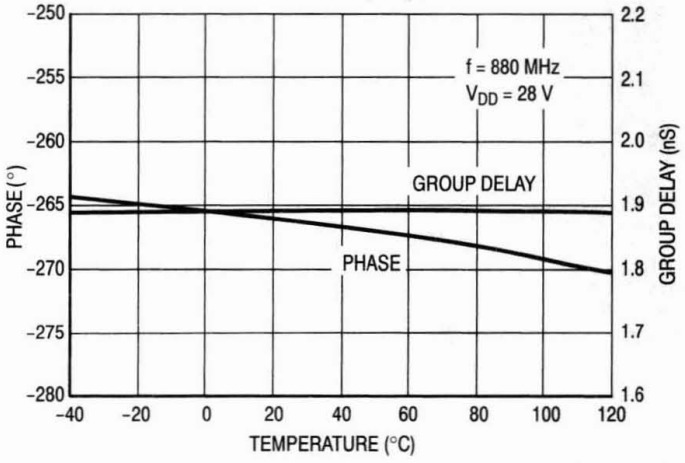


Figure 5. Phase(1), Group Delay(1) versus Temperature

(1)In Production Test Fixture

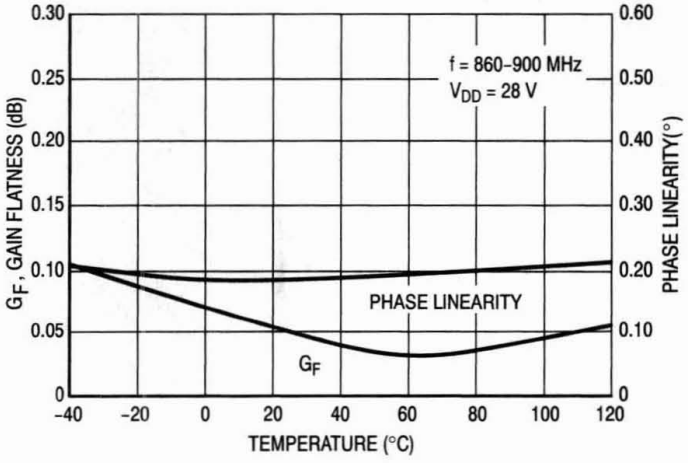


Figure 6. Gain Flatness, Phase Linearity versus Temperature

TYPICAL CHARACTERISTICS

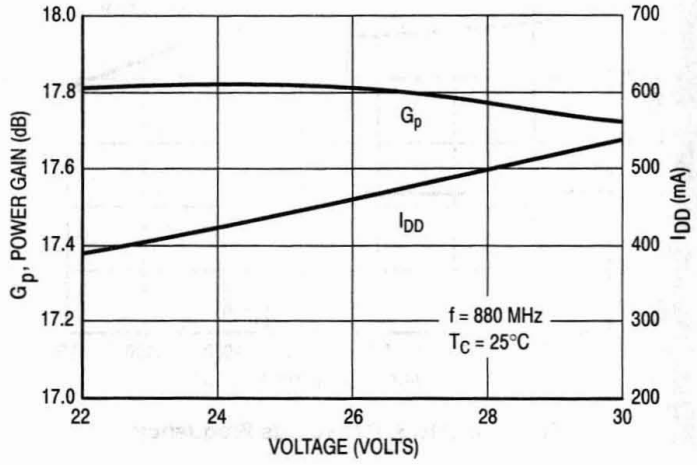


Figure 7. Power Gain, I_{DD} versus Voltage

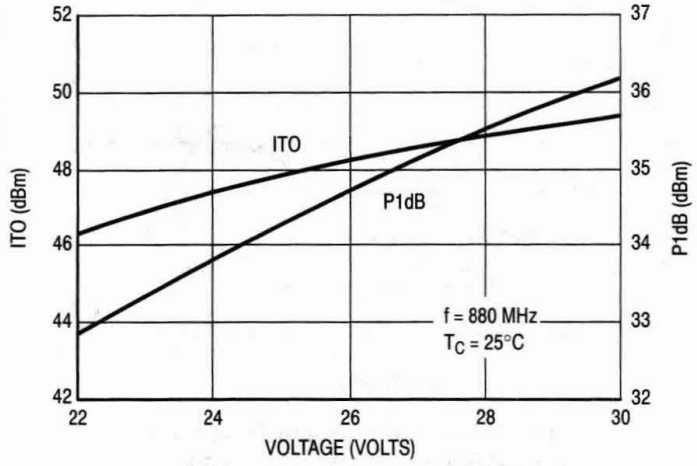


Figure 8. ITO, P1dB versus Voltage

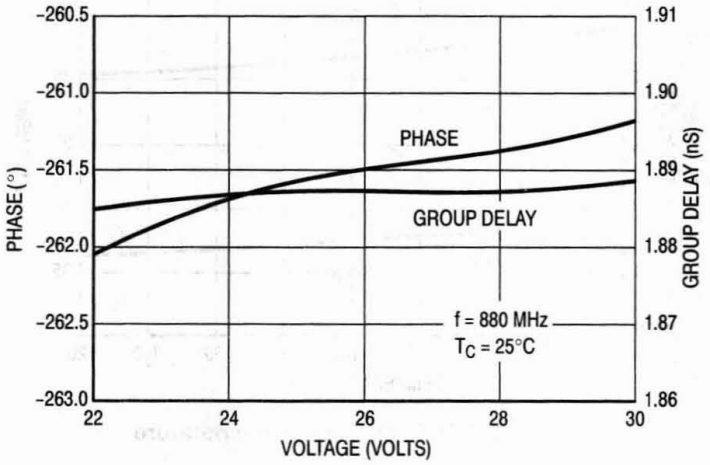


Figure 9. Phase(1), Group Delay(1) versus Voltage

(1)In Production Test Fixture

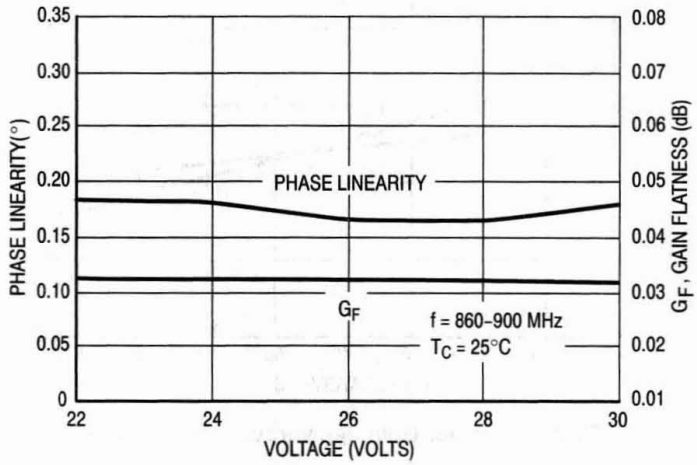


Figure 10. Phase Linearity, Gain Flatness versus Voltage

The RF Line

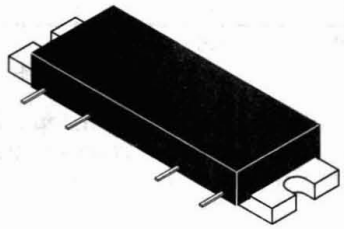
Cellular Band RF Linear LDMOS Amplifier

MHL9838

800–925 MHz
8.0 W, 31 dB
RF LINEAR LDMOS AMPLIFIER

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 50 dBm Typ
- Power Gain: 31 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA and CDMA Multi–Carrier Applications



CASE 301AP–02, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+6	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	770	800	mA
Power Gain	(f = 880 MHz)	G_p	30	31	32	dB
Gain Flatness	(f = 800–925 MHz)	G_F	—	0.1	0.3	dB
Power Output @ 1 dB Comp.	(f = 880 MHz)	P_{out} 1 dB	—	39	—	dBm
Input VSWR	(f = 800–925 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR	(f = 800–925 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	49	50	—	dBm
Noise Figure	(f = 925 MHz)	NF	—	3.7	4.5	dB

TYPICAL CHARACTERISTICS

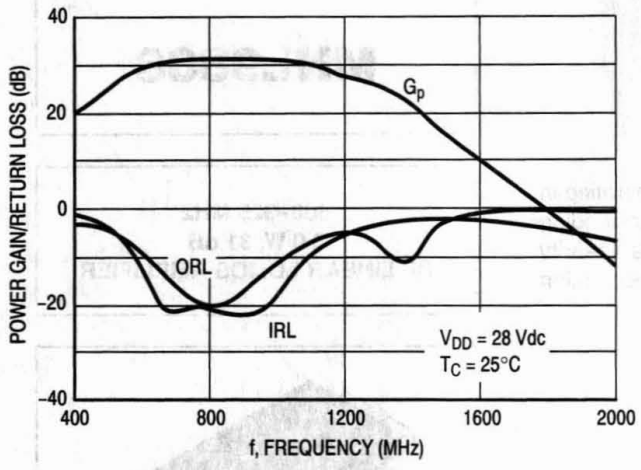


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

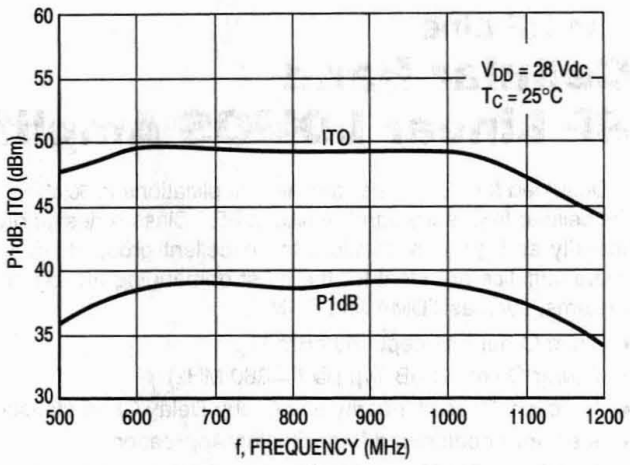


Figure 2. P1dB, ITO versus Frequency

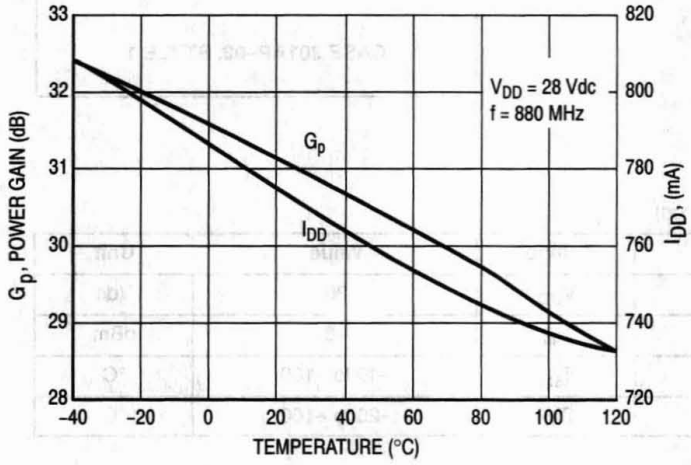


Figure 3. Power Gain, I_{DD} versus Temperature

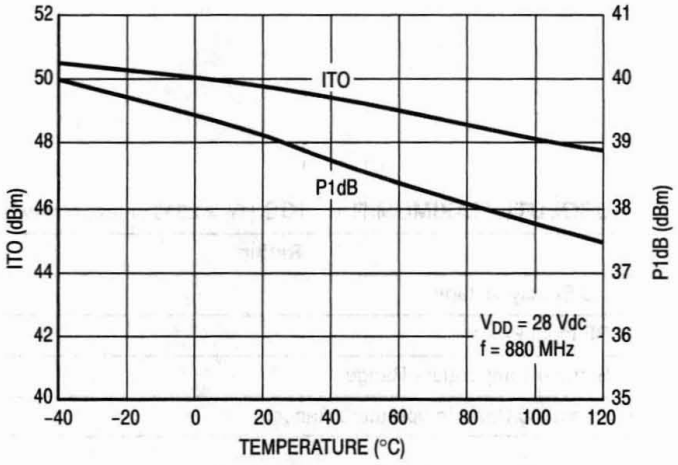


Figure 4. ITO, P1dB versus Temperature

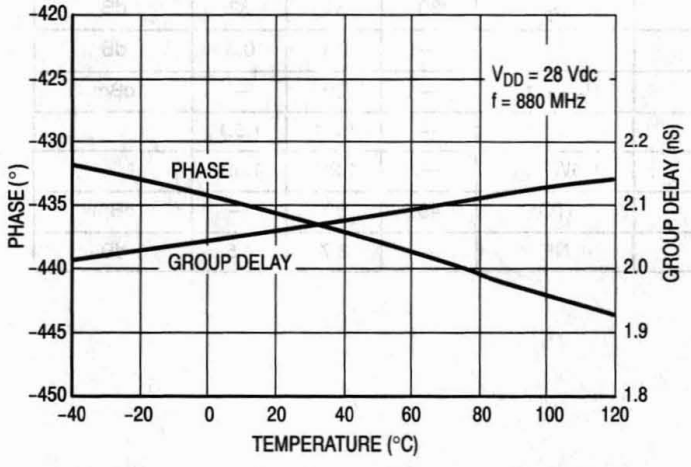


Figure 5. Phase(1), Group Delay(1) versus Temperature

(1)In Production Test Fixture

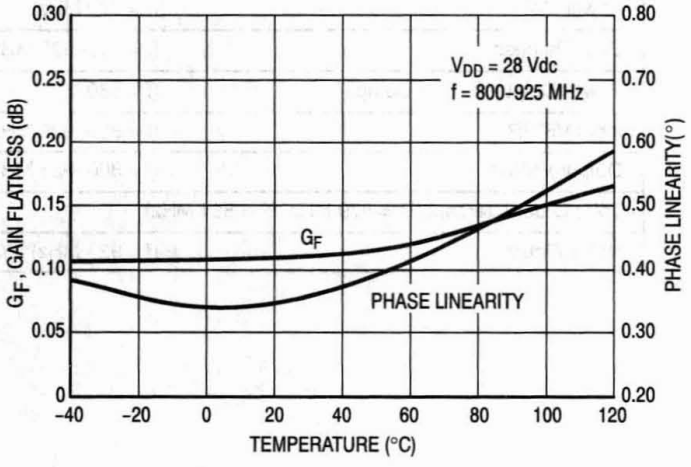


Figure 6. Gain Flatness, Phase Linearity versus Temperature

TYPICAL CHARACTERISTICS

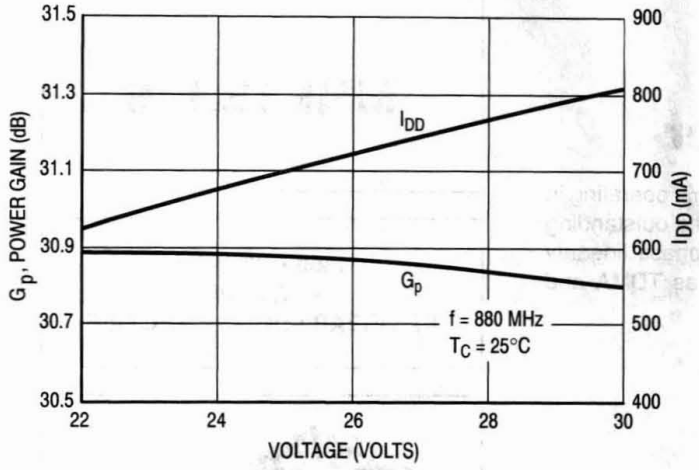


Figure 7. Power Gain, I_{DD} versus Voltage

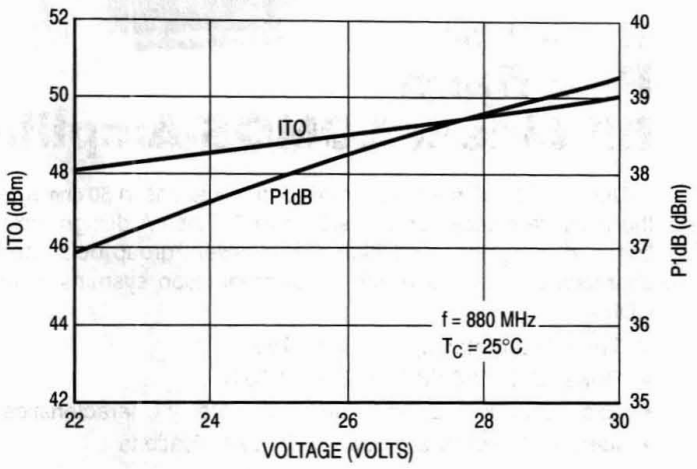


Figure 8. ITO, P1dB versus Voltage

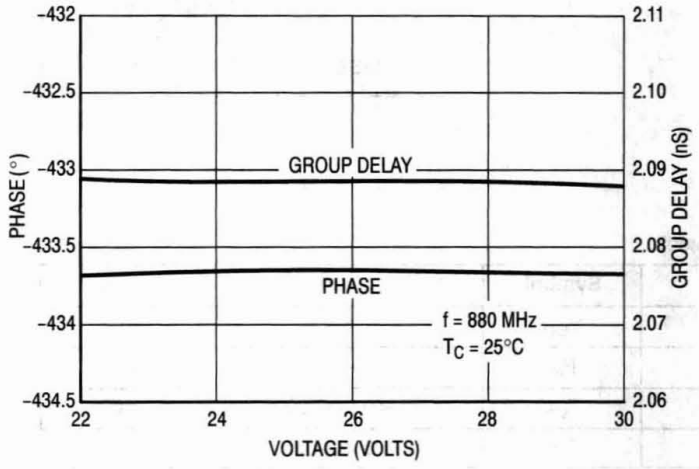


Figure 9. Phase[1], Group Delay[1] versus Voltage

[1]In Production Test Fixture

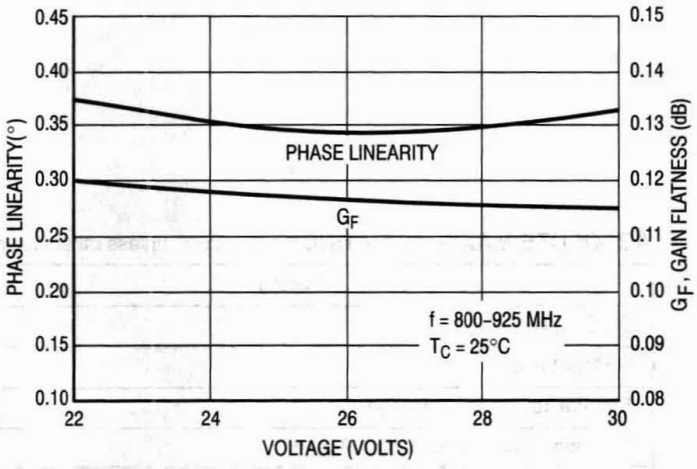


Figure 10. Phase Linearity, Gain Flatness versus Voltage

The RF Line

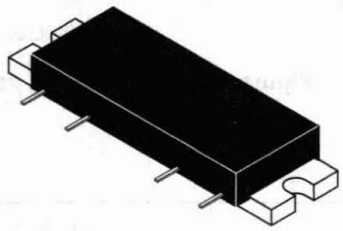
PCS Band RF Linear LDMOS Amplifier

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 46 dBm Typ
- Power Gain: 30 dB Typ (@ f =1850 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

MHL18336

1800–1900 MHz
4 W, 30 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AP–02, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+10	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	500	525	mA
Power Gain	(f =1850 MHz)	G_p	29	30	31	dB
Gain Flatness	(f = 1800–1900 MHz)	G_F	—	0.2	0.4	dB
Power Output @ 1 dB Comp.	(f = 1850 MHz)	P_{out} 1 dB	35	36	—	dBm
Input VSWR	(f = 1800–1900 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1847 MHz, f2 = 1852 MHz)		ITO	45	46	—	dBm
Noise Figure	(f = 1850 MHz)	NF	—	4.2	4.5	dB

The RF Line

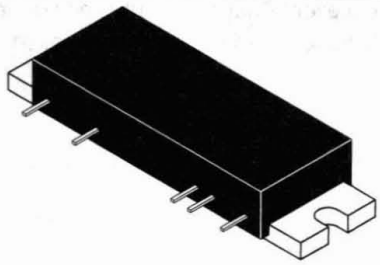
PCS Band RF Linear LDMOS Amplifier

Designed for ultra–linear amplifier applications in 50 Ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA, EDGE and CDMA.

- Third Order Intercept Point: 50 dBm Typ
- Power Gain: 28.6 dB Typ (@ f = 1842 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Application

MHL18926

1805–1880 MHz, 10 W, 28.6 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AY–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+7	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C; V_{DD} = 26 Vdc; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	1.1	1.15	A
Power Gain	(f = 1842 MHz)	G_p	27.6	28.6	29.6	dB
Gain Flatness	(f = 1805–1880 MHz)	G_F	—	0.3	0.5	dB
Power Output @ 1 dB Compression	(f = 1842 MHz)	P1 dB	39	40	—	dBm
Input VSWR	(f = 1805–1880 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept	(f1 =1839 MHz, f2=1844 MHz)	ITO	49.5	50	—	dBm
Noise Figure	(f = 1880 MHz)	NF	—	4.2	5	dB

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

The RF Line

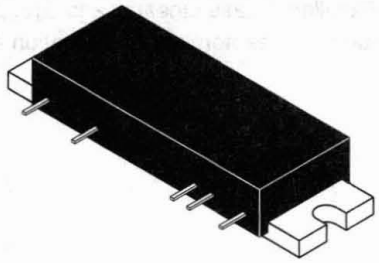
PCS Band RF Linear LDMOS Amplifier

Designed for ultra–linear amplifier applications in 50 Ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA, EDGE and CDMA.

- Third Order Intercept Point: 50 dBm Typ
- Power Gain: 29.4 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Application

MHL19926

1930–1990 MHz, 10 W, 29.4 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AY–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+7	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C; V_{DD} = 26 Vdc; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	1	1.05	A
Power Gain	(f = 1960 MHz)	G_p	28.4	29.4	30.4	dB
Gain Flatness	(f = 1930–1990 MHz)	G_F	—	0.3	0.5	dB
Power Output @ 1 dB Compression	(f = 1960 MHz)	P1 dB	39	40	—	dBm
Input VSWR	(f = 1930–1990 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept	(f1 =1957 MHz, f2=1962 MHz)	ITO	49.5	50	—	dBm
Noise Figure	(f = 1990 MHz)	NF	—	4.2	5	dB

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

The RF Line

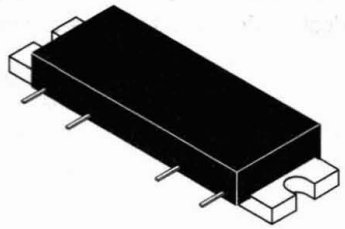
PCS Band RF Linear LDMOS Amplifier

MHL19338

1900–2000 MHz
4.0 W, 30 dB
RF LINEAR LDMOS AMPLIFIER

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 46 dBm Typ
- Power Gain: 30 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications



CASE 301AP–02, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+10	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	500	525	mA
Power Gain	(f = 1960 MHz)	G_p	29	30	31	dB
Gain Flatness	(f = 1900–2000 MHz)	G_F	—	0.1	0.4	dB
Power Output @ 1 dB Comp.	(f = 1950 MHz)	P_{out} 1 dB	35	36	—	dBm
Input VSWR	(f = 1900–2000 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1950 MHz, f2 = 1955 MHz)		ITO	45	46	—	dBm
Noise Figure	(f = 2000 MHz)	NF	—	4.2	4.5	dB

The RF Line

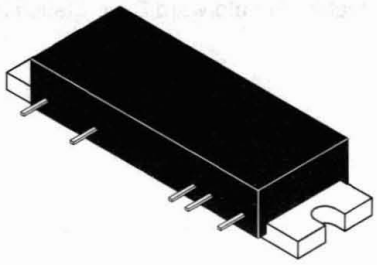
PCS Band RF Linear LDMOS Amplifier

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 49.5 dBm Typ
- Power Gain: 29 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

MHL19936

1900–2000 MHz
12 W, 29 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AY–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+10	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	1.4	1.45	A
Power Gain	(f = 1960 MHz)	G_p	28	29	30	dB
Gain Flatness	(f = 1900–2000 MHz)	G_F	—	0.2	0.4	dB
Power Output @ 1 dB Comp.	(f = 1950 MHz)	P_{out} 1 dB	40	41	—	dBm
Input VSWR	(f = 1900–2000 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept	(f1 = 1950 MHz, f2 = 1955 MHz)	ITO	49	49.5	—	dBm
Noise Figure	(f = 2000 MHz)	NF	—	4.2	4.5	dB

The RF Line

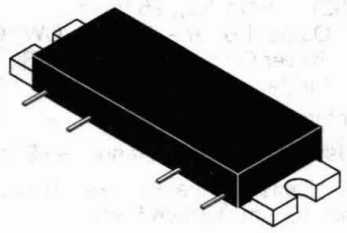
3G Band RF Linear LDMOS Amplifier

MHL21336

2110–2170 MHz
3.0 W, 31 dB
RF LINEAR LDMOS AMPLIFIER

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the 3G frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital CDMA modulation systems.

- Third Order Intercept: 45 dBm Typ
- Power Gain: 31 dB Typ (@ f = 2140 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications



CASE 301AP–02, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+5	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	500	525	mA
Power Gain	(f = 2140 MHz)	G_p	30	31	32	dB
Gain Flatness	(f = 2110–2170 MHz)	G_F	—	0.15	0.4	dB
Power Output @ 1 dB Comp.	(f = 2140 MHz)	P_{out} 1 dB	34	35	—	dBm
Input VSWR	(f = 2110–2170 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 2137 MHz, f2 = 2142 MHz)		ITO	44	45	—	dBm
Noise Figure	(f = 2170 MHz)	NF	—	4.5	5	dB

The RF Line

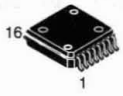
921 MHz - 960 MHz SiFET RF Integrated Power Amplifier

MHVIC910HR2

The MHVIC910HR2 integrated circuit is designed for GSM base stations, uses Motorola's newest High Voltage (26 Volts) LDMOS IC technology, and contains a three–stage amplifier. Target applications include macrocell (driver function) and microcell base stations (final stage). The device is packaged in a PFP–16 Power Flat Pack package which gives excellent thermal performances through a solderable backside contact.

- Typical GSM Performance @ Full Frequency Band (921 – 960 MHz), 26 Volts
  Output Power – 40 dBm (CW) @ P1dB
  Power Gain – 39 dB @ P1dB
  Efficiency – 48% @ P1dB
- Integrated ESD Protection
- Usable Frequency Range – 921 to 960 MHz
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

960 MHz, 10 W, 26 V
GSM CELLULAR
RF LDMOS INTEGRATED CIRCUIT



CASE 978–03
(PFP–16)

MAXIMUM RATINGS

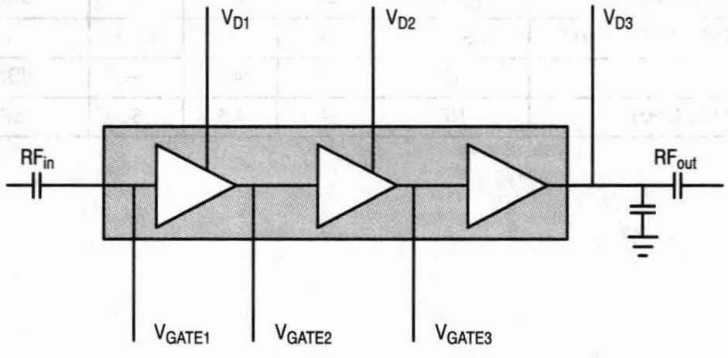
Rating	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	28	Vdc
Gate Supply Voltage	V_{GS}	6	Vdc
RF Input Power	P_{in}	5	dBm
Case Operating Temperature	T_C	– 30 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Operating Channel Temperature	T_{ch}	150	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	0 (Minimum)
Machine Model	M2 (Minimum)

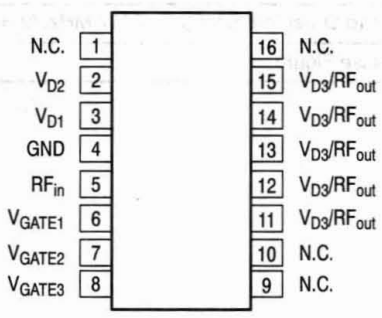
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.9	°C/W



Functional Block Diagram

PIN CONNECTIONS



(Top View)

NOTE: MHVIC910HR2 Moisture Sensitivity Level (MSL) = 3.

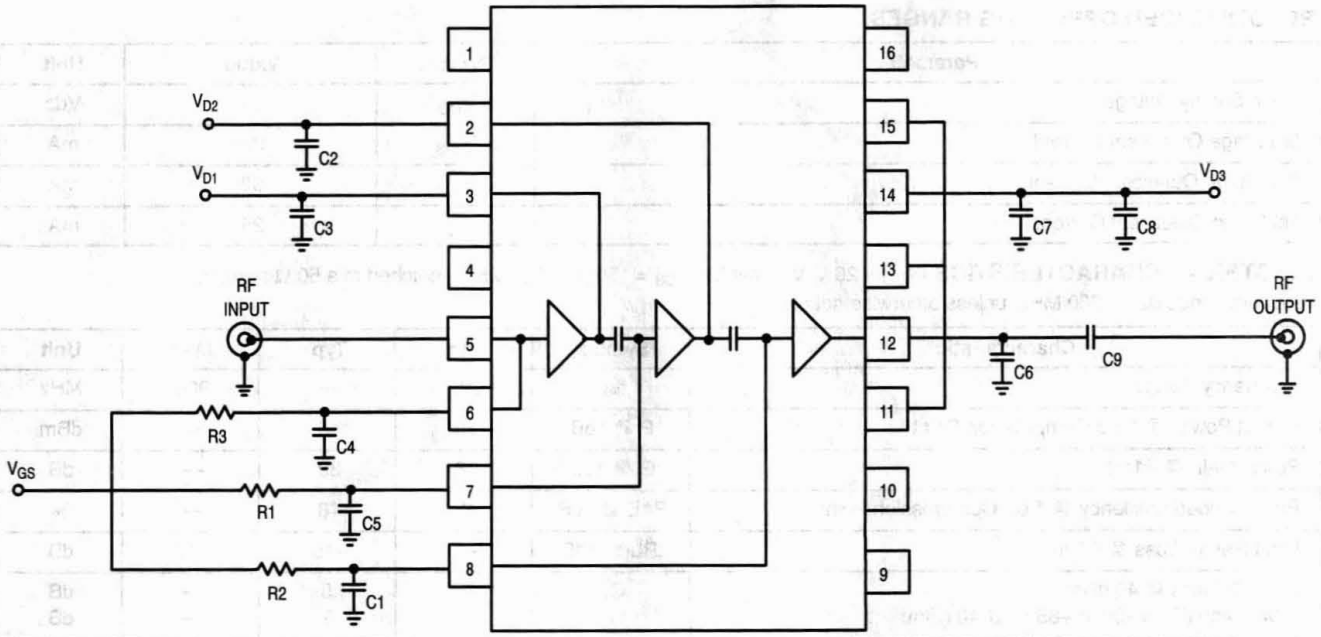
REV 3

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	26	Vdc
3rd Stage Quiescent Current	I_{DQ3}	150	mA
2nd Stage Quiescent Current	I_{DQ2}	50	mA
1st Stage Quiescent Current	I_{DQ1}	25	mA

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 V, V_{GS} set for I_{DQ3} = 150 mA, T_A = 25°C matched to a 50 Ω system, frequency range 921 – 960 MHz, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	f_{RF}	921	—	960	MHz
Output Power @ 1 dB Compression Point	P @ 1dB	39	40	—	dBm
Power Gain @ P1dB	G @ 1dB	38	39	—	dB
Power Added Efficiency @ 1 dB Compression Point	PAE @ 1dB	43	48	—	%
Input Return Loss @ P1dB	IRL @ 1dB	—	–15	–10	dB
Gain Flatness @ 40 dBm Variation (T_C = –30 to +85°C @ 40 dBm)	G_F G_V	— —	.5 5	— —	dB dB
Load Stability (V_{DS} = 24 V to 28 V, P_{out} = P1dB Down to 0 dBm, All Phase Angles)	VSWR	10:1	—	—	—
Ruggedness (V_{DS} = 26 V, P_{out} = 42 dBm, Load VSWR = 10:1, All Phase Angles)	Ψ	No Damage After Test			



C1, C2, C3, C4, C5, C8	1 µF Surface Mount Chip Capacitors	J1, J2	Header (Break-away), HDR2X10STIMCSAFU
C6	4.7 pF AVX Chip Capacitor, ACCU-P (08051J4R7BBT)	J3, J4	SMA Connector 2052-1618-02 (Threaded)
C7	47 pF AVX Chip Capacitor, ACCU-P (08055K470JBTTR)	R1, R2, R3	100 Ω Chip Resistors (0402)
C9	33 pF AVX Chip Capacitor, ACCU-P (08053J330JBT)	PCB	Rogers 04350, 20 mils

Figure 1. 921–960 MHz Demo Board Schematic

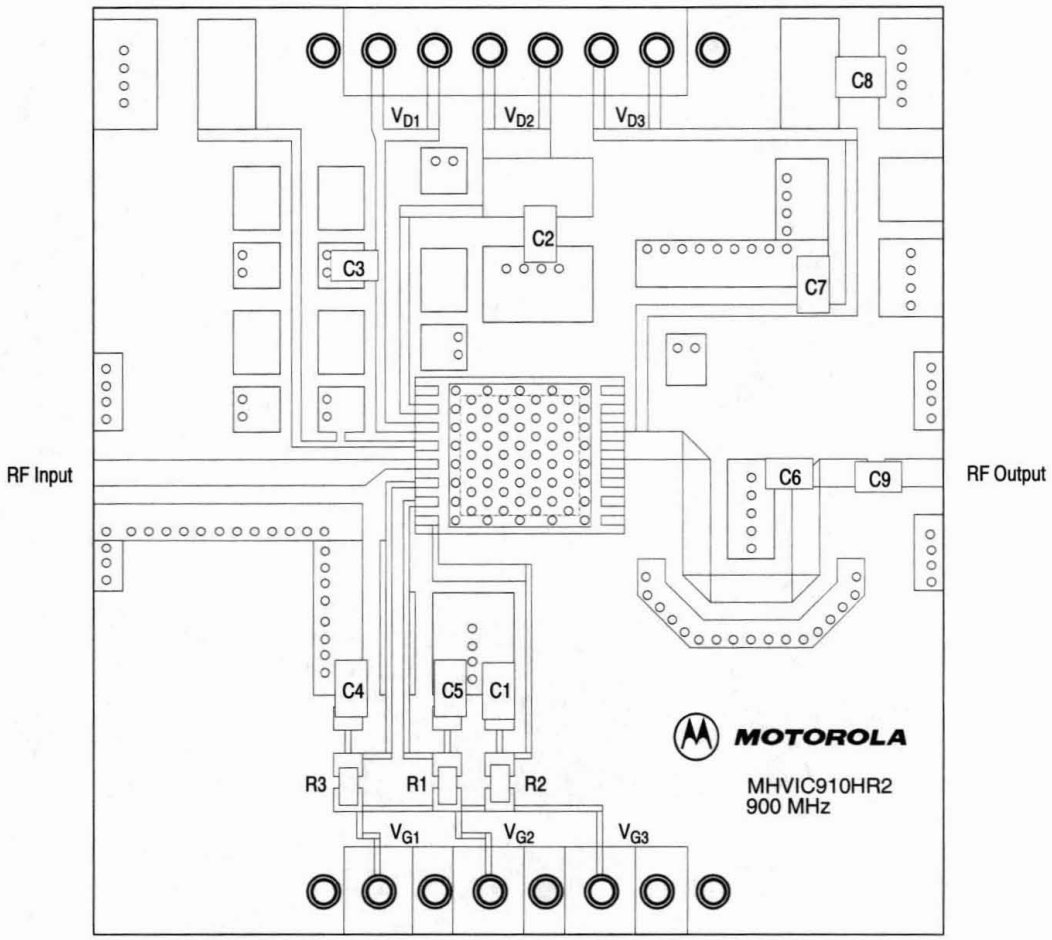


Figure 2. 921–960 MHz Demo Board Component Layout

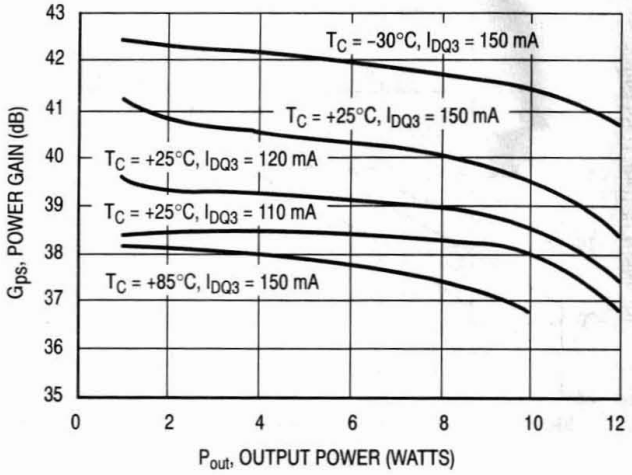


Figure 3. Power Gain versus Output Power

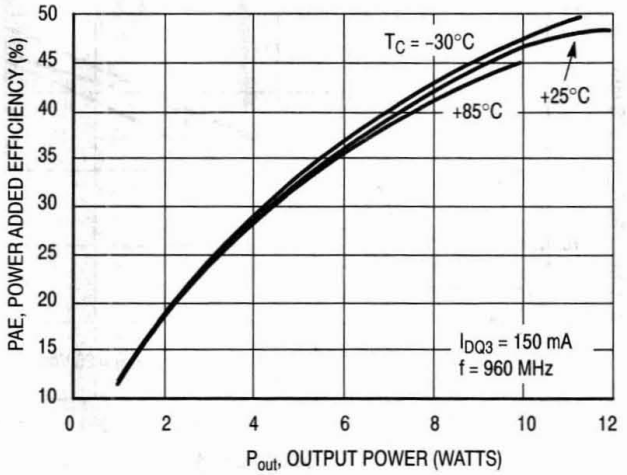


Figure 4. Power Added Efficiency versus Output Power

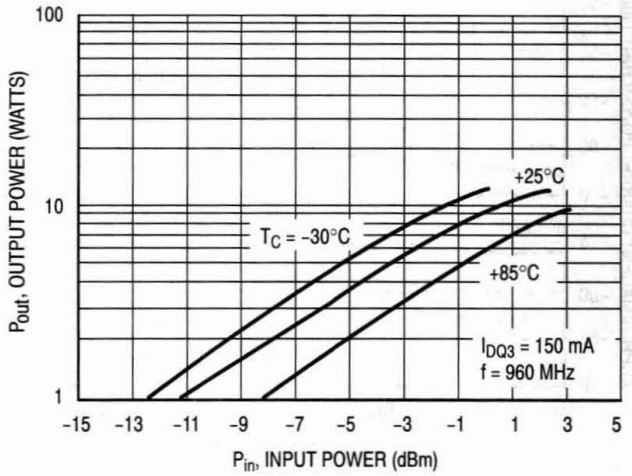


Figure 5. Output Power versus Input Power

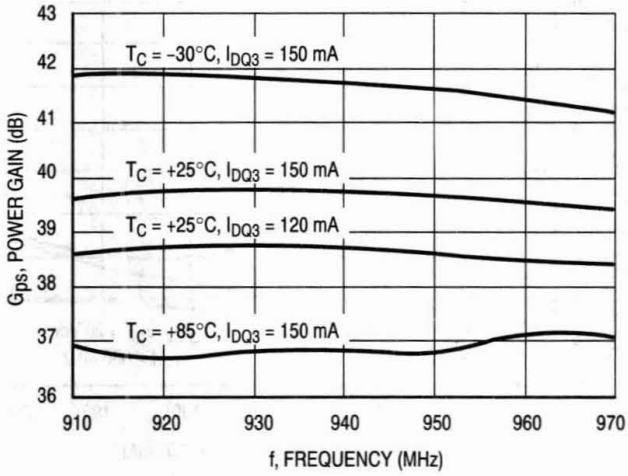


Figure 6. Power Gain versus Frequency P_{out} = 10 W

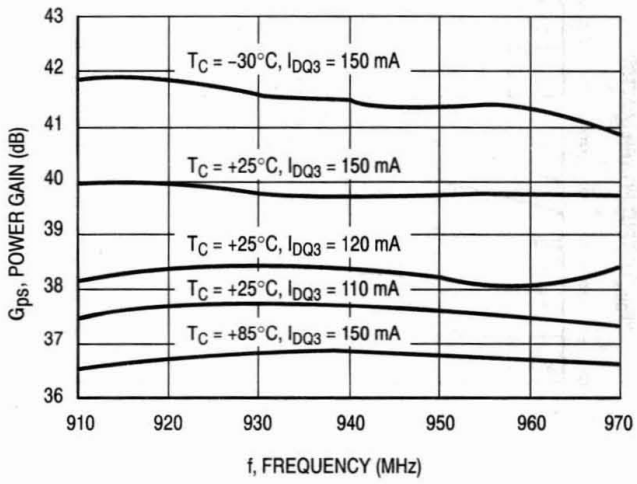


Figure 7. Power Gain versus Frequency P_{out} = P1dB

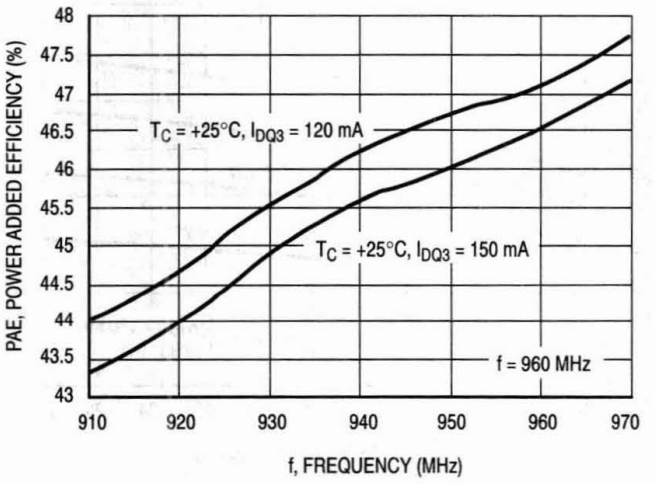


Figure 8. Power Added Efficiency versus Frequency P_{out} = 10 W

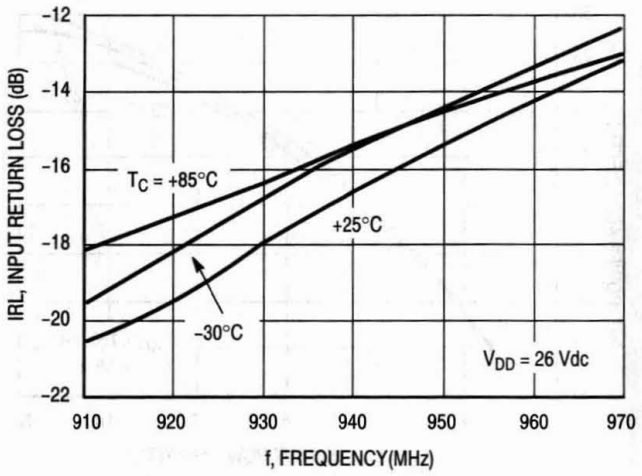


Figure 9. Input Return Loss versus Frequency
P_{out} = 10 W

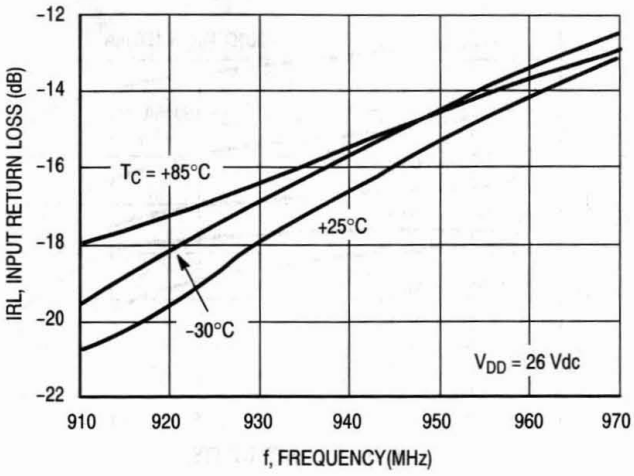


Figure 10. Input Return Loss versus Frequency
P_{out} = P1dB

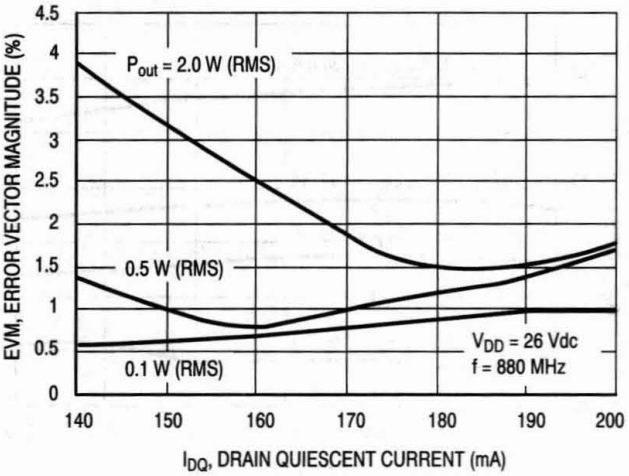


Figure 11. Error Vector Magnitude versus I_{DQ} Total

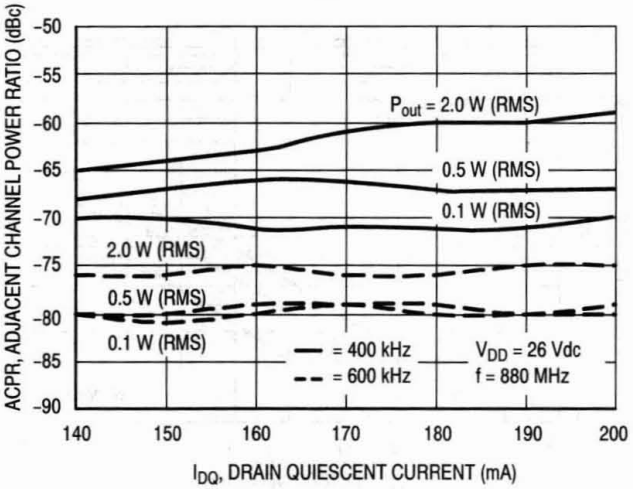


Figure 12. Adjacent Channel Power Ratio versus I_{DQ} Total

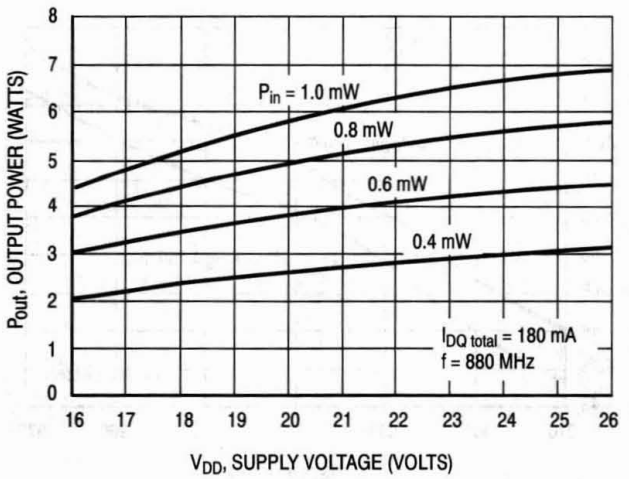


Figure 13. Output Power versus Supply Voltage

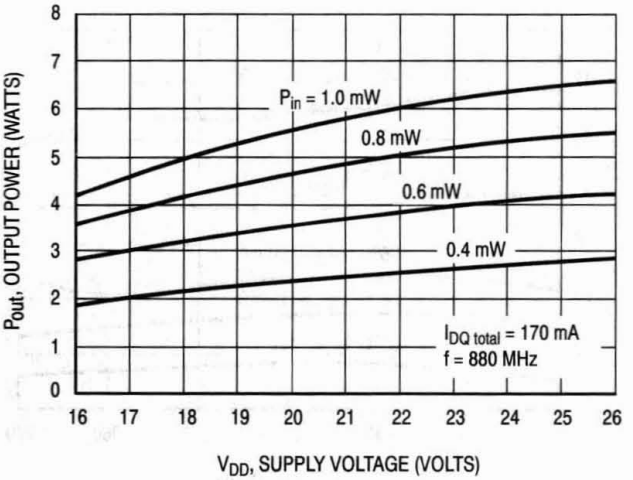


Figure 14. Output Power versus Supply Voltage

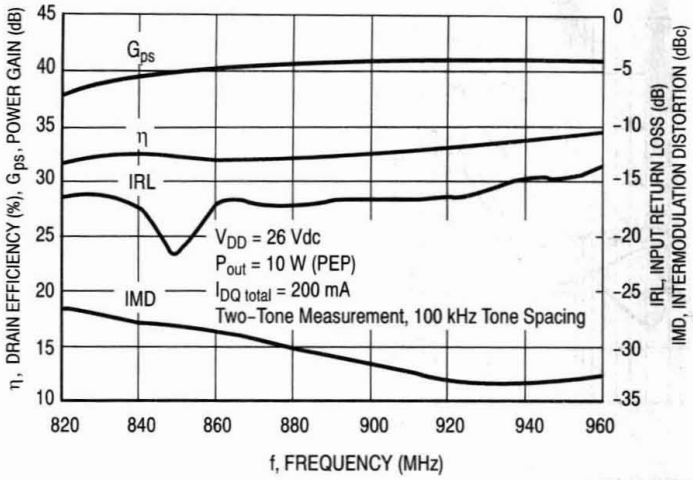


Figure 15. Two–Tone Broadband Performance

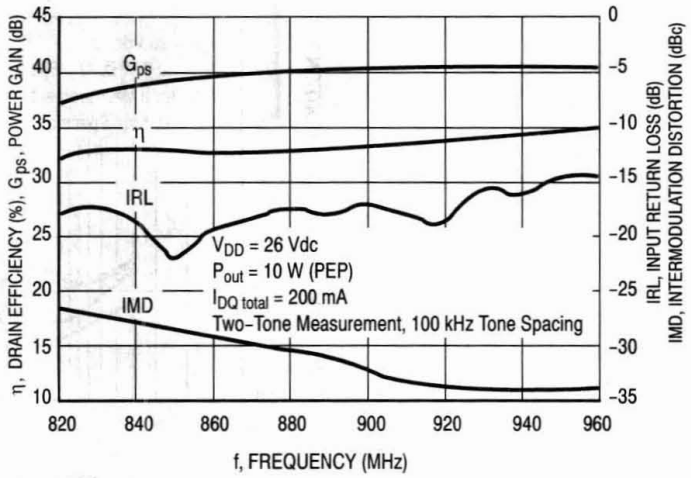


Figure 16. Two–Tone Broadband Performance

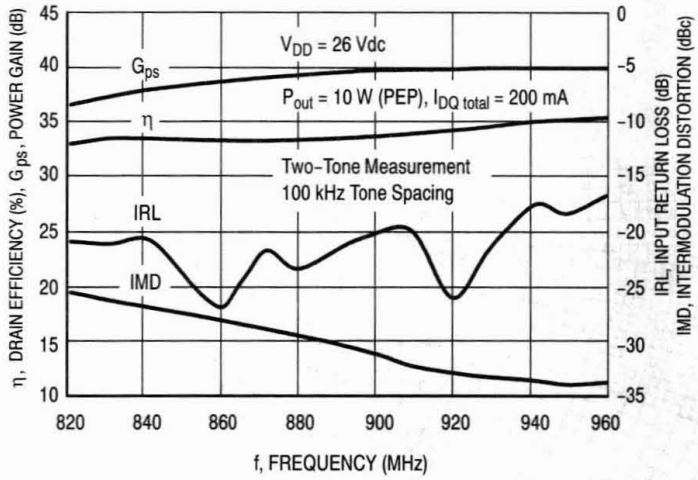


Figure 17. Two–Tone Broadband Performance

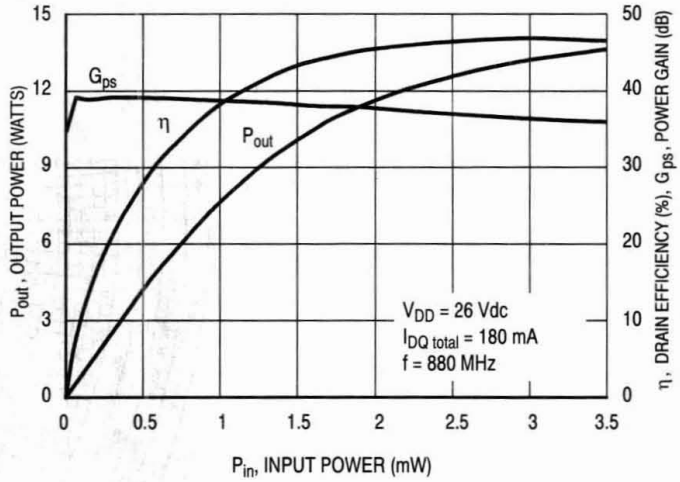


Figure 18. CW Performance @ 880 MHz

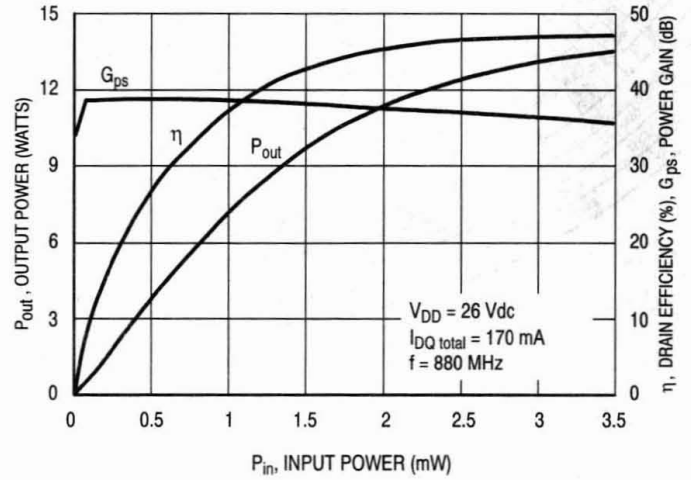


Figure 19. CW Performance @ 880 MHz

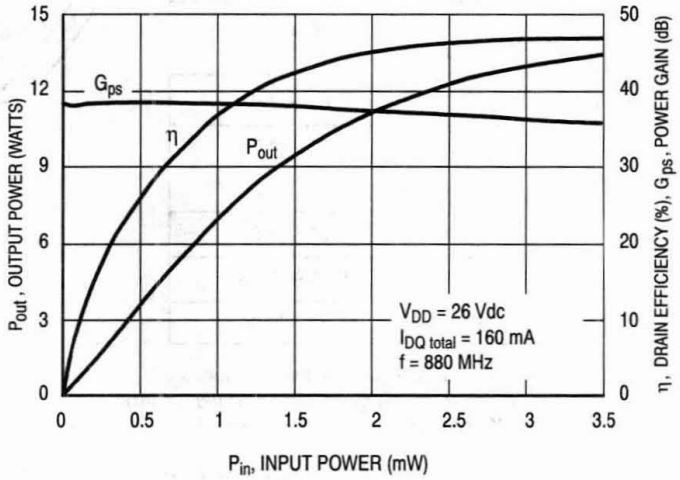


Figure 20. CW Performance @ 880 MHz

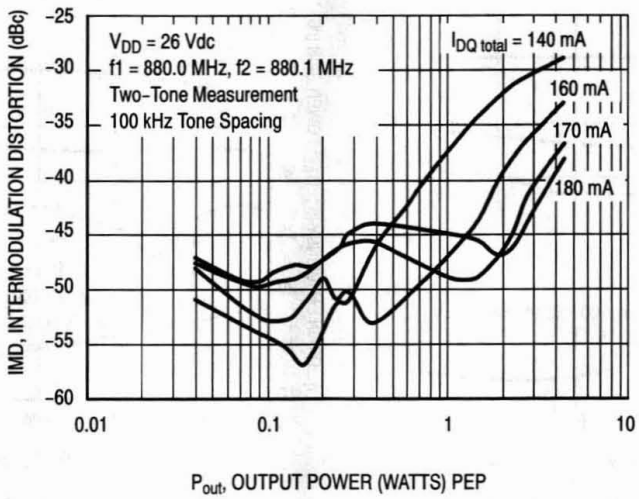
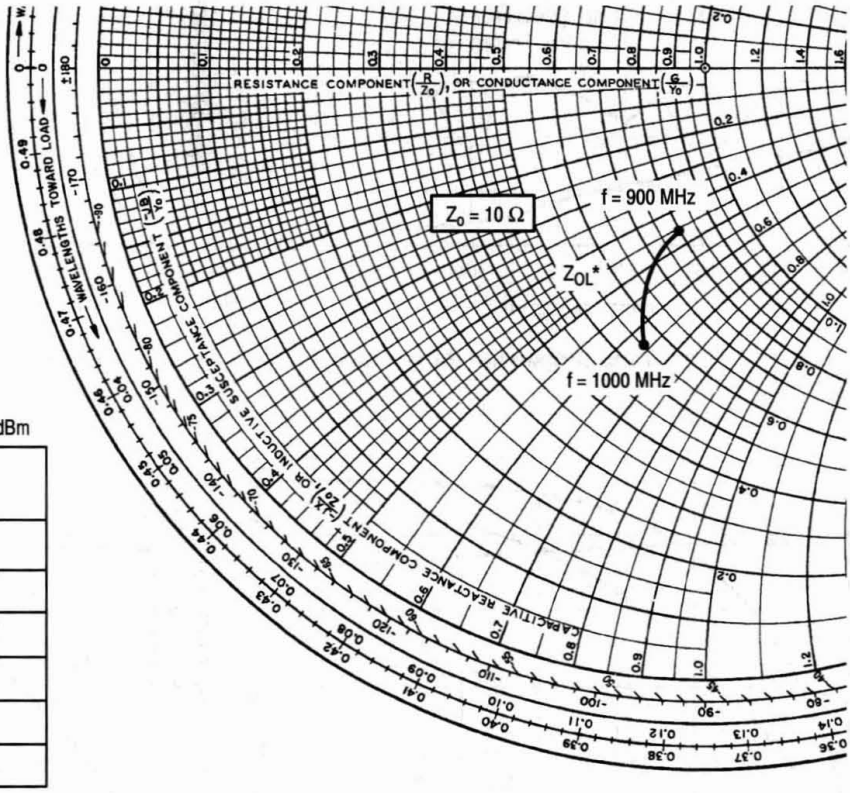


Figure 21. Intermodulation Distortion versus Output Power



V_{DD} = 26 V, I_{DQ} = 225 mA, P_{out} = 40 dBm

f MHz	Z_{OL}* Ω
900	7.81 – j4.61
920	7.27 – j4.90
940	6.77 – j5.23
960	6.31 – j5.59
980	5.90 – j5.96
1000	5.53 – j6.36

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, and drain efficiency.

Figure 22. Large Signal Impedance

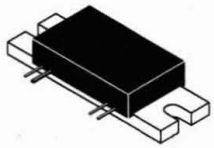
The RF Line

PCS Band RF Power LDMOS Amplifiers

MHW1810-1
MHW1810-2

- Specified 26 Volts, 1805–1880 MHz, Class AB Characteristics
  Output Power = 16 Watts CW Typ
  Power Gain = 26 dB Typ @ 10 Watts (MHW1810–1)
  Power Gain = 34 dB Typ @ 10 Watts (MHW1810–2)
  Efficiency = 34% Min @ 10 Watts
- 50 Ω Input/Output System
- Designed for GSM Linearity Requirements

1805–1880 MHz, 10 W
RF POWER LDMOS AMPLIFIERS



CASE 301AW–02, STYLE 1

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
DC Supply Voltage		V_S	28	Vdc
DC Bias Voltage		V_{bias}	28	Vdc
RF Input Power	MHW1810–1 MHW1810–2	P_{in}	21 16	dBm
RF Output Power		P_{out}	20	W
Operating Case Temperature Range		T_C	– 10 to +90	°C
Storage Temperature Range		T_{stg}	– 30 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C, V_S = 26 Vdc; V_{bias} = 5 Vdc; 50 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	1805	—	1880	MHz
Quiescent Current (P_{in} = 0 mW)		I_{DQ}	100	—	150	mA
Bias Current		I_{bias}	—	—	2	mA
Output Power at 1 dB Compression		P_{1dB}	10	14	—	W
Power Gain (P_{out} = 10 W) (P_{out} = 10 W)	MHW1810–1 MHW1810–2	G_p	24 32	26 34	28 36	dB
Efficiency (P_{out} = 10 W)		η	34	—	—	%
Input VSWR (P_{out} = 10 W)		$VSWR_{in}$	—	—	1.8:1	—
Harmonics at $2f_o$ (P_{out} = 10 W)		H_2	—	—	– 35	dBc
Harmonics at $3f_o$ (P_{out} = 10 W)		H_3	—	—	– 45	dBc
Reverse IMD; P_{out} = 10 W; Preverse = –40 dBc (F1 = F0 ±200 kHz @ –40 dBc)		IMD_r	—	—	– 50	dBc
Load Mismatch Stress Load VSWR = 5:1, All Phase Angles		ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 10 W, $V_S \leq$ 26 Vdc) Load VSWR = 5:1, All Phase Angles		—	All Spurious Outputs More Than 60 dB Below Desired Signal			

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

EXTREME CASE ELECTRICAL CHARACTERISTICS (T_C = –10 to +85°C, V_S = 23.5 to 26 Vdc, V_{bias} = 3 to 26 Vdc, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1805	—	1880	MHz
Quiescent Current (P_{in} = 0 mW)	I_{DQ}	100	—	160	mA
Bias Current	I_{bias}	—	—	2	mA
Output Power at 1 dB Compression	P_{1dB}	8	—	—	W
Power Gain Variation for a Given Part (P_{out} = 10 W)	G_p	—	5	6.5	dB
Efficiency (P_{out} = 10 W)	η	32	—	—	%
Input VSWR	$VSWR_{in}$	—	—	2:1	—
Harmonics at $2f_o$	H_2	—	—	– 35	dBc
Harmonics at $3f_o$	H_3	—	—	– 45	dBc
Reverse IMD; P_{out} = 10 W; Preverse = –40 dBc (F1 = F0 ±200 kHz @ –40 dBc)	IMD_r	—	—	– 50	dBc
Load Mismatch Stress Load VSWR = 5:1, All Phase Angles	ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 10 W, $V_S \leq$ 26 Vdc) Load VSWR = 5:1, All Phase Angles	—	All Spurious Outputs More Than 60 dB Below Desired Signal			

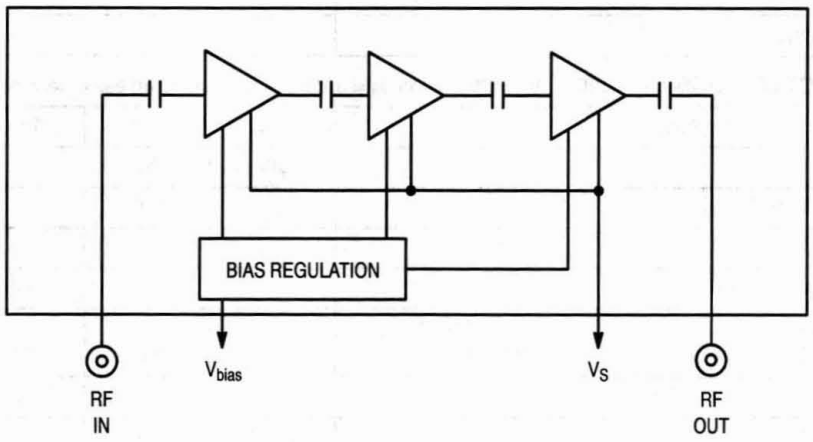


Figure 1. Internal Diagram

TYPICAL CHARACTERISTICS
MHW1810–1

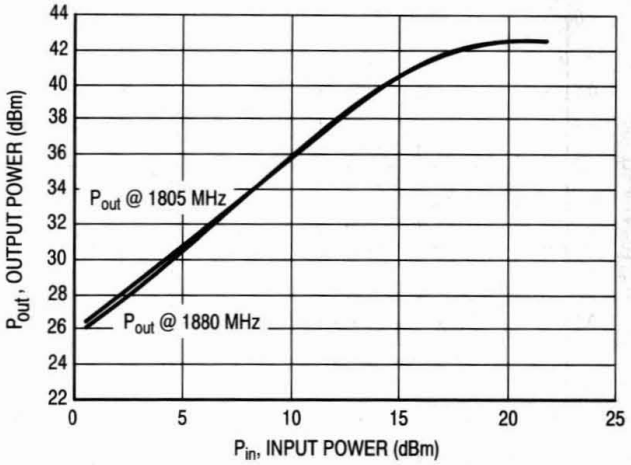


Figure 2. Output Power versus Input Power

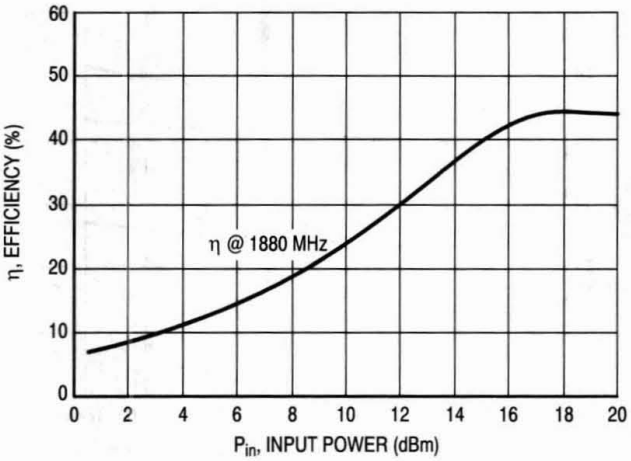


Figure 3. Efficiency versus Input Power

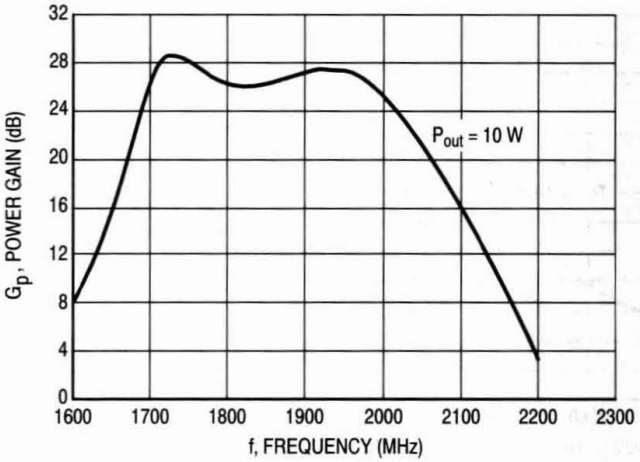


Figure 4. Power Gain versus Frequency

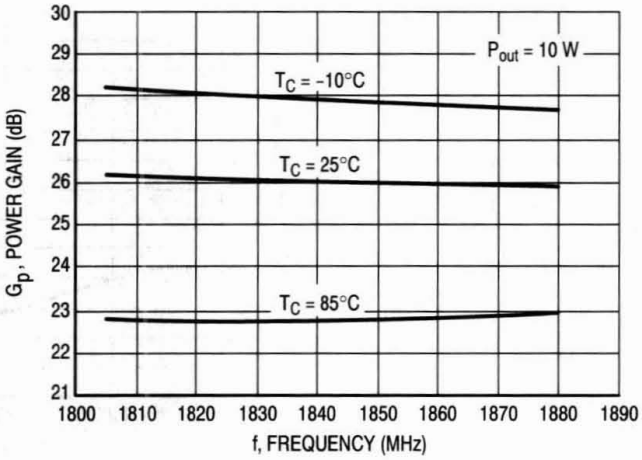


Figure 5. Gain versus Frequency

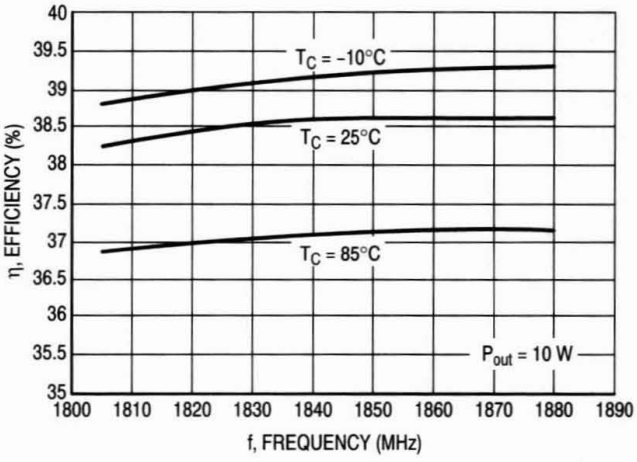


Figure 6. Efficiency versus Frequency

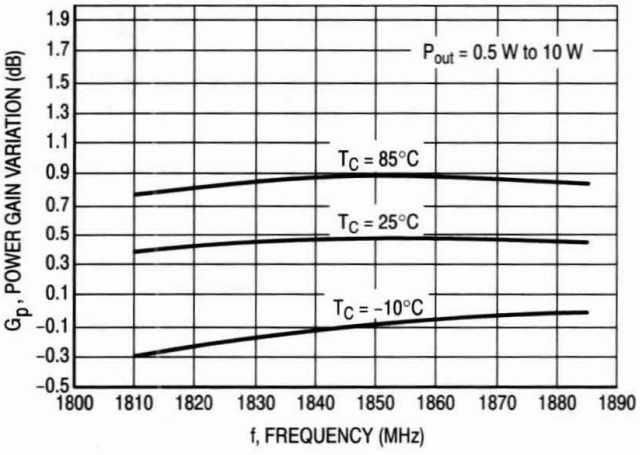


Figure 7. Power Gain Variation versus Frequency

TYPICAL CHARACTERISTICS
MHW1810–1

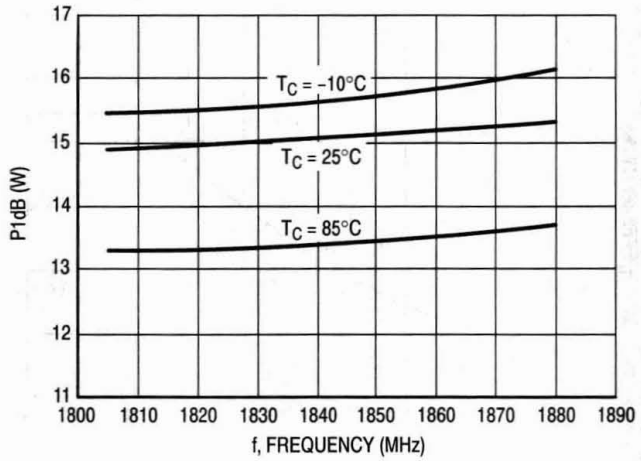


Figure 8. P1dB versus Frequency

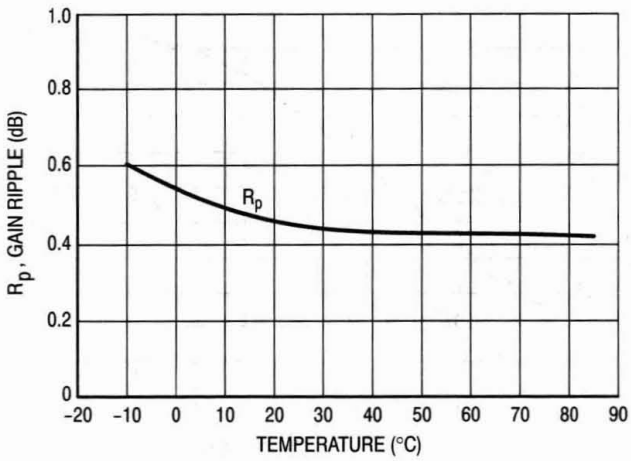


Figure 9. Gain Ripple versus Temperature

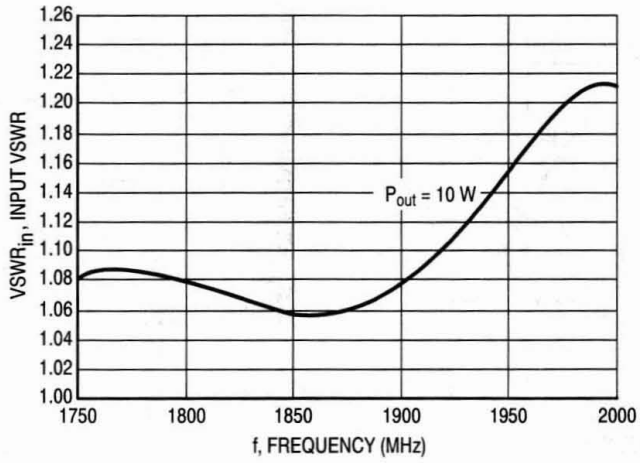


Figure 10. Input VSWR

TYPICAL CHARACTERISTICS
MHW1810–2

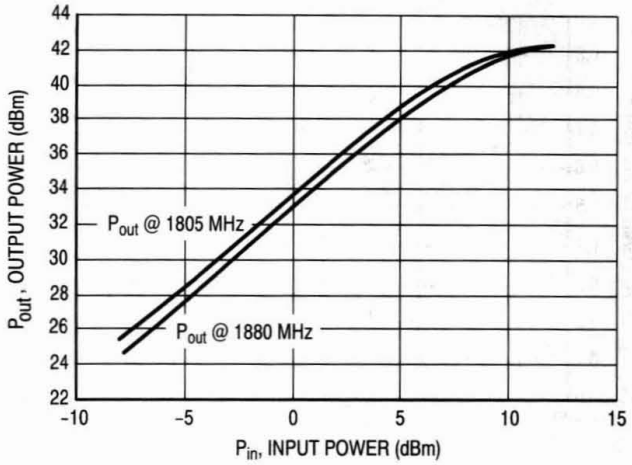


Figure 11. Output Power versus Input Power

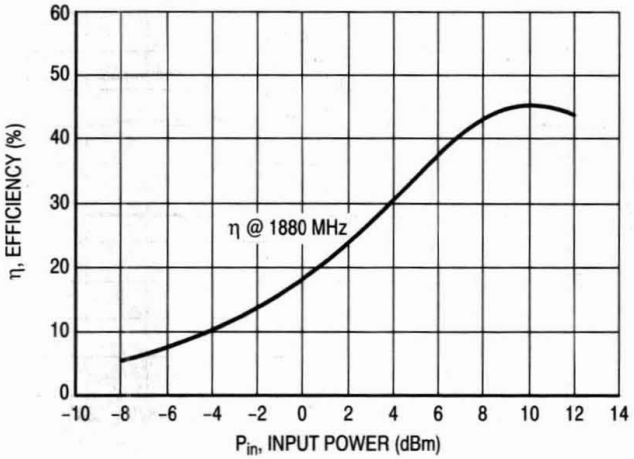


Figure 12. Efficiency versus Input Power

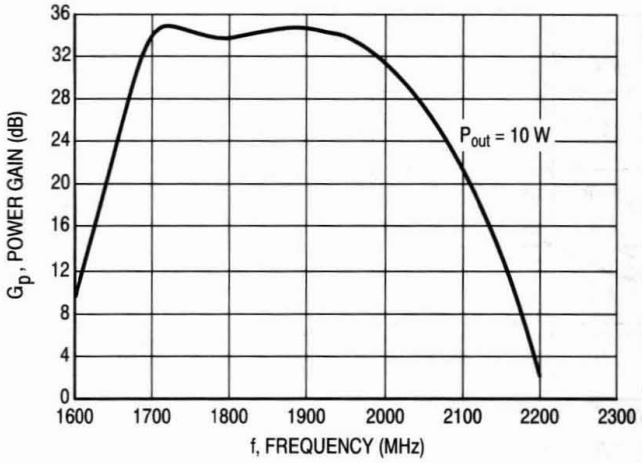


Figure 13. Power Gain versus Frequency

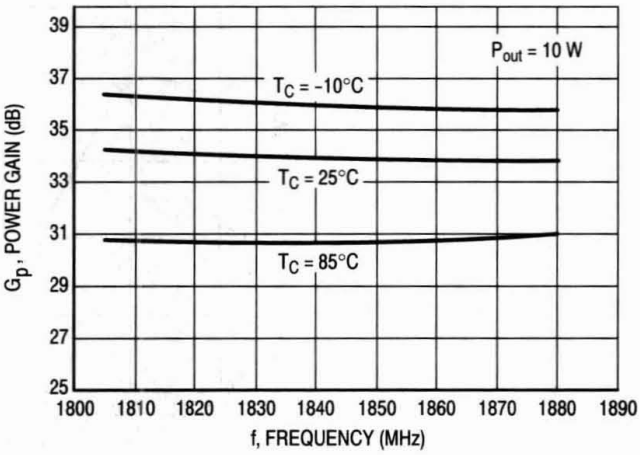


Figure 14. Gain versus Frequency

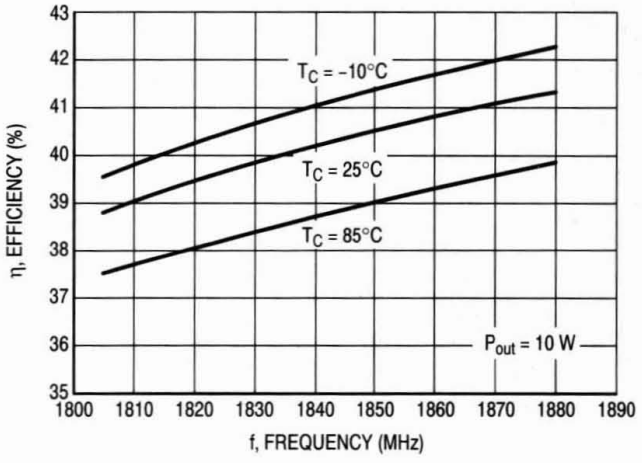


Figure 15. Efficiency versus Frequency

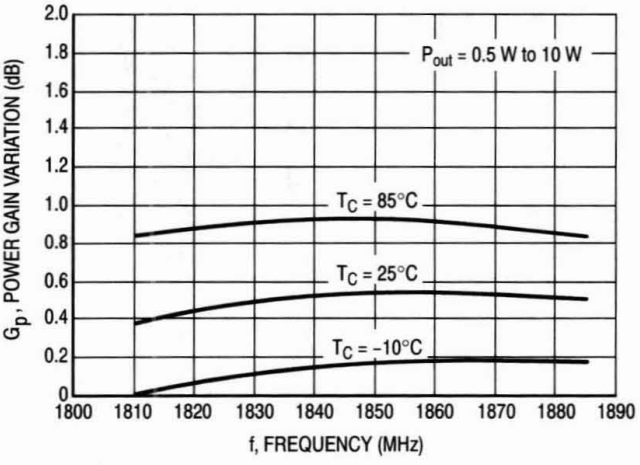


Figure 16. Power Gain Variation versus Frequency

TYPICAL CHARACTERISTICS
MHW1810–2

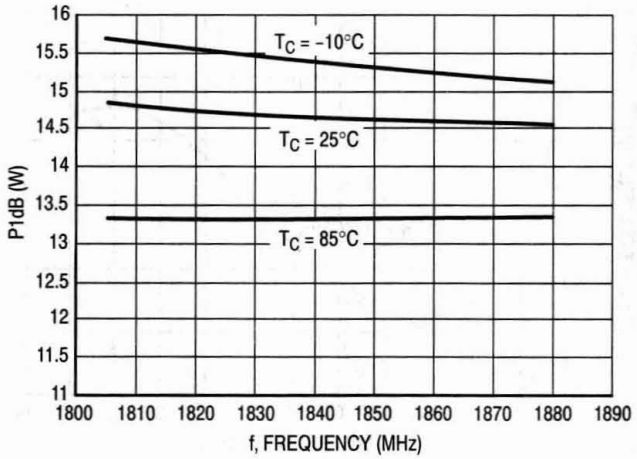


Figure 17. P1dB versus Frequency

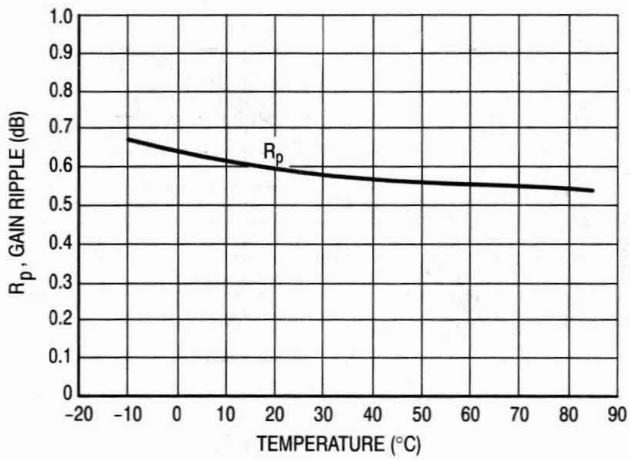


Figure 18. Gain Ripple versus Temperature

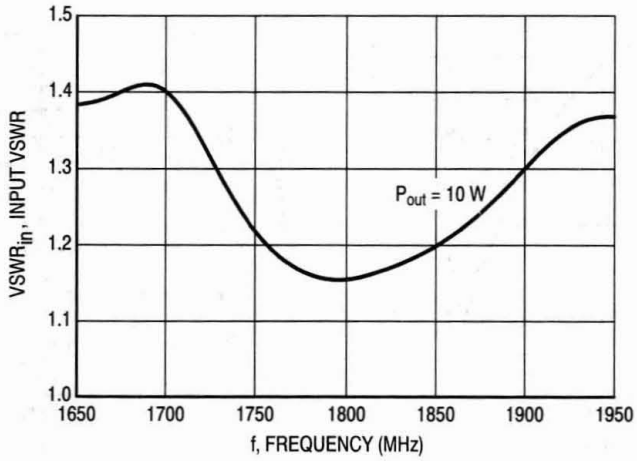


Figure 19. Input VSWR

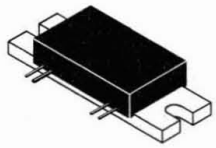
The RF Line

PCS Band RF Power LDMOS Amplifier

- Specified 26 Volts, 1930–1990 MHz, Class AB Characteristics
  Output Power = 14 Watts CW Typ
  Power Gain = 26 dB Typ @ 10 Watts
  Efficiency = 34% Min @ 10 Watts
- 50 Ω Input/Output System
- Designed for GSM Linearity Requirements

MHW1910-1

1930–1990 MHz, 10 W
RF POWER LDMOS AMPLIFIER



CASE 301AW–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_S	28	Vdc
DC Bias Voltage	V_{bias}	28	Vdc
RF Input Power	P_{in}	21	dBm
RF Output Power	P_{out}	20	W
Operating Case Temperature Range	T_C	– 10 to +90	°C
Storage Temperature Range	T_{stg}	– 30 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C, V_S = 26 Vdc; V_{bias} = 5 Vdc; 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1930	—	1990	MHz
Quiescent Current (P_{in} = 0 mW)	I_{DQ}	100	—	150	mA
Bias Current	I_{bias}	—	—	2	mA
Output Power at 1 dB Compression	P_{1dB}	10	14	—	W
Power Gain (P_{out} = 10 W)	G_p	24	26	28	dB
Efficiency (P_{out} = 10 W)	η	34	—	—	%
Input VSWR	$VSWR_{in}$	—	—	1.8:1	—
Harmonics at $2f_o$	H_2	—	—	– 35	dBc
Harmonics at $3f_o$	H_3	—	—	– 45	dBc
Reverse IMD; P_{out} = 10 W; Preverse = –40 dBc (F1 = F0 ±200 kHz @ –40 dBc)	IMD_r	—	—	– 50	dBc
Load Mismatch Stress Load VSWR = 5:1, All Phase Angles	ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 10 W, $V_S \leq$ 26 Vdc) Load VSWR = 5:1, All Phase Angles	—	All Spurious Outputs More Than 60 dB Below Desired Signal			

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 2

EXTREME CASE ELECTRICAL CHARACTERISTICS (T_C = –10 to +85°C, V_S = 23.5 to 26 Vdc, V_{bias} = 3 to 26 Vdc, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1930	—	1990	MHz
Quiescent Current (P_{in} = 0 mW)	I_{DQ}	100	—	160	mA
Bias Current	I_{bias}	—	—	2	mA
Output Power at 1 dB Compression	P_{1dB}	8	—	—	W
Power Gain Variation for a Given Part (P_{out} = 10 W)	G_p	—	5	6.5	dB
Efficiency (P_{out} = 10 W)	η	32	—	—	%
Input VSWR	$VSWR_{in}$	—	—	2:1	—
Harmonics at $2f_o$	H_2	—	—	– 35	dBc
Harmonics at $3f_o$	H_3	—	—	– 45	dBc
Reverse IMD; P_{out} = 10 W; Preverse = –40 dBc (F1 = F0 ±200 kHz @ –40 dBc)	IMD_r	—	—	– 46	dBc
Load Mismatch Stress Load VSWR = 5:1, All Phase Angles	ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 10 W, $V_S \leq$ 26 Vdc) Load VSWR = 5:1, All Phase Angles	—	All Spurious Outputs More Than 60 dB Below Desired Signal			

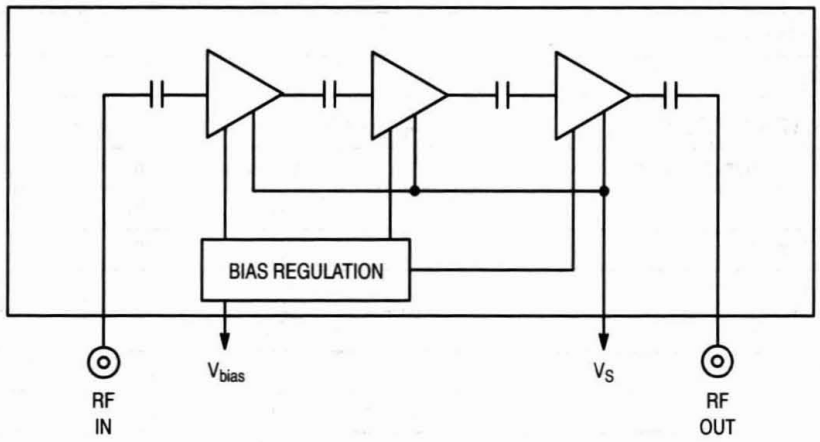


Figure 1. Internal Diagram

TYPICAL CHARACTERISTICS

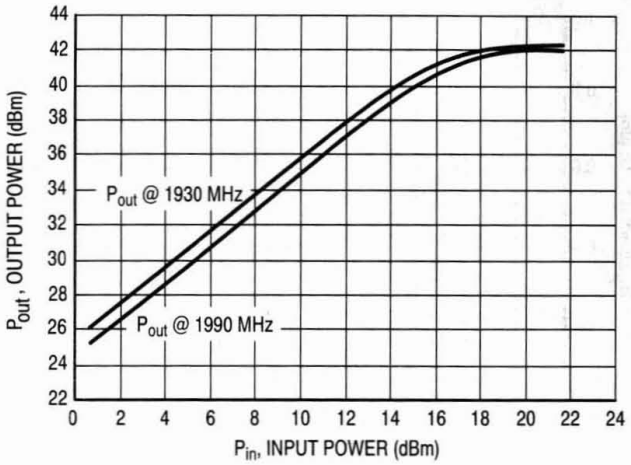


Figure 2. Output Power versus Input Power

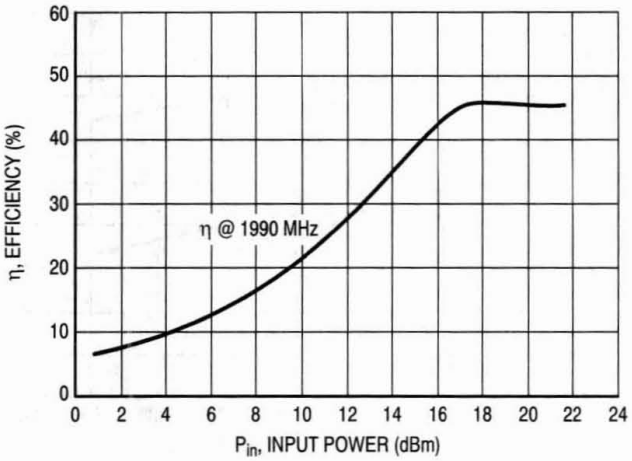


Figure 3. Efficiency versus Input Power

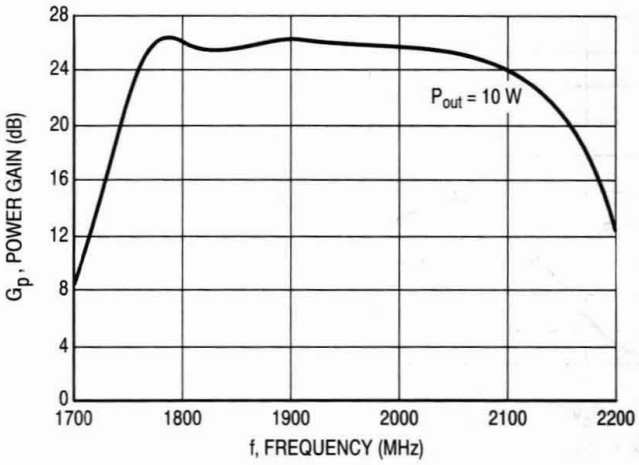


Figure 4. Power Gain versus Frequency

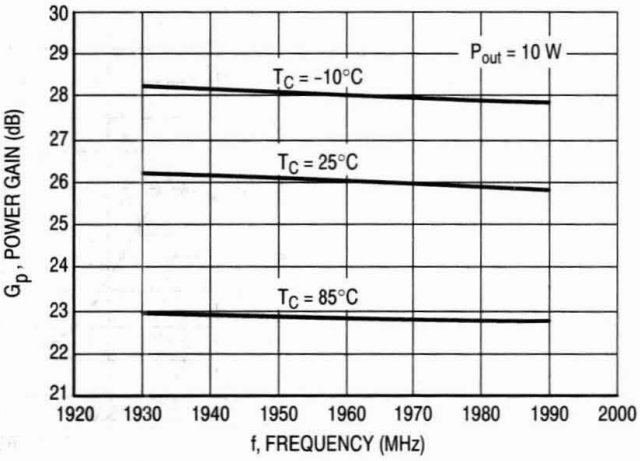


Figure 5. Gain versus Frequency

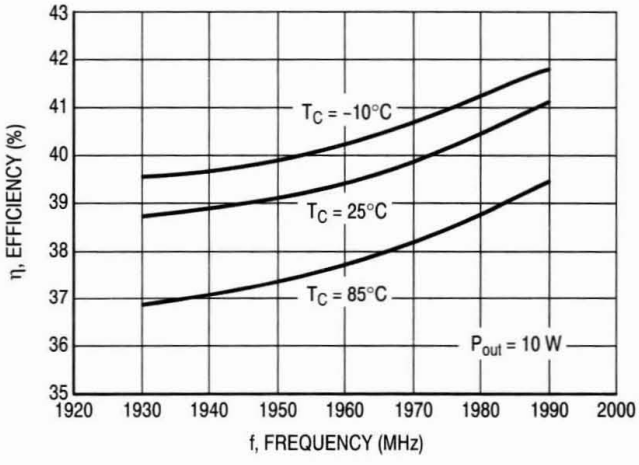


Figure 6. Efficiency versus Frequency

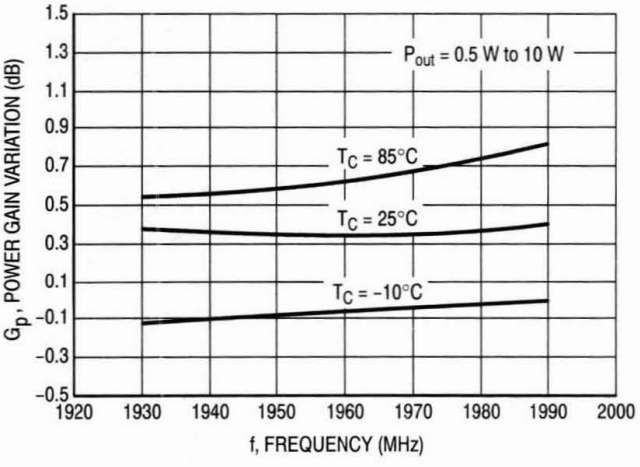


Figure 7. Power Gain Variation versus Frequency

TYPICAL CHARACTERISTICS

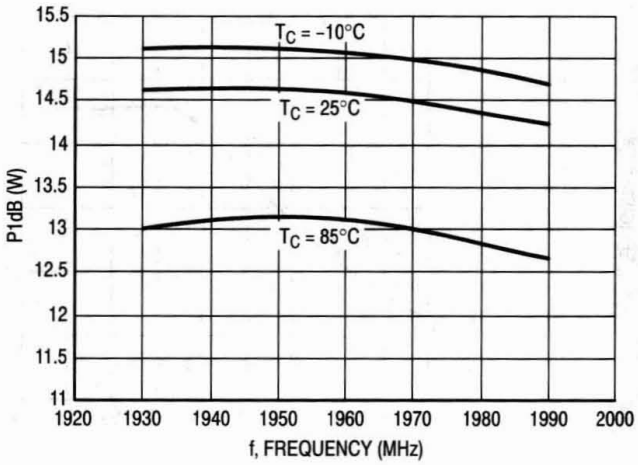


Figure 8. P1dB versus Frequency

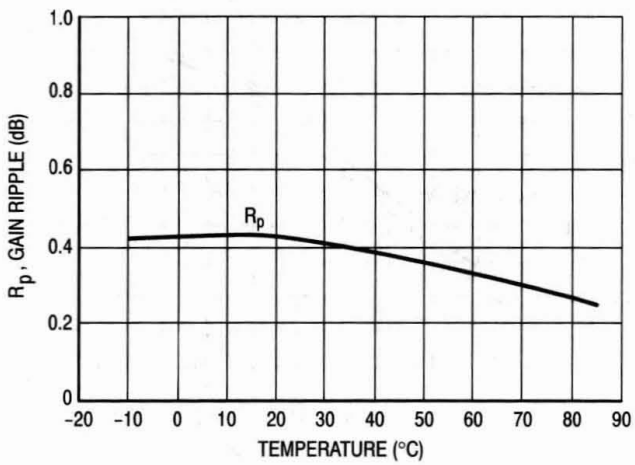


Figure 9. Gain Ripple versus Temperature

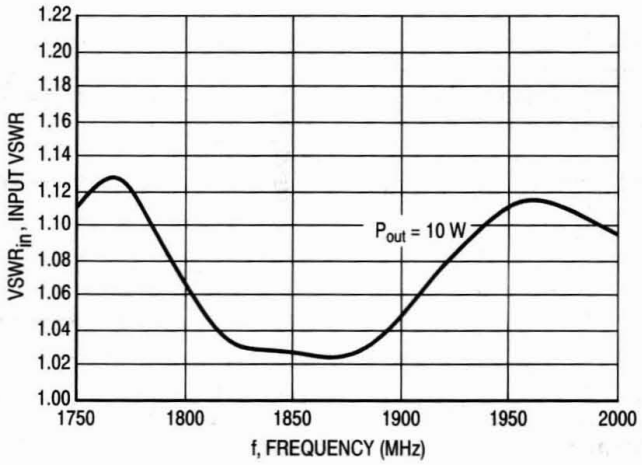


Figure 10. Input VSWR

Chapter Seven
RF CATV Distribution Amplifiers

Section One **7.1–0**
RF CATV Distribution Amplifiers –
Selector Guide

Section Two **7.2–0**
RF CATV Distribution Amplifiers –
Data Sheets

Section One
Selector Guide

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest CATV generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels. Additions to our CATV product family include 40–870 MHz high output gallium arsenide (GaAs) power doublers as well as low distortion, low power consumption reverse amplifiers.

Table of Contents

	Page
RF CATV Distribution Amplifiers	7.1–1
Forward Amplifiers	7.1–2
Reverse Amplifiers	7.1–4
Packages	7.1–6

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Forward Amplifiers

40–1000 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 1000 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 152 CH	Cross Modulation dB 152 CH		
MHW9182B	18.5	152	+38	–63(40)	–61	–61	7.5	714Y/1
MHW9242A	24	152	+38	–61(40)	–58	–59	8.0	714Y/1

40–870 MHz High Output Gallium Arsenide Power Doubler

Product	Hybrid Gain (Nom.) @ 870 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 870 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 132 CH	Cross Modulation dB 132 CH		
MHW9187★	20	132	+48	–62(34)	–56	–55	4.5	1302/1
MHW9227(9)	22	132	+48	–58(34)	–54	–54	6.0	1302/1
MHW9247(46b)	24	132	+48	–59(34)	–55	–54	5.5	1302/1
MHW9267(9)	26	132	+48	–60(34)	–56	–54	5.5	1302/1

40–870 MHz Gallium Arsenide Preamplifiers

Product	Hybrid Gain (Nom.) @ 870 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 870 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 132 CH	Cross Modulation dB 132 CH		
MHW9146(9)	14	132	+44	–64(36)	–56	–55	5.5	1302/1
MHW9186(46a)	18.5	128	+44	–62(36)	–58	–52	5.0	1302/1
MHW9206(46b)	20	132	+44	–64(36)	–55	–55	4.5	1302/1
MHW9236(46b)	23	132	+44	–60(36)	–54	–53	5.5	1302/1
MHW9256(9)	25	132	+44	–60(36)	–55	–53	5.0	1302/1
MHW9276(9)	27	132	+44	–60(36)	–56	–53	5.0	1302/1

(9)In development.

(34)Composite 2nd Order; V_{out} = +48 dBmV/ch

(36)Composite 2nd order; V_{out} = +44 dBmV/ch

(40)Composite 2nd Order; V_{out} = +38 dBmV/ch

(46)To be introduced: a) 1Q02; b) 2Q02

★New Product

CATV Distribution: Forward Amplifiers (continued)

40–870 MHz Preamplifiers

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation dB 128 CH	Noise Figure @ 870 MHz dB Max	Package/ Style
MHW8202B[46a]	20.4	128	+38	–67[40]	–64	–64	7.0	1302/1

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55 MHz dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
MHW8182B	18.5	128	+38	–64[40]	–66	–65	7.5	714Y/1
MHW8222B	21.9	128	+38	–60[40]	–64	–63	7.0	1302/1
MHW8242A	24	128	+38	–62[40]	–64	–62	7.5	714Y/1
MHW8272A	27.2	128	+38	–64[40]	–64	–62	7.0	714Y/1
Power Doubling Hybrids								
MHW8185L[21]	18.5	128	+40	–62[39]	–63	–64	8.5*	714Y/1
MHW8185	18.8	128	+40	–62[39]	–64	–64	8.0	714Y/1
MHW8205L[22]	19.5	128	+40	–60[39]	–63	–64	8.5*	714Y/1
MHW8205	19.8	128	+40	–60[39]	–63	–64	8.0	714Y/1

*@ 870 MHz

40–750 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Cross Modulation FM = 55 MHz dB 110 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
MHW7182B	18.5	110	+40	–63[39]	–66	–64	6.5	714Y/1
MHW7222B	21.9	110	+40	–60[39]	–61	–60	6.5	1302/1
MHW7242A	24	110	+40	–62[39]	–63	–61	7.0	714Y/1
MHW7272A	27.2	110	+40	–64[39]	–64	–60	6.5	714Y/1
Power Doubling Hybrids								
MHW7185C	18.8	110	+44	–64[36]	–62	–63	7.5	714Y/1
MHW7205C	19.8	110	+44	–63[36]	–61	–62	7.5	714Y/1

[21]Low DC Current Version of MHW8185; Typical I_{CC} @ Vdc = 24 V is 365 mA.

[22]Low DC Current Version of MHW8205; Typical I_{CC} @ Vdc = 24 V is 365 mA.

[36]Composite 2nd order; V_{out} = +44 dBmV/ch

[39]Composite 2nd order; V_{out} = +40 dBmV/ch

[40]Composite 2nd Order; V_{out} = +38 dBmV/ch

[46]To be introduced: a) 1Q02; b) 2Q02

CATV Distribution: Forward Amplifiers (continued)

40–550 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 77 CH	Cross Modulation dB 77 CH	Noise Figure @ 550 MHz dB Max	Package/ Style
MHW6342T	34.5	77	+44	–64[35]	–57	–57	6.5	1302/1

Reverse Amplifiers

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test[30] dB	Composite Triple Beat dB 22 CH	Composite Triple Beat dB 26 CH	Cross Modulation dB 22 CH	Cross Modulation dB 26 CH	Noise Figure @ 175 MHz dB Max	Package/ Style
MHW1244	24	22	+50	–72	–68	–67.5[19]	–61	–61[19]	5.0	714Y/1

Low Current Amplifiers — 5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB 6 CH	2nd Order Test dB 10 CH	Composite Triple Beat dB 6 CH	Composite Triple Beat dB 10 CH	Cross Modulation dB 6 CH	Cross Modulation dB 10 CH	DC Current mA Typ.	Noise Figure @ 200 MHz dB Max	Pkg/ Style
MHW1223LA	22.7	6,10	50	–68	–65	–75	–66	–65	–60	95	7.0	1302/1
MHW1253LA	25.5	6,10	50	–68	–66	–75	–66	–65	–61	95	6.5	1302/1
MHW1303LA	30.8	6,10	50	–68	–65	–74	–64	–64	–58	95	5.7	1302/1

Low Current Amplifiers — 5–150 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB 6 CH	2nd Order Test dB 10 CH	Composite Triple Beat dB 6 CH	Composite Triple Beat dB 10 CH	Cross Modulation dB 6 CH	Cross Modulation dB 10 CH	DC Current mA Typ.	Noise Figure @ 150 MHz dB Max	Pkg/ Style
MHW1353LA	35.2	6,10	50	–68	–65	–73	–62	–63	–57	95	5.4	1302/1

[19]Typical

[30]Channels 2 and A @ 7

[35]Channels 2 and M30 @ M39

CATV Distribution: Reverse Amplifiers (continued)

Low Current Amplifiers — 5–65 MHz Hybrids, V_{CC} = 24 Vdc, Class A

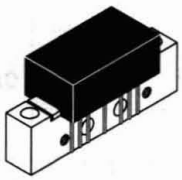
Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB: 6 CH	2nd Order Test dB: 10 CH	Composite Triple Beat dB: 6 CH	Composite Triple Beat dB: 10 CH	Cross Modulation dB: 6 CH	Cross Modulation dB: 10 CH	DC Current mA Typ.	Noise Figure @ 65 MHz dB Max	Pkg/ Style
MHW1224LA	22.7	6,10	50	–68	–65	–75	–66	–65	–60	95	7.0	1302/1
MHW1254LA	25.5	6,10	50	–68	–66	–75	–66	–65	–61	95	6.5	1302/1
MHW1304LA	30.8	6,10	50	–68	–65	–74	–64	–64	–58	95	5.7	1302/1
MHW1354LA	35.2	6,10	50	–68	–65	–73	–62	–63	–57	95	5.4	1302/1

Low Current Amplifiers — 5–50 MHz Hybrids, V_{CC} = 24 Vdc, Class A

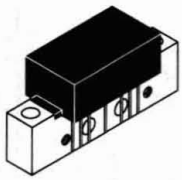
Product	Hybrid Gain (Nom.) dB	Channel Loading Capacity	I_{DC} mA Max	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test[30] dB	Composite Triple Beat dB: 4 CH	Cross Modulation dB: 4 CH	Noise Figure @ 50 MHz dB Max	Package/ Style
MHW1254L	25	4	135	+50	–70	–70	–62	4.5	714Y/1

[30]Channels 2 and A @ 7

RF CATV Distribution Amplifiers Packages



CASE 714Y
STYLE 1, 2



CASE 1302
STYLE 1

SCALE 1:2

Section Two

Motorola RF CATV Distribution Amplifiers – Data Sheets

Device Number	Page Number
MHW1223LA	7.2–3
MHW1224LA	7.2–5
MHW1244	7.2–7
MHW1253LA	7.2–9
MHW1254L	7.2–11
MHW1254LA	7.2–12
MHW1303LA	7.2–14
MHW1304LA	7.2–16
MHW1353LA	7.2–18
MHW1354LA	7.2–20
MHW6342T	7.2–22
MHW7182B	7.2–24
MHW7185C	7.2–25
MHW7205C	7.2–26
MHW7222B	7.2–27
MHW7242A	7.2–29
MHW7272A	7.2–30
MHW8182B	7.2–31
MHW8185	7.2–32
MHW8185L	7.2–33
MHW8205	7.2–34
MHW8205L	7.2–35
MHW8222B	7.2–36
MHW8242A	7.2–38
MHW8272A	7.2–39
MHW9182B	7.2–40
MHW9187	7.2–41
MHW9242A	5.2–43

The RF Line

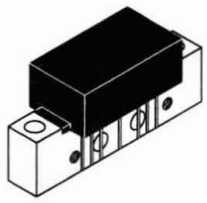
Low Distortion Wideband Reverse Amplifier Modules

Designed specifically for broadband applications requiring low multi–channel distortion characteristics. Specified for use as return amplifiers for 2–way cable TV systems.

- Designed for Low Power Consumption
- Specified for 6 and 10 Channel Performance
- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- All Gold Metallization
- Designed to Ensure Good Gain Stability versus Temperature

MHW1223LA

5–200 MHz, 22.7 dB
CATV LOW CURRENT AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Bandwidth	All	BW	5	—	200	MHz
Power Gain	(f = 5 MHz)	G_p	22.1	22.7	23.5	dB
Slope	(5–200 MHz)	S	– 0.2	—	0.7	dB
Gain Flatness (Peak To Valley)	(5–200 MHz)	—	—	—	0.4	dB
Return Loss — Input/Output		IRL/ORL				dB
	(@ f = 5–150 MHz)		20	—	—	
	(@ f = 150–200 MHz)		18	—	—	
Composite Second Order (V_{out} = +50 dBmV per Ch., Worst Case)						dB
	6–Channel FLAT	CSO_6	—	– 73	– 68	
	10–Channel FLAT	CSO_{10}	—	– 72	– 65	

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	XMD_6	—	–69	–65	
10–Channel FLAT	XMD_{10}	—	–63	–60	
Composite Triple Beat (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	CTB_6	—	–78	–75	
10–Channel FLAT	CTB_{10}	—	–69	–66	
Noise Figure (f = 5–200 MHz)	NF	—	6.3	7	dB
DC Current	I_{DC}	85	95	110	mA

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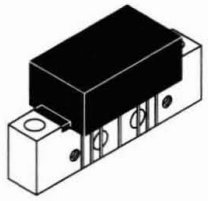
- Guaranteed Broadband Noise Figure
- All Gold Metallization
- Designed to Ensure Good Gain Stability versus Temperature

MHW1224LA

5–65 MHz, 22.7 dB
CATV LOW CURRENT AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Bandwidth	All	BW	5	—	65	MHz
Power Gain	(f = 5 MHz)	G_p	22.1	22.7	23.2	dB
Slope	(5–65 MHz)	S	– 0.2	—	0.5	dB
Gain Flatness (Peak To Valley)	(5–65 MHz)	—	—	—	0.4	dB
Return Loss — Input/Output	(@ f = 5–65 MHz)	IRL/ORL	20	—	—	dB
Composite Second Order (V_{out} = +50 dBmV per Ch., Worst Case)						dB
	6–Channel FLAT	CSO_6	—	– 73	– 68	
	10–Channel FLAT	CSO_{10}	—	– 72	– 65	

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	XMD_6	—	–69	–65	
10–Channel FLAT	XMD_{10}	—	–63	–60	
Composite Triple Beat (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	CTB_6	—	–78	–75	
10–Channel FLAT	CTB_{10}	—	–69	–66	
Noise Figure (f = 5–65 MHz)	NF	—	6.3	7	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line

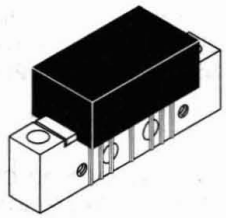
Low Distortion Wideband Amplifier

MHW1244

24.0 dB
5.0–200 MHz
CATV HIGH–SPLIT
REVERSE AMPLIFIER

Designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for mid–split and high–split 2–way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain @ f = 5.0–200 MHz
- Guaranteed Broadband Noise Figure @ f = 5.0–175 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- All Ion–Implanted Arsenic Emitter Transistor Chips with 6.0 GHz f_T's
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Ensure Good Low Frequency Gain Stability versus Temperature



CASE 714Y–03, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system)

Characteristic	Symbol	MHW1244	Units
Power Gain @ 10 MHz	G_P	24.0 ± 0.5	dB
Frequency Range (Response/Return Loss) Note 1	BW	5.0–200	MHz
Cable Slope Equivalent (5.0–200 MHz)	S	–0.2 Min/+0.8 Max	dB
Gain Flatness (5.0–200 MHz)	F	±0.2 Max	dB
Input/Output Return Loss (5.0–200 MHz) Note 1	IRL/ORL	18.0 Min	dB
Cross Modulation Distortion @ +50 dBmV per ch. 12–Channel FLAT (5.0–120 MHz) 22–Channel FLAT (5.0–175 MHz) (2) (3) 26–Channel FLAT (5.0–200 MHz)	 XM_{12} XM_{22} XM_{26}	 –66 Typ –61 Max –61 Typ	 dB dB dB

NOTES:

1. Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
2. Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22–channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7–Channels
2–6	55.25–83.25 MHz	5–Channels
A–7	121.25–175.25 MHz	10–Channels

3. Video carriers used for 12–Channel typical performances are T7–6; For 26–Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22–Channel carriers listed above.

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system)

Characteristic	Symbol	MHW1244	Units
Composite Triple Beat Distortion @ +50 dBmV per ch. 22–Channel FLAT (5.0–175 MHz) 26–Channel FLAT (5.0–200 MHz) Notes 2 and 3	 CTB_{22} CTB_{26}	 –68 Max –67.5 Typ	 dB dB
Individual Triple Beat Distortion @ +50 dBmV per ch. Mid–Split (5.0–120 MHz) T11, T12 and CH2 @ 123.25 MHz High–Split (5.0–175 MHz) T13, CH2 and CH5 @ 175.5 MHz	 TB_3 TB_3	 –87 Typ –84 Typ	 dB dB
Second Order Distortion @ +50 dBmV per ch. High–Split (5.0–175 MHz) CH2, CHA @ 176.5 MHz	IMD	–72 Max	dB
Noise Figure High–Split (5.0–175 MHz) Note 2	NF	5.0 Max	dB
DC Current	I_{DC}	210 Typ/240 Max	mAdc

NOTES:

1. Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
2. Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22–channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7–Channels
2–6	55.25–83.25 MHz	5–Channels
A–7	121.25–175.25 MHz	10–Channels

3. Video carriers used for 12–Channel typical performances are T7–6; For 26–Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22–Channel carriers listed above.

The RF Line

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- Designed for Low Power Consumption
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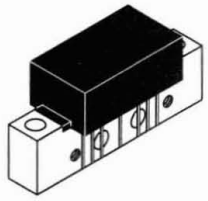
- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- All Gold Metallization
- Designed to Ensure Good Gain Stability versus Temperature

MHW1253LA

5–200 MHz, 25.5 dB
CATV LOW CURRENT AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Bandwidth	All	BW	5	—	200	MHz
Power Gain	(f = 5 MHz)	G_p	25	25.5	26	dB
Slope	(5–200 MHz)	S	– 0.2	—	0.7	dB
Gain Flatness (Peak To Valley)	(5–200 MHz)	—	—	—	0.4	dB
Return Loss — Input/Output		IRL/ORL				dB
	(@ f = 5–150 MHz)		20	—	—	
	(@ f = 150–200 MHz)		18	—	—	
Composite Second Order (V_{out} = +50 dBmV per Ch., Worst Case)						dB
	6–Channel FLAT	CSO_6	—	– 73	– 68	
	10–Channel FLAT	CSO_{10}	—	– 71	– 66	

REV 1

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	XMD_6	—	–69	–65	
10–Channel FLAT	XMD_{10}	—	–64	–61	
Composite Triple Beat (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	CTB_6	—	–78	–75	
10–Channel FLAT	CTB_{10}	—	–69	–66	
Noise Figure (f = 5–200 MHz)	NF	—	5.8	6.5	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line

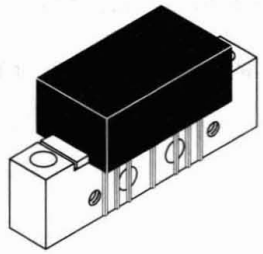
Low Distortion Wideband Reverse Amplifier Module

MHW1254L

24 Vdc, 50 MHz, 25 dB
CATV LOW CURRENT AMPLIFIER

Designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for low–split, 2–way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Insure Good Low Frequency Gain Stability versus Temperature



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{IN}	+70	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 ohm system, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Bandwidth		BW	5.0	50	MHz
Power Gain	(f = 5.0 MHz)	Gp	24.3	25.8	dB
Return Loss	(@ f = 5.0–50 MHz)	RL	20	—	dB
Second Order Distortion	(V_{out} = +50 dBmV/ch)	IMD	—	–70	dBc
Cross Modulation	(V_{out} = +50 dBmV/ch)	XMD_4	—	–62	dBc
Triple Beat Distortion	(V_{out} = +50 dBmV/ch)	TB_3	—	–70	dBc
Noise Figure	(f = 50 MHz)	NF	—	4.5	dB
DC Current		IDC	100	135	mA

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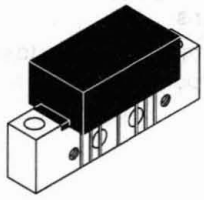
- Guaranteed Broadband Noise Figure
- All Gold Metallization
- Designed to Ensure Good Gain Stability versus Temperature

MHW1254LA

5–65 MHz, 25.5 dB
CATV LOW CURRENT AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Bandwidth	All	BW	5	—	65	MHz
Power Gain	(f = 5 MHz)	G_p	25	25.5	26	dB
Slope	(5–65 MHz)	S	– 0.2	—	0.5	dB
Gain Flatness (Peak To Valley)	(5–65 MHz)	—	—	—	0.4	dB
Return Loss — Input/Output	(@ f = 5–65 MHz)	IRL/ORL	20	—	—	dB
Composite Second Order (V_{out} = +50 dBmV per Ch., Worst Case)						dB
	6–Channel FLAT	CSO_6	—	– 73	– 68	
	10–Channel FLAT	CSO_{10}	—	– 71	– 66	

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	XMD_6	—	–69	–65	
10–Channel FLAT	XMD_{10}	—	–64	–61	
Composite Triple Beat (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	CTB_6	—	–78	–75	
10–Channel FLAT	CTB_{10}	—	–69	–66	
Noise Figure	NF				dB
(f = 5–65 MHz)		—	5.8	6.5	
DC Current	I_{DC}	85	95	110	mA

The RF Line

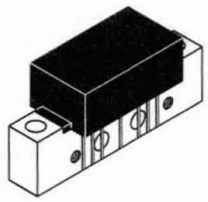
Low Distortion Wideband Reverse Amplifier Modules

Designed specifically for broadband applications requiring low multi–channel distortion characteristics. Specified for use as return amplifiers for 2–way cable TV systems.

- Designed for Low Power Consumption
- Specified for 6 and 10 Channel Performance
- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- All Gold Metallization
- Designed to Ensure Good Gain Stability versus Temperature

MHW1303LA

5–200 MHz, 30.8 dB
CATV LOW CURRENT AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Bandwidth	All	BW	5	—	200	MHz
Power Gain	(f = 5 MHz)	G_p	30	30.8	31.2	dB
Slope	(5–200 MHz)	S	0	—	1.0	dB
Gain Flatness (Peak To Valley)	(5–200 MHz)	—	—	—	0.7	dB
Return Loss — Input/Output		IRL/ORL				dB
	(@ f = 5–65 MHz)		20	—	—	
	(@ f = 65–200 MHz)		18	—	—	
Composite Second Order (V_{out} = +50 dBmV per Ch., Worst Case)						dB
	6–Channel FLAT	CSO_6	—	– 73	– 68	
	10–Channel FLAT	CSO_{10}	—	– 70	– 65	

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	XMD_6	—	–67	–64	
10–Channel FLAT	XMD_{10}	—	–61	–58	
Composite Triple Beat (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	CTB_6	—	–76	–74	
10–Channel FLAT	CTB_{10}	—	–67	–64	
Noise Figure	NF				dB
(f = 5–200 MHz)		—	5	5.7	
DC Current	I_{DC}	85	95	110	mA

The RF Line

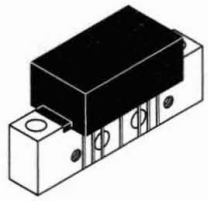
Low Distortion Wideband Reverse Amplifier Modules

Designed specifically for broadband applications requiring low multi–channel distortion characteristics. Specified for use as return amplifiers for 2–way cable TV systems.

- Designed for Low Power Consumption
- Specified for 6 and 10 Channel Performance
- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- All Gold Metallization
- Designed to Ensure Good Gain Stability versus Temperature

MHW1304LA

5–65 MHz, 30.8 dB
CATV LOW CURRENT AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Bandwidth	All	BW	5	—	65	MHz
Power Gain	(f = 5 MHz)	G_p	30	30.8	31.2	dB
Slope	(5–65 MHz)	S	– 0.2	—	0.5	dB
Gain Flatness (Peak To Valley)	(5–65 MHz)	—	—	—	0.5	dB
Return Loss — Input/Output	(@ f = 5–65 MHz)	IRL/ORL	20	—	—	dB
Composite Second Order (V_{out} = +50 dBmV per Ch., Worst Case)	6–Channel FLAT	CSO_6	—	– 73	– 68	dB
	10–Channel FLAT	CSO_{10}	—	– 70	– 65	

REV 1

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	XMD_6	—	–67	–64	
10–Channel FLAT	XMD_{10}	—	–61	–58	
Composite Triple Beat (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	CTB_6	—	–76	–74	
10–Channel FLAT	CTB_{10}	—	–67	–64	
Noise Figure	NF				dB
(f = 5–65 MHz)		—	5	5.7	
DC Current	I_{DC}	85	95	110	mA

The RF Line

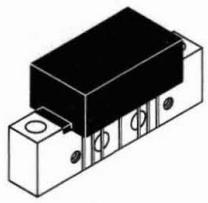
Low Distortion Wideband Reverse Amplifier Modules

Designed specifically for broadband applications requiring low multi–channel distortion characteristics. Specified for use as return amplifiers for 2–way cable TV systems.

- Designed for Low Power Consumption
- Specified for 6 and 10 Channel Performance
- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- All Gold Metallization
- Designed to Ensure Good Gain Stability versus Temperature

MHW1353LA

5–150 MHz, 35.2 dB
CATV LOW CURRENT AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Bandwidth	All	BW	5	—	150	MHz
Power Gain	(f = 5 MHz)	G_p	34.5	35.2	35.7	dB
Slope	(5–150 MHz)	S	0	—	1	dB
Gain Flatness (Peak To Valley)	(5–150 MHz)	—	—	—	0.7	dB
Return Loss — Input/Output		IRL/ORL				dB
	(@ f = 5–65 MHz)		20	—	—	
	(@ f = 65–150 MHz)		18	—	—	
Composite Second Order (V_{out} = +50 dBmV per Ch., Worst Case)						dB
	6–Channel FLAT	CSO_6	—	– 73	– 68	
	10–Channel FLAT	CSO_{10}	—	– 69	– 65	

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	XMD_6	—	–66	–63	
10–Channel FLAT	XMD_{10}	—	–60	–57	
Composite Triple Beat (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	CTB_6	—	–75	–73	
10–Channel FLAT	CTB_{10}	—	–65	–62	
Noise Figure	NF				dB
(f = 5–150 MHz)		—	4.4	5.4	
DC Current	I_{DC}	85	95	110	mA

The RF Line

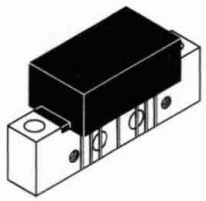
Low Distortion Wideband Reverse Amplifier Module

Designed specifically for broadband applications requiring low multi–channel distortion characteristics. Specified for use as return amplifiers for 2–way cable TV systems.

- Designed for Low Power Consumption
- Specified for 6 and 10 Channel Performance
- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- All Gold Metallization
- Designed to Ensure Good Gain Stability versus Temperature

MHW1354LA

5–65 MHz, 35.2 dB
CATV LOW CURRENT AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Bandwidth	All	BW	5	—	65	MHz
Power Gain	(f = 5 MHz)	G_p	34.5	35.2	35.7	dB
Slope	(5–65 MHz)	S	– 0.2	—	0.5	dB
Gain Flatness (Peak To Valley)	(5–65 MHz)	—	—	—	0.5	dB
Return Loss — Input/Output	(@ f = 5–65 MHz)	IRL/ORL	20	—	—	dB
Composite Second Order (V_{out} = +50 dBmV per Ch., Worst Case)						dB
	6–Channel FLAT	CSO_6	—	– 73	– 68	
	10–Channel FLAT	CSO_{10}	—	– 69	– 65	

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	XMD_6	—	–66	–63	
10–Channel FLAT	XMD_{10}	—	–60	–57	
Composite Triple Beat (V_{out} = +50 dBmV per Ch., Worst Case)					dB
6–Channel FLAT	CTB_6	—	–75	–73	
10–Channel FLAT	CTB_{10}	—	–65	–62	
Noise Figure	NF				dB
(f = 5–65 MHz)		—	4.4	5.4	
DC Current	I_{DC}	85	95	110	mA

The RF Line

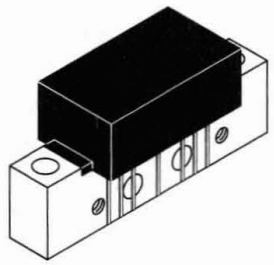
77-Channel (550 MHz) CATV Amplifier

The MHW6342T is designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- Specified for 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 34.5 dB (Typ) @ 50 MHz
  35.2 dB (Typ) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 5.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion–Implanted Transistors

MHW6342T

34 dB GAIN
550 MHz
77–CHANNEL
CATV AMPLIFIER



CASE 1302–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz	G_p	33.5	34.5	35.5	dB
Power Gain	550 MHz	G_p	34.5	35.2	—	dB
Slope		S	0	0.7	2	dB
Gain Flatness (Peak To Valley)		—	—	0.3	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz 450–550 MHz	IRL/ORL	18 16	— —	— —	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — —	 –80 –74	 — —	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60–Channel FLAT 77–Channel FLAT	 XMD_{60} XMD_{77}	 — —	 –62 –63	 — –57	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60–Channel FLAT 77–Channel FLAT	 CTB_{60} CTB_{77}	 — —	 –64 –63	 — –57	dB
Composite Second Order (V_{out} = +46 dBmV/ch, 60–Channel FLAT) (V_{out} = +44 dBmV/ch, 77–Channel FLAT)		 CSO_{60} CSO_{77}	 — —	 –70 –65	 — –57	dB
Noise Figure	550 MHz	NF	—	5.5	6.5	dB
DC Current		I_{DC}	—	310	340	mA

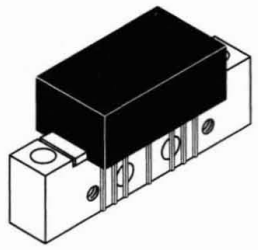
The RF Line

110-Channel 750 MHz CATV Amplifier

MHW7182B

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 750 MHz
  G_p = 19 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ) @ 750 MHz
- All Gold Metallization
- Improved Distortion Performance

18 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	18 18.2	18.5 19	19 20	dB
Slope	40–750 MHz	S	0	0.4	1	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.005	 dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CSO_{110} CSO_{77}	 — —	 –70 –70	 –63 –64	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 77–Channel FLAT	 XMD_{110} XMD_{77}	 — —	 –66 –61	 –64 –59	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CTB_{110} CTB_{77}	 — —	 –68 –66	 –66 –64	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	4.0 4.5 5.0	5.0 — 6.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	180	220	240	mA

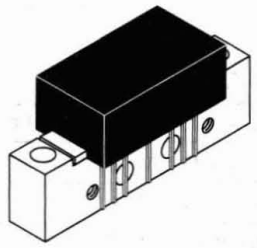
The RF Line

High Output Power Doubler 750 MHz CATV Amplifier

MHW7185C

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 6.2 dB (Typ) @ 750 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

19.4 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	18.3 19	18.8 19.4	19.3 20	dB
Slope	40–750 MHz	S	0	0.4	1.0	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL				
	@ 40 MHz		19	—	—	dB
	@ f > 40 MHz (Derate)		—	—	0.006	dB/MHz
Composite Second Order						dBc
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–72	–64	
	77–Channel FLAT	CSO_{77}	—	–80	–68	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +44 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–66	–63	
	77–Channel FLAT	XMD_{77}	—	–70	–68	
Composite Triple Beat						dBc
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–64	–62	
	77–Channel FLAT	CTB_{77}	—	–71	–69	
Noise Figure	50 MHz	NF	—	5.0	6.0	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	7.5	
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

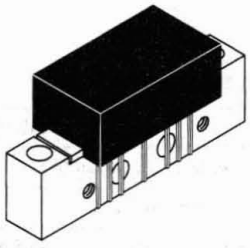
The RF Line

High Output Power Doubler 750 MHz CATV Amplifier

MHW7205C

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 20.2 dB (Typ)
- Broadband Noise Figure
  NF = 6.2 dB (Typ) @ 750 MHz
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 110–Channel Loading
  CTB = –63 dB (Typ)

20.2 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	19.3 20	19.8 20.2	20.3 21	dB
Slope	40–750 MHz	S	0	0.4	1.0	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 19 —	 — —	 — 0.006	 dB dB/MHz
Composite Second Order (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CSO_{110} CSO_{77}	 — —	 –70 –80	 –63 –68	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 77–Channel FLAT	 XMD_{110} XMD_{77}	 — —	 –67 –70	 –62 –68	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CTB_{110} CTB_{77}	 — —	 –63 –71	 –61 –69	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	5.0 5.8 6.2	6.0 — 7.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

The RF Line

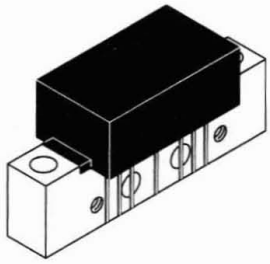
110-Channel (750 MHz) CATV Amplifier

MHW7222B

750 MHz
22.7 dB GAIN
110–CHANNEL
CATV AMPLIFIER

The MHW7222B is designed specifically for up to 750 MHz CATV systems as amplifiers in trunk, bridge and line extender applications. This amplifier features ion–implanted, arsenic emitter transistors, an all gold metallization system and offers improved ruggedness and distortion performance.

- Specified for 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 22.7 dB Typ @ 750 MHz
- Broadband Noise Figure
  NF = 5.0 dB Typ @ 750 MHz
- All Gold Metallization



CASE 1302–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	f = 50 MHz f = 750 MHz	G_p	21.4 22.2	21.9 22.7	22.4 23.2	dB
Slope (f = 40–750 MHz)		S	0.2	0.7	1.2	—
Gain Flatness (Peak To Valley)	(f = 40–750 MHz)	G_f	—	0.4	0.6	—
Input/Output Return Loss @ f = 40 MHz		IRL/ORL	20	25	—	dB
Derate Return Loss @ f > 40 MHz		RLD	—	—	0.006	dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch; 110 Channels) (V_{out} = +44 dBmV/ch; 77 Channels)		 CSO_{110} CSO_{77}	 — —	 –67 –67	 –60 –60	dB

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion					dBc
(V_{out} = +40 dBmV/ch, 110–Channel @ Fm = 55.25 MHz)	XMD_{110}	—	–63	–60	
(V_{out} = +44 dBmV/ch, 77–Channel @ Fm = 55.25 MHz)	XMD_{77}	—	–59	–56	
Composite Triple Beat					dBc
(V_{out} = +40 dBmV/ch, 110–Channels, Worst Case)	CTB_{110}	—	–64	–61	
(V_{out} = +44 dBmV/ch, 77–Channels, Worst Case)	CTB_{77}	—	–65	–62	
Noise Figure f = 50 MHz	NF	—	3.7	4.5	dB
f = 750 MHz		—	5	6.5	
DC Current	I_{DC}	180	220	240	mA

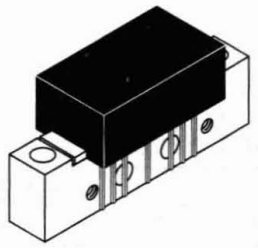
The RF Line

110-Channel (750 MHz) CATV Line Extender Amplifier

MHW7242A

- Specified for 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 24 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Max) @ 750 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Improved CTB Performance

750 MHz
24 dB GAIN
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	23.2 24	24 24.7	24.8 26	dB
Slope	40–750 MHz	S	0	0.6	1.5	dB
Gain Flatness (40–750 MHz, Peak To Valley)		—	—	0.4	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CSO_{110} CSO_{77}	 — —	 –69 –78	 –62 —	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 110–Channel FLAT 77–Channel FLAT	 XMD_{110} XMD_{77}	 — —	 –63 –58	 –61 —	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 110–Channel FLAT 77–Channel FLAT	 CTB_{110} CTB_{77}	 — —	 –67 –64	 –63 —	dBc
Noise Figure	50 MHz 750 MHz	NF	— —	4.8 5.5	5.5 7	dB
DC Current		I_{DC}	280	318	350	mA

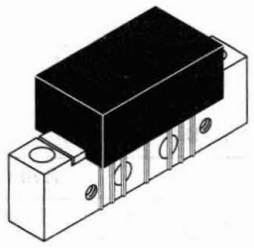
The RF Line

110-Channel (750 MHz) CATV Line Extender Amplifier

MHW7272A

- 24 V Supply Voltage
- Specified for 110–Channel Performance
- Typical Noise Figure
  NF = 5.5 dB @ 750 MHz
- All Gold Metallization
- Improved CTB Performance over Previous Versions

27 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	26.2 27	27.2 27.7	27.8 29	dB
Slope	40–750 MHz	S	0	0.7	1.5	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–70	–64	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–63	–60	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–68	–64	dBc
Noise Figure	50 MHz 750 MHz	NF	— —	— 5.5	5.5 6.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

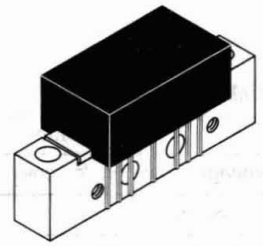
The RF Line

128-Channel 860 MHz CATV Amplifier

MHW8182B

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 860 MHz
  G_p = 19.1 dB (Typ)
- Broadband Noise Figure
  NF = 5.5 dB (Typ) @ 860 MHz
- All Gold Metallization
- Improved CTB Distortion Performance

18 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	18 18.2	18.5 19.1	19 20.5	dB
Slope	40–860 MHz	S	0	0.7	2.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	 20 —	 — —	 — 0.005	 dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case) (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –71 –70 –70	 –64 –63 –64	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz) (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{110} XMD_{77}	 — — —	 –68 –66 –61	 –65 –64 –59	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case) (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{110} CTB_{77}	 — — —	 –69 –68 –66	 –66 –66 –64	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 860 MHz	NF	— — — —	4.0 4.5 5.0 5.5	5.0 — 6.5 7.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	180	220	240	mA

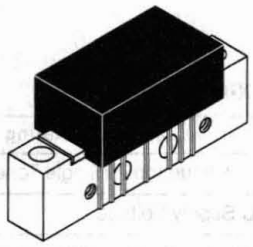
The RF Line

High Output Power Doubler 860 MHz CATV Amplifier

MHW8185

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Typ) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

19.4 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	18.3 19	18.8 19.4	19.3 20.5	dB
Slope	40–860 MHz	S	0	.5	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL				
	@ 40 MHz		19	—	—	dB
	@ f > 40 MHz (Derate)		—	—	0.006	dB/MHz
Composite Second Order						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	–70	–62	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–72	–64	
	77–Channel FLAT	CSO_{77}	—	–80	–68	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +40 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–72	–64	
(V_{out} = +44 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–67	–63	
	77–Channel FLAT	XMD_{77}	—	–70	–68	
Composite Triple Beat						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–67	–64	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–64	–62	
	77–Channel FLAT	CTB_{77}	—	–71	–69	
Noise Figure	50 MHz	NF	—	5.0	6.0	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	—	
	860 MHz		—	7.0	8.0	
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

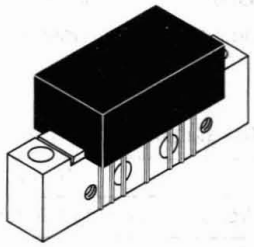
The RF Line

High Output Power Doubler 870 MHz CATV Amplifier

MHW8185L

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–870 MHz
  G_p = 19.4 dB (Typ)
- Lower DC Current Consumption
- Superior DC Current Stability with Temperature

19.4 dB GAIN
870 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

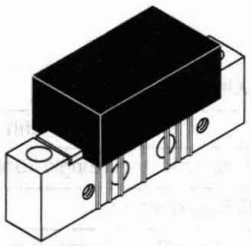
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	870	MHz
Power Gain	50 MHz 870 MHz	G_p	18 19	18.5 19.4	19 20.5	dB
Slope	40–870 MHz	S	0.4	0.9	1.4	dB
Gain Flatness (40–870 MHz, Peak–to–Valley)		—	—	0.3	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL				
	@ 40 MHz		20	—	—	dB
	@ f > 40 MHz (Derate)		—	—	0.007	dB/MHz
Composite Second Order						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	–69	–62	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–70	–64	
(V_{out} = +44 dBmV/ch., Worst Case)	77–Channel FLAT	CSO_{77}	—	–85	–68	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +40 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–72	–64	
(V_{out} = +44 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–66	–63	
(V_{out} = +44 dBmV/ch., FM = 55 MHz)	77–Channel FLAT	XMD_{77}	—	–69	–67	
Composite Triple Beat						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–66	–63	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–63	–61	
(V_{out} = +44 dBmV/ch., Worst Case)	77–Channel FLAT	CTB_{77}	—	–70	–68	
Noise Figure	50 MHz	NF	—	5.3	6.2	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.6	—	
	870 MHz		—	7.8	8.5	
DC Current (V_{DC} = 24 V, T_C = –20 to +100°C)		I_{DC}	345	365	385	mA

The RF Line
High Output Power Doubler 860 MHz CATV Amplifier

MHW8205

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 20.2 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Typ) @ 860 MHz
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 128–Channel Loading
  CTB = –66 dB (Typ)

20.2 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	19.3 20	19.8 20.2	20.3 21.5	dB
Slope	40–860 MHz	S	0	.4	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL				
	@ 40 MHz		19	—	—	dB
	@ f > 40 MHz (Derate)		—	—	0.006	dB/MHz
Composite Second Order						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	–69	–60	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–70	–63	
	77–Channel FLAT	CSO_{77}	—	–80	–68	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +40 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–72	–64	
(V_{out} = +44 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–67	–62	
	77–Channel FLAT	XMD_{77}	—	–71	–68	
Composite Triple Beat						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–66	–63	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–63	–61	
	77–Channel FLAT	CTB_{77}	—	–71	–69	
Noise Figure	50 MHz	NF	—	5.0	6.0	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	—	
	860 MHz		—	7.0	8.0	
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

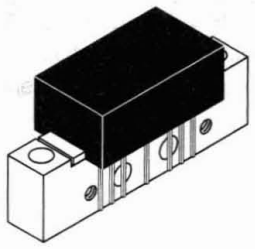
The RF Line

High Output Power Doubler 870 MHz CATV Amplifier

MHW8205L

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 870 MHz
  G_p = 20.4 dB (Typ)
- Broadband Noise Figure
  NF = 7.7 dB (Typ) @ 870 MHz
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 128–Channel Loading
  CTB = –66 dB (Typ)
- Lower DC Current Consumption and Superior DC Stability with Temperature

20.4 dB GAIN
870 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	870	MHz
Power Gain	50 MHz 870 MHz	G_p	19 19.8	19.5 20.4	20 21.3	dB
Slope	40–870 MHz	S	0.2	0.8	1.7	dB
Gain Flatness (40–870 MHz, Peak to Valley)		—	—	0.5	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL				
	@ 40 MHz		20	—	—	dB
	@ f > 40 MHz (Derate)		—	—	0.007	dB/MHz
Composite Second Order						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	–69	–60	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–70	–63	
	77–Channel FLAT	CSO_{77}	—	–80	–67	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +40 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–72	–64	
(V_{out} = +44 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–65	–62	
	77–Channel FLAT	XMD_{77}	—	–69	–66	
Composite Triple Beat						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–66	–63	
(V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–63	–61	
	77–Channel FLAT	CTB_{77}	—	–70	–68	
Noise Figure	50 MHz	NF	—	5.0	6.2	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	—	
	870 MHz		—	7.7	8.5	
DC Current (V_{DC} = 24 V, T_C = –20°C to +100°C)		I_{DC}	345	365	385	mA

The RF Line

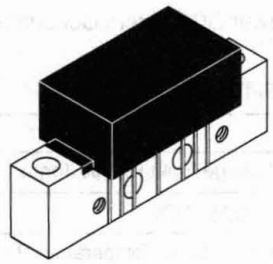
128-Channel (860 MHz) CATV Amplifier

MHW8222B

860 MHz
22.7 dB GAIN
128–CHANNEL
CATV AMPLIFIER

The MHW8222B is designed specifically for up to 860 MHz CATV systems as amplifiers in trunk, bridge and line extender applications. This amplifier features ion–implanted, arsenic emitter transistors, an all gold metallization system and offers improved ruggedness and distortion performance.

- Specified for 77, 110, 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 22.7 dB Typ @ 860 MHz
- Broadband Noise Figure
  NF = 5.6 dB Typ @ 860 MHz
- All Gold Metallization
- Improved Distortion Performance



CASE 1302–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	f = 50 MHz f = 860 MH	G_p	21.4 21.8	21.9 22.7	22.4 24	dB
Slope (f = 40–860 MHz)		S	0.1	0.8	1.5	—
Gain Flatness (Peak To Valley)	(f = 40–860 MHz)	G_f	—	0.4	0.6	—
Input/Output Return Loss @ f = 40 MHz		IRL/ORL	20	24	—	dB
Derate Return Loss @ f > 40 MHz		RLD	—	—	0.009	dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch; 128 Channels) (V_{out} = +40 dBmV/ch; 110 Channels) (V_{out} = +44 dBmV/ch; 77 Channels)		 CSO_{128} CSO_{110} CSO_{77}	 — — —	 –68 –64 –65	 –60 –61 –62	dB

ELECTRICAL CHARACTERISTICS — continued

Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion						dBc
(V_{out} = +38 dBmV/ch, 128–Channel @ Fm = 55.25 MHz)		XMD_{128}	—	–65	–63	
(V_{out} = +40 dBmV/ch, 110–Channel @ Fm = 55.25 MHz)		XMD_{110}	—	–63	–60	
(V_{out} = +44 dBmV/ch, 77–Channel @ Fm = 55.25 MHz)		XMD_{77}	—	–59	–56	
Composite Triple Beat						dBc
(V_{out} = +38 dBmV/ch, 128–Channels, Worst Case)		CTB_{128}	—	–66	–64	
(V_{out} = +40 dBmV/ch, 110–Channels, Worst Case)		CTB_{110}	—	–64	–61	
(V_{out} = +44 dBmV/ch, 77–Channels, Worst Case)		CTB_{77}	—	–65	–62	
Noise Figure	f = 50 MHz	NF	—	3.7	4.5	dB
	f = 750 MHz		—	5	6.5	
	f = 860 MHz		—	5.6	7	
DC Current		I_{DC}	180	220	240	mA

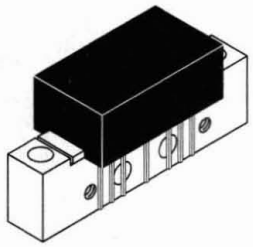
The RF Line

128-Channel (860 MHz) CATV Line Extender Amplifier

MHW8242A

- Specified for 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 24 dB (Typ)
- Broadband Noise Figure
  NF = 7.5 dB (Max) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Improved CTB Performance

860 MHz
25 dB GAIN
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	23.2 24	24 25	24.8 26	dB
Slope	40–860 MHz	S	0	0.8	1.8	dB
Gain Flatness (40–860 MHz, Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 77–Channel FLAT	 CSO_{128} CSO_{77}	 — —	 –69 –78	 –62 —	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	 128–Channel FLAT 77–Channel FLAT	 XMD_{128} XMD_{77}	 — —	 –65 –58	 –62 —	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	 128–Channel FLAT 77–Channel FLAT	 CTB_{128} CTB_{77}	 — —	 –68 –64	 –64 —	dBc
Noise Figure	50 MHz 860 MHz	NF	— —	4.8 5.8	5.5 7.5	dB
DC Current		I_{DC}	280	318	350	mA

REV 3

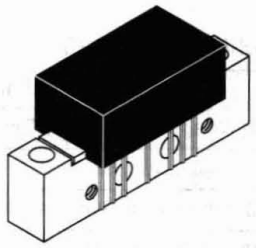
The RF Line

128-Channel (860 MHz) CATV Line Extender Amplifier

MHW8272A

- Specified for 128–Channel Performance
- Broadband Power Gain — @ f = 50 MHz
  G_p = 27.2 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 860 MHz
- All Gold Metallization
- Improved CTB Performance over Previous Version

27 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	26.2 27	27.2 27.7	27.8 29.5	dB
Slope	40–860 MHz	S	0	0.6	2	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	 @ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	 20 —	 — —	 — 0.007	 dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	–69	–64	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–65	–62	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–69	–64	dBc
Noise Figure	50 MHz 860 MHz	NF	— —	— 6.0	5.5 7.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

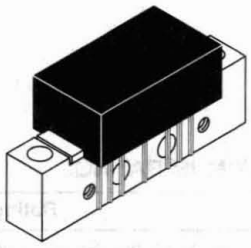
The RF Line

152-Channel 1000 MHz CATV Amplifier

MHW9182B

- Specified for 152–Channel Performance
- Broadband Power Gain — @ f = 1000 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 1000 MHz
- All Gold Metallization
- Improved Ruggedness and Composite Second Order Distortion Performance

19.4 dB GAIN
1000 MHz
152–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	1000	MHz
Power Gain	50 MHz 1000 MHz	G_p	18 18.7	18.5 19.4	19 20.7	dB
Slope	40–1000 MHz	S	0.4	0.9	1.4	dB
Gain Flatness (40–1000 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL				
	@ 40 MHz		20	—	—	dB
	@ f > 40 MHz (Derate)		—	—	0.006	dB/MHz
Composite Second Order						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	70	–63	
(V_{out} = +38 dBmV/ch., Worst Case)	152–Channel FLAT	CSO_{152}	—	–69	–63	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +40 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–66	–64	
(V_{out} = +38 dBmV/ch., FM = 55 MHz)	152–Channel FLAT	XMD_{152}	—	–65	–61	
Composite Triple Beat						dBc
(V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–68	–66	
(V_{out} = +38 dBmV/ch., Worst Case)	152–Channel FLAT	CTB_{152}	—	–64	–61	
Noise Figure	50 MHz	NF	—	4.0	5.0	dB
	550 MHz		—	4.5	—	
	860 MHz		—	5.5	—	
	1000 MHz		—	6.0	7.5	
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	180	210	240	mA

The RF Line

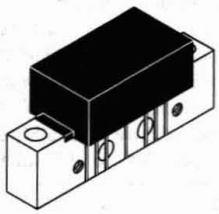
Gallium Arsenide 870 MHz CATV Amplifier

High Output Power Doubler

- Designed for Maximum Output Capability Under Tilted Output Levels
- Specified for 79–, 112– and 132–Channel Performance
- Broadband Power Gain
- Broadband Noise Figure
  NF = 4.0 dB (Typ)
- Specified at High Output Levels (48 dBmV/ch) Under Flat Output Levels
- Superior DC Current Stability with Temperature

MHW9187

870 MHz
20 dB GAIN
132–CHANNEL
GaAs CATV AMPLIFIER



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000–4–5	200	200	V
Human Body Model per Mil. Std. 1686	0.7	2	kV

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +45°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	870	MHz
Power Gain	870 MHz	G_p	19.4	20	20.6	dB
Slope	40–870 MHz	S	0	0.5	1.0	dB
Gain Flatness (40–870 MHz, Peak–to–Valley)		—	—	—	0.5	dB
Return Loss — Input (Z_o = 75 Ohms)	40–500 Mhz 501–750 Mhz 751–870 Mhz	IRL	 20 18 16	 — — —	 — — —	dB
Return Loss — Output (Z_o = 75 Ohms)	40–160 Mhz f > 160 Mhz	ORL	 20 18	 — —	 — —	dB

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = +45°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Second Order						dBc
(V_{out} = +48 dBmV/ch., Worst Case)	132–Channel FLAT	CSO_{132}	—	–64	–62	
(V_{out} = +48 dBmV/ch., Worst Case)	112–Channel FLAT	CSO_{112}	—	–66	–64	
(V_{out} = +48 dBmV/ch., Worst Case)	79–Channel FLAT	CSO_{79}	—	–70	–68	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 12db Tilt	CSO_{112}	—	–65	–63	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 13.5db Tilt	CSO_{112}	—	–64	–62	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 17db Tilt	CSO_{112}	—	–63	–61	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 12db Tilt	CSO_{79}	—	–69	–67	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 13.5db Tilt	CSO_{79}	—	–74	–72	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 17db Tilt	CSO_{79}	—	–73	–71	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +48 dBmV/ch., FM = 55 MHz)	132–Channel FLAT	XMD_{132}	—	–57	–55	
(V_{out} = +48 dBmV/ch., FM = 55 MHz)	112–Channel FLAT	XMD_{112}	—	–59	–57	
(V_{out} = +48 dBmV/ch., FM = 55 MHz)	79–Channel FLAT	XMD_{79}	—	–62	–60	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 12db Tilt	XMD_{112}	—	–53	–51	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 13.5db Tilt	XMD_{112}	—	–55	–53	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 17db Tilt	XMD_{112}	—	–58	–56	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 12db Tilt	XMD_{79}	—	–60	–47	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 13.5db Tilt	XMD_{79}	—	–62	–60	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 17db Tilt	XMD_{79}	—	–67	–65	
Composite Triple Beat						dBc
(V_{out} = +48 dBmV/ch., Worst Case)	132–Channel FLAT	CTB_{132}	—	–60	–56	
(V_{out} = +48 dBmV/ch., Worst Case)	112–Channel FLAT	CTB_{112}	—	–64	–60	
(V_{out} = +48 dBmV/ch., Worst Case)	79–Channel FLAT	CTB_{79}	—	–68	–66	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 12db Tilt	CTB_{112}	—	–60	–58	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 13.5db Tilt	CTB_{112}	—	–61	–59	
(V_{out} = +56 dBmV @ 870 Mhz Equiv)	112–Channel, 17db Tilt	CTB_{112}	—	–64	–62	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 12db Tilt	CTB_{79}	—	–66	–64	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 13.5db Tilt	CTB_{79}	—	–71	–69	
(V_{out} = +58 dBmV @ 870 Mhz Equiv)	79–Channel, 17db Tilt	CTB_{79}	—	–74	–72	
Noise Figure	50 MHz	NF	—	4.0	4.5	dB
	550 MHz		—	3.5	4.5	
	750 MHz		—	3.5	4.5	
	870 MHz		—	4.0	4.5	
DC Current (V_{DC} = 24 V, T_C = 45°C)		I_{DC}	410	425	440	mA

NOTE: Typical specifications reflect that level of performance achieved by at least 85% of the units produced and sold.

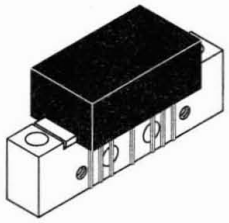
The RF Line

152-Channel (1000 MHz) CATV Line Extender Amplifier

MHW9242A

- Specified for 152–Channel Performance
- Broadband Power Gain — @ f = 40–1000 MHz
  G_p = 24 dB
- Broadband Noise Figure
  NF = 8 dB (Max) @ 1000 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

1000 MHz
24 dB GAIN
152–CHANNEL
CATV AMPLIFIER



CASE 714Y–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	1000	MHz
Power Gain	50 MHz 1000 MHz	G_p	23.2 24	— —	24.8 26	dB
Slope	40–1000 MHz	S	0	—	2.5	dB
Gain Flatness (40–1000 MHz, Peak–to–Valley)		—	—	—	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms) @ f > 40 MHz (Derate)	@ 40 MHz	IRL/ORL	20 —	— —	— 0.01	dB dB/MHz
Composite Second Order						dBc
(V_{out} = +38 dBmV/ch; Worst Case)	152–Channel FLAT	CSO_{152}	—	–66	–61	
(V_{out} = +38 dBmV/ch; Worst Case)	128–Channel FLAT	CSO_{128}	—	–69	—	
(V_{out} = +40 dBmV/ch;Worst Case)	110–Channel FLAT	CSO_{110}	—	–69	—	
(V_{out} = +44 dBmV/ch; Worst Case)	77–Channel FLAT	CSO_{77}	—	–78	—	
Cross Modulation Distortion @ Ch 2						dBc
(V_{out} = +38 dBmV/ch., FM= 55 MHz)	152–Channel FLAT	XMD_{152}	—	–62	–59	
(V_{out} = +38 dBmV/ch, FM = 55.25 MHz)	128–Channel FLAT	XMD_{128}	—	–65	—	
(V_{out} = +40 dBmV/ch, FM = 55.25 MHz)	110–Channel FLAT	XMD_{110}	—	–63	—	
(V_{out} = +44 dBmV/ch, FM = 55.25 MHz)	77–Channel FLAT	XMD_{77}	—	–58	—	

ELECTRICAL CHARACTERISTICS — continued

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Triple Beat						dBc
(V_{out} = +38 dBmV/ch., Worst Case)	152–Channel FLAT	CTB_{152}	—	–64	–58	
(V_{out} = +38 dBmV/ch, Worst Case)	128–Channel FLAT	CTB_{128}	—	–68	—	
(V_{out} = +40 dBmV/ch, Worst Case)	110–Channel FLAT	CTB_{110}	—	–67	—	
(V_{out} = +44 dBmV/ch, Worst Case)	77–Channel FLAT	CTB_{77}	—	–64	—	
Noise Figure	f = 50 MHz	NF	—	4.8	5.5	dB
	f = 750 MHz		—	5.5	7.0	
	f = 860 MHz		—	5.8	7.5	
	f = 1000 MHz		—	—	8.0	
DC Current		I_{DC}	280	318	350	mA

Chapter Eight
Tape and Reel Specifications

Motorola offers the convenience of Tape and Reel packaging for our growing family of standard integrated circuit products. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

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Embossed Tape and Reel Data for Discretes	8.1–5

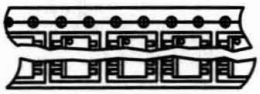
RF and IF Tape and Reel Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel–back" cover tape.

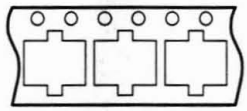
- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, –1, –2
- SOT–363 in 8 mm Tape
- Micro–8, QFN–32, PLD–1, PLD–1.5, NI–200S, NI–200Z in 12 mm Tape
- SO–16/16L, TSSOP–16 in 16 mm Tape
- SO–20L, SO–28L, TO–270 in 24 mm Tape
- NI–360, NI–360S, NI–400, NI–400S, NI–600 in 32 mm Tape
- TO–272, TO–272 Dual Lead in 44 mm Tape
- NI–780, NI–780S, NI–880, NI–880S in 56 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

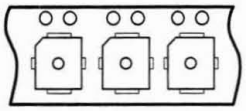
Micro–8 (12 mm)
SO–16/16L (16 mm)
SO–20L, SO–28L (24 mm)



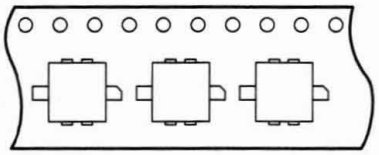
PLD–1 (12 mm)



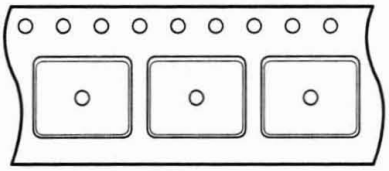
PLD–1.5 (12 mm)



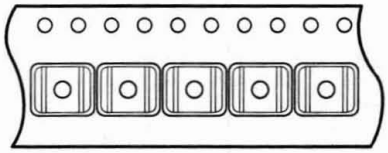
NI–200S, NI–200Z (12 mm)



PFP–16 (16 mm)

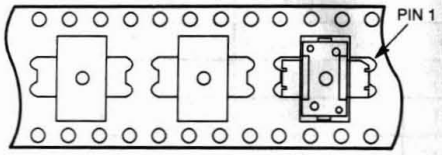


TSSOP–16 (16 mm)

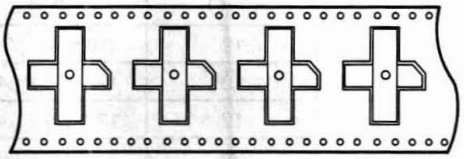


DIRECTION
OF FEED

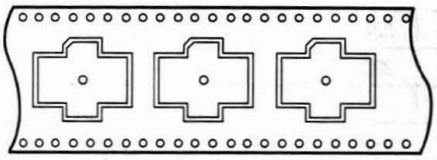
TO–270 (24 mm)



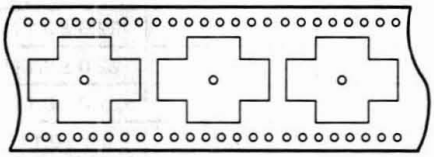
NI–360, NI–360S (32 mm)



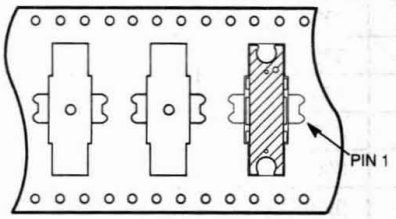
NI–400, NI–400S (32 mm)



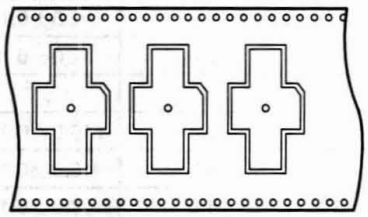
NI–600 (32 mm)



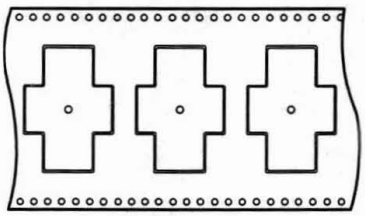
TO–272, TO–272 Dual Lead (44 mm)



NI–780, NI–780S (56 mm)



NI–880, NI–880S (56 mm)



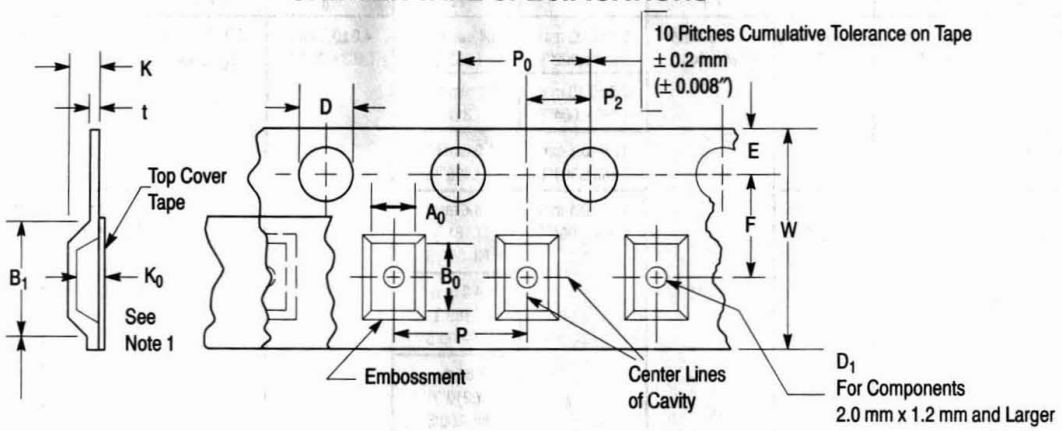
DIRECTION
OF FEED

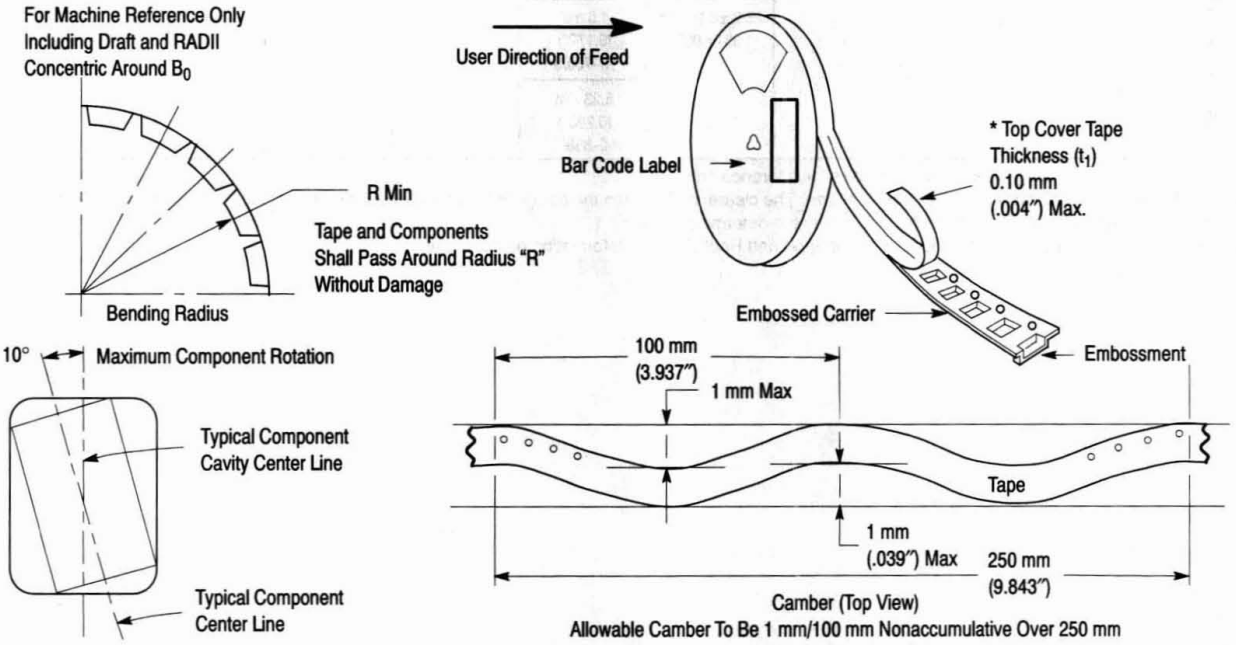
RF and IF EMBOSSED TAPE AND REEL ORDERING INFORMATION

Package	Tape Width (mm)	Pitch mm (inch)	Reel Size mm (inch)	Devices Per Reel and Minimum Order Quantity	Device Suffix
Micro–8	12	8.0 ± 0.1 (.315 ± .003)	330 (13)	2,500	R2
NI–200S (458B)	12	12.0 ± 0.1 (.471 ± .004)	178 (7)	500	R1
NI–200Z (458C)	12	12.0 ± 0.1 (.471 ± .004)	178 (7)	500	R1
NI–360 (360B)	32	24.0 ± 0.1 (.945 ± .004)	330 (13)	500	R1
NI–360S (360C)	32	24.0 ± 0.1 (.945 ± .004)	330 (13)	500	R1
NI–400 (465E)	32	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI–400S (465F)	32	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI–600 (465D)	32	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI–780 (465)	56	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI–780S (465A)	56	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI–880 (465B)	56	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI–880S (465C)	56	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
PLD–1	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
PLD–1.5	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
PFP–16	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,500	R2
QFN–24	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	2,500	R2
QFN–32 (5x5 mm)	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	2,500	R2
SO–16/16L	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
SO–20L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SO–28L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SOT–363	8	4.0 ± 0.1 (.157 ± .004)	178 (7)	3,000	T1
TO–270 (1265)	24	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	R1
TO–272 (1264)	44	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	T1
TO–272 Dual Lead (1337)	44	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	R1
TSSOP–16	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2

EMBOSSED TAPE AND REEL DATA FOR DISCRETES

CARRIER TAPE SPECIFICATIONS





DIMENSIONS

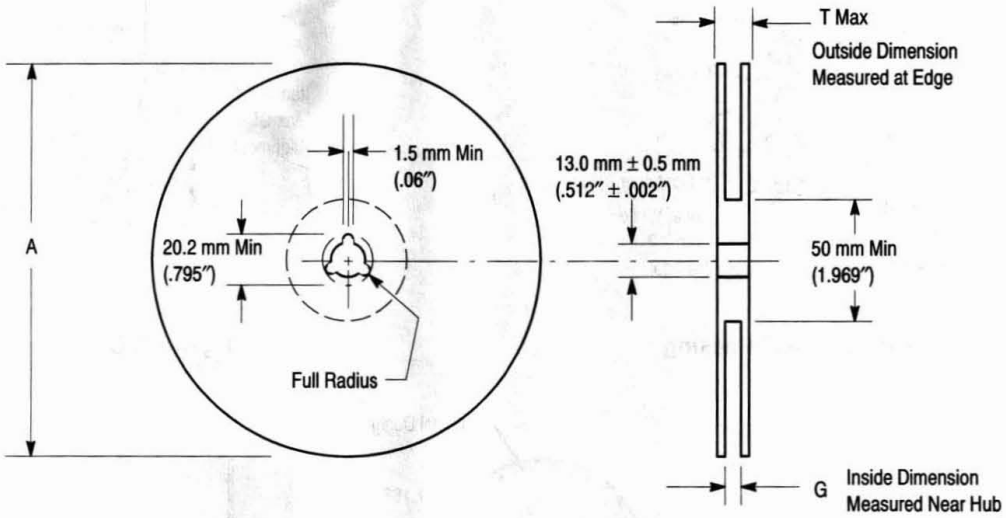
Tape Size	B_1 Max	D	D_1	E_1	F	K	P_0	P_2	R Min	t Max	W Max
12 mm	8.2 mm (.323″)	1.5+0.1 mm −0.0 (.059+.004″ −0.0)	1.5 mm Min (.060″)	1.75±0.1 mm (.069±.004″)	5.5±0.05 mm (.217±.002″)	6.4 mm Max (.252″)	4.0±0.1 mm (.157±.004″)	2.0±0.1 mm (.079±.004″)	30 mm (1.18″)	0.4 mm (.016″)	12±.30 mm (.470±.012″)
16 mm	12.1 mm (.476″)				7.5±0.10 mm (.295±.004″)	7.9 mm Max (.311″)					16.3 mm (.642″)
24 mm	20.1 mm (.791″)				11.5±0.1 mm (.453±.004″)	11.9 mm Max (.468″)					24.3 mm (.957″)
32 mm	23.0 mm (.906″)		1.5 mm Min (.059″)		14.2±0.1 mm (.559 ±.004″)	4.6 mm (.181″) NI-360/S			50 mm (1.969″)	0.6 mm (.024″)	32.2 mm (1.272″)
						4.3 mm (.169″) NI-400/S					
						5.34 mm (.210″) NI-600/S					
44 mm	35.0 mm (1.378″)		2.0 mm Min (.079″)		11.5±0.1 mm (.453±.004″)	15.9 mm Max (.625″)		2.0±0.15 mm (.079±.006″)			44±.30 mm (1.732±.012″)
56 mm	34.7 mm (1.366″)				26.2 ±0.15 mm (1.031±.006″)	4.5 mm (0.177″) NI-780/S					56±.30 mm (2.205± .012″)
						5.23 mm (0.206″) NI-880/S					

Metric dimensions govern — English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 3: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 8.1–4.

EMBOSSED TAPE AND REEL DATA FOR DISCRETES



Size	A Max	G	T Max
12 mm	330 mm (12.992″)	12.4 mm + 2.0 mm, –0.0 (.49″ + .079″, –0.00)	18.4 mm (.72″)
16 mm	360 mm (14.173″)	16.4 mm + 2.0 mm, –0.0 (.646″ + .078″, –0.00)	22.4 mm (.882″)
24 mm	360 mm (14.173″)	24.4 mm + 2.0 mm, –0.0 (.961″ + .070″, –0.00)	30.4 mm (1.197″)
32 mm	360 mm (14.163″)	32.4 mm + 2.0 mm, –0.0 (1.276″+ 0.79″, –0.00)	38.4 mm (1.512″)
44 mm	330 mm (12.992″)	44.4 mm + 2.0 mm, –0.0 (1.748″+ 0.79″, –0.00)	50.4 mm (1.984″)
56 mm	330 mm (12.992″)	56.4 mm + 2.0 mm, –0.0 (2.220″+ 0.79″, –0.00)	62 mm (2.441″)

Reel Dimensions

Metric Dimensions Govern — English are in parentheses for reference only

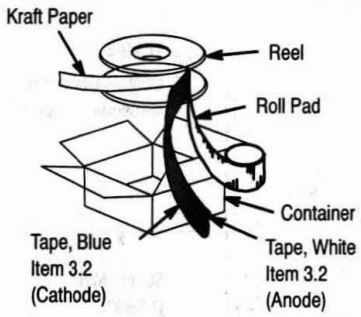


Figure 1. Reel Packing

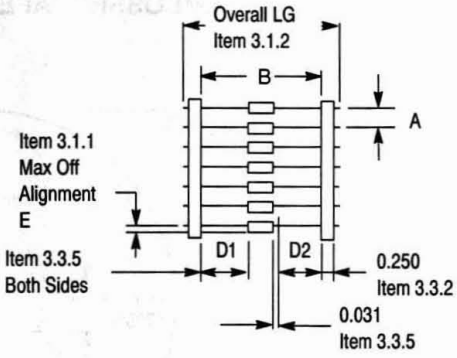


Figure 2. Component Spacing

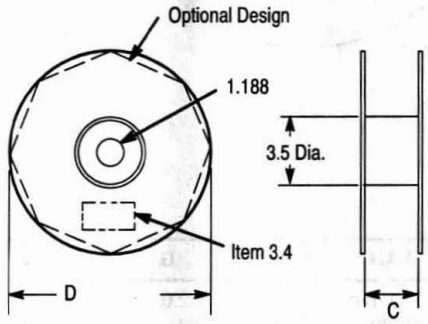


Figure 3. Reel Dimensions

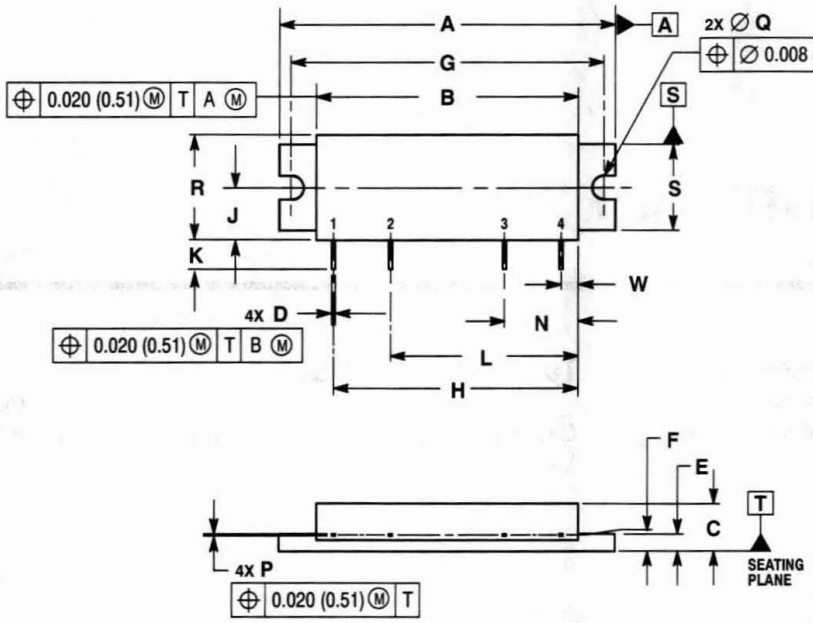
Chapter Nine
Packaging Information

The packaging availability for each device type is indicated on the individual data sheets and in the Selector Guide. All of the outline dimensions for the packages are given in this section.

Table of Contents

	Page
Case Dimensions	9.1–2

Case Dimensions



NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "F" TO CENTER OF LEADS.

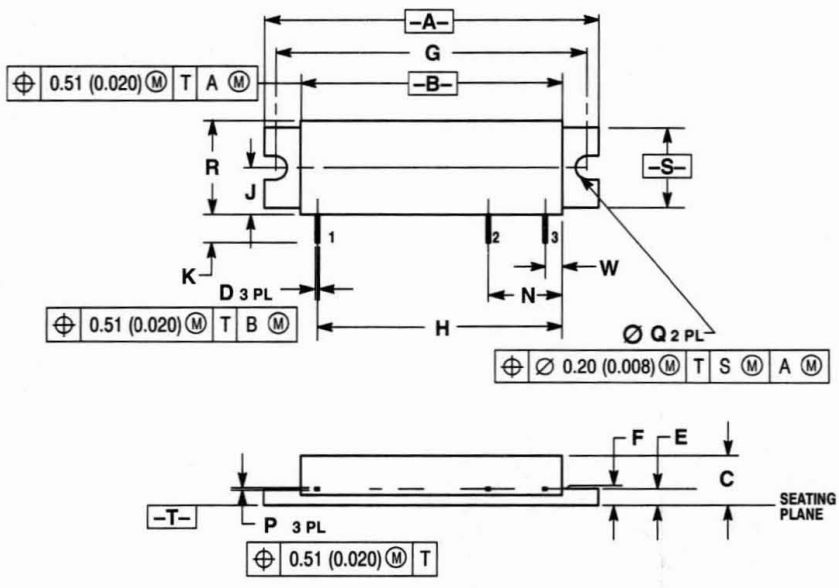
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
L	0.990 BSC		25.15 BSC	
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VDD1
3. VDD2
4. RF OUTPUT
CASE: GROUND

STYLE 2:
PIN 1. RF OUTPUT
2. VDD2
3. VDD1
4. RF INPUT
CASE: GROUND

STYLE 3:
PIN 1. RF INPUT
2. VBIAS
3. VDD
4. RF OUTPUT
CASE: GROUND

CASE 301AP–02
ISSUE C



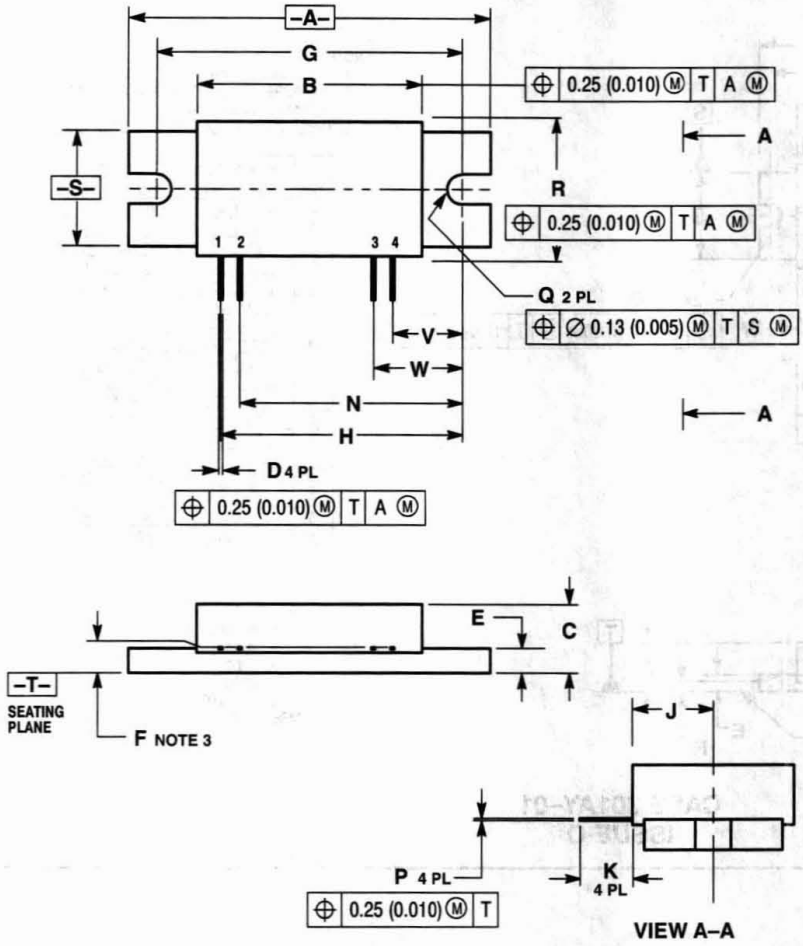
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VDD
3. RF OUTPUT
CASE: GROUND

CASE 301AS–01
ISSUE A

CASE DIMENSIONS (continued)



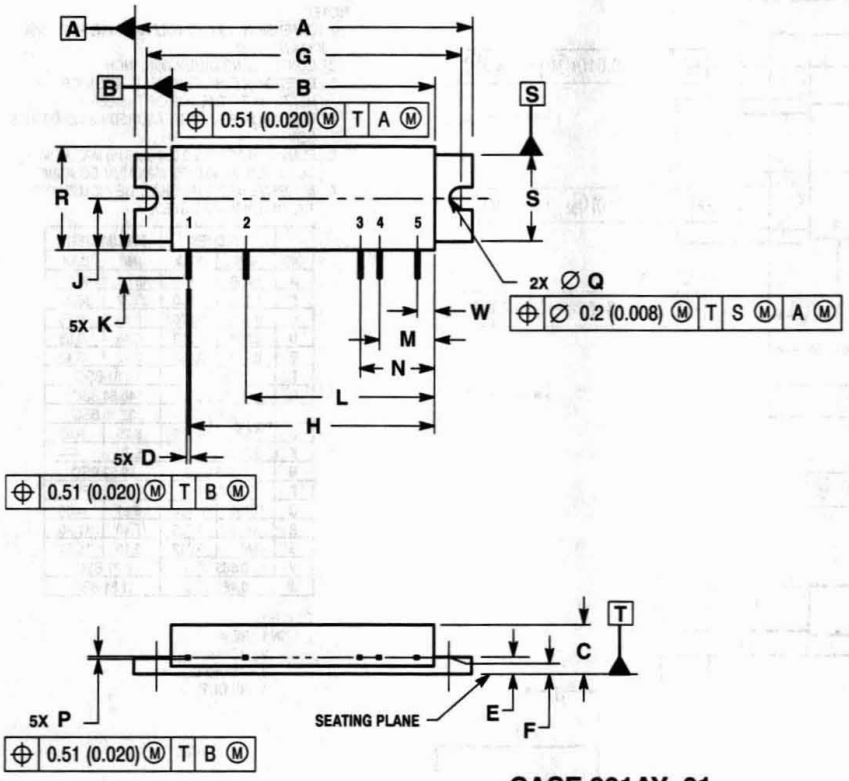
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F IS FROM THE BOTTOM OF HEATSINK TO THE TOP OF THE LEAD.
4. DIMENSION P TO BE MEASURED AS LEAD EXITS COVER.
5. FLANGE FLATNESS 0.038 (0.0015) MAXIMUM CONVEX, 0.063 (0.0025) MAXIMUM CONCAVE.
6. ADHESIVE MATERIAL SHALL BE INCLUDED IN THE DIMENSIONS LISTED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.890	1.910	48.01	48.51
B	1.170	1.190	29.72	30.22
C	0.350	0.376	8.89	9.55
D	0.018	0.022	0.46	0.55
E	0.115	0.135	2.92	3.42
F	0.170 BSC		4.31 BSC	
G	1.600 BSC		40.64 BSC	
H	1.265 BSC		32.13 BSC	
J	0.325	0.375	8.25	9.52
K	0.225	---	5.72	---
N	1.165 BSC		29.59 BSC	
P	0.010 REF		0.25 REF	
Q	0.150	0.160	3.81	4.06
R	0.685	0.705	17.40	17.90
S	0.598	0.612	15.18	15.54
V	0.365 BSC		9.27 BSC	
W	0.465 BSC		11.81 BSC	

STYLE 1:
PIN 1. RF IN
2. V BIAS
3. V SUPPLY
4. RF OUT

CASE 301AW–02
ISSUE B

CASE DIMENSIONS (continued)



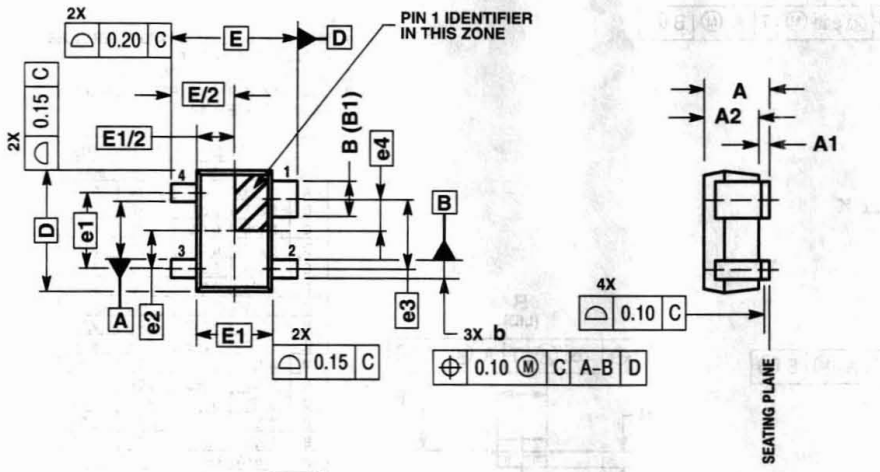
NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
3. DIMENSION F TO CENTER LINE OF LEADS.

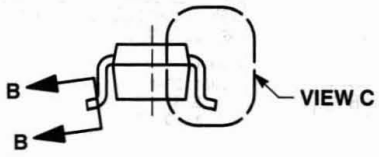
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	44.7	45.21	1.760	1.780
B	34.8	35.31	1.370	1.390
C	6.22	6.73	0.245	0.265
D	0.43	0.58	0.017	0.023
E	2.03	2.54	0.080	0.100
F	2.18 BSC		0.086 BSC	
G	41.91 BSC		1.650 BSC	
H	32.77 BSC		1.290 BSC	
J	6.76	7.11	0.266	0.280
K	3.18	4.19	0.125	0.165
L	25.15 BSC		0.990 BSC	
M	7.37 BSC		0.290 BSC	
N	9.91 BSC		0.390 BSC	
P	0.2	0.33	0.008	0.013
Q	3	3.35	0.118	0.132
R	13.59	14.1	0.535	0.555
S	11.3	11.81	0.445	0.465
W	2.29 BSC		0.090 BSC	

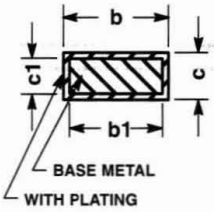
STYLE 1:
PIN 1. RF INPUT
2. VDD1
3. VDD2
4. VDD3
5. RF OUTPUT
CASE: GROUND

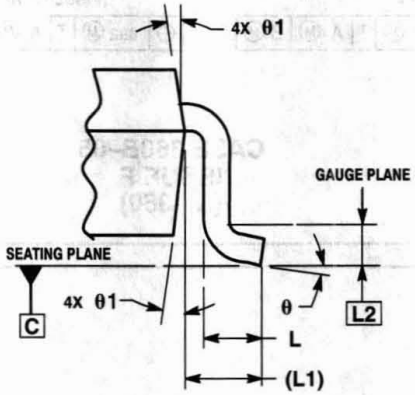
CASE 301AY–01
ISSUE O

CASE DIMENSIONS (continued)







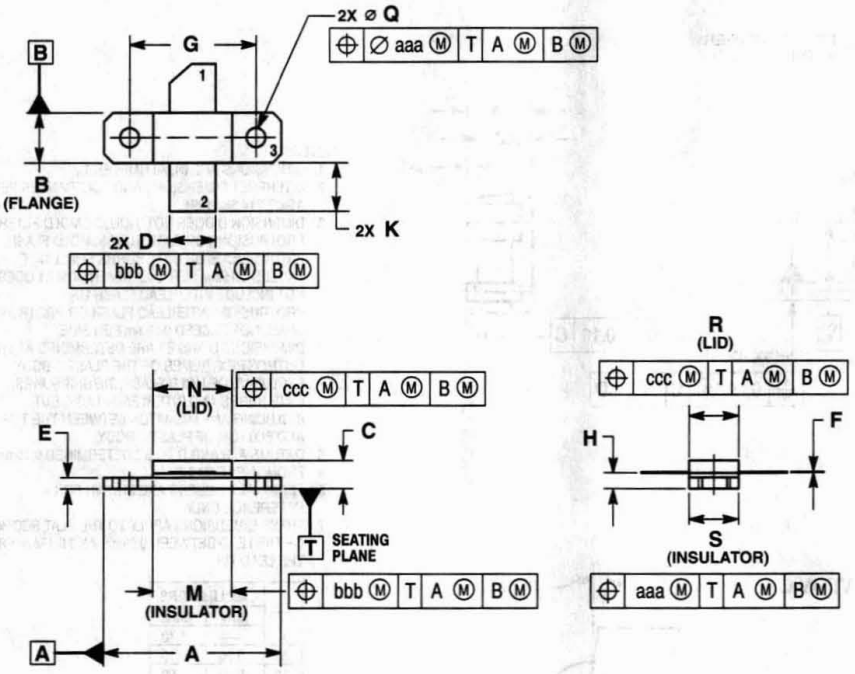


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm PER SIDE.
4. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF PLASTIC BODY.
5. DATUMS A, B AND D TO BE DETERMINED 0.10mm FROM THE LEAD TIP.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08mm AND 0.15mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.10
A1	0.00	0.10
A2	0.80	1.00
b	0.25	0.40
b1	0.25	0.35
B	0.55	0.70
B1	0.55	0.65
c	0.10	0.25
c1	0.08	0.20
D	2.00 BSC	
E	2.10 BSC	
E1	1.25 BSC	
e1	1.30 BSC	
e2	0.65 BSC	
e3	1.15 BSC	
e4	0.50 BSC	
L	0.26	0.46
L1	0.425 REF	
L2	0.15 BSC	
θ	0°	8°
θ1	4°	10°

CASE 318M–01
ISSUE O
(SOT–343)

CASE DIMENSIONS (continued)

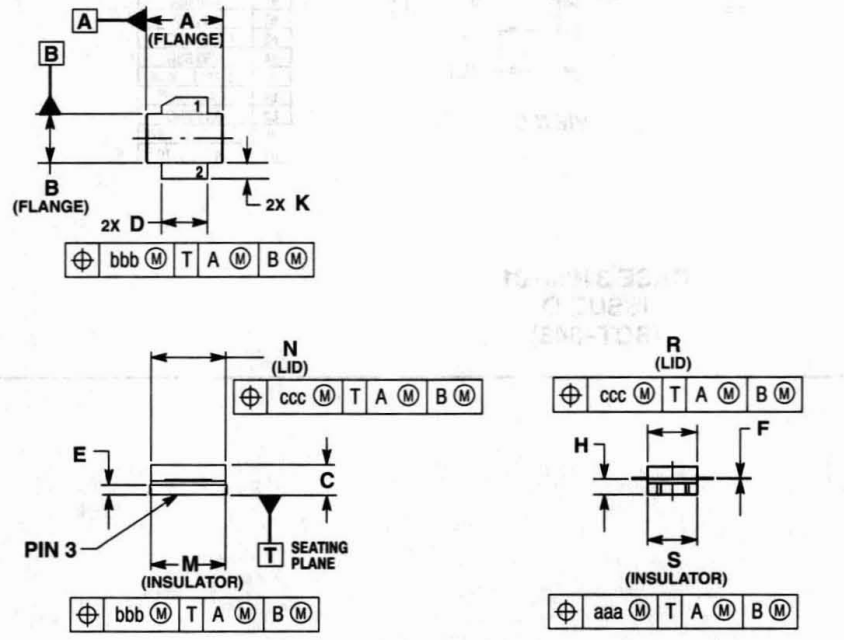


NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.795	0.805	20.19	20.45
B	0.225	0.235	5.72	5.97
C	0.125	0.175	3.18	4.45
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.10	0.15
G	0.562 BSC		14.28 BSC	
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
Q	0.125	0.135	3.18	3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 360B–05
ISSUE F
(NI–360)



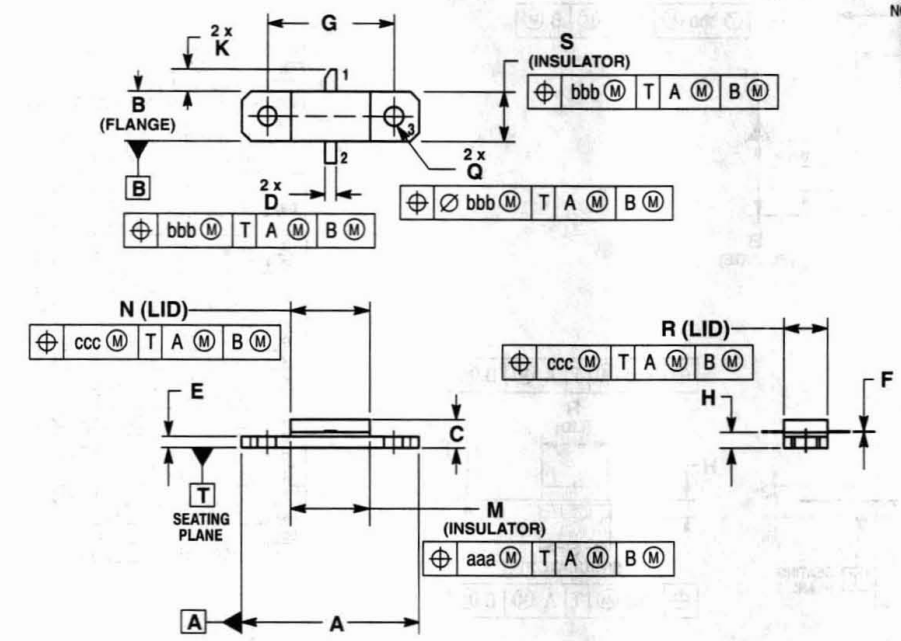
NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.375	0.385	9.53	9.78
B	0.225	0.235	5.72	5.97
C	0.105	0.155	2.67	3.94
D	0.210	0.220	5.33	5.59
E	0.035	0.045	0.89	1.14
F	0.004	0.006	0.10	0.15
H	0.057	0.067	1.45	1.70
K	0.085	0.115	2.16	2.92
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
R	0.227	0.23	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 360C–05
ISSUE D
(NI–360S)

CASE DIMENSIONS (continued)

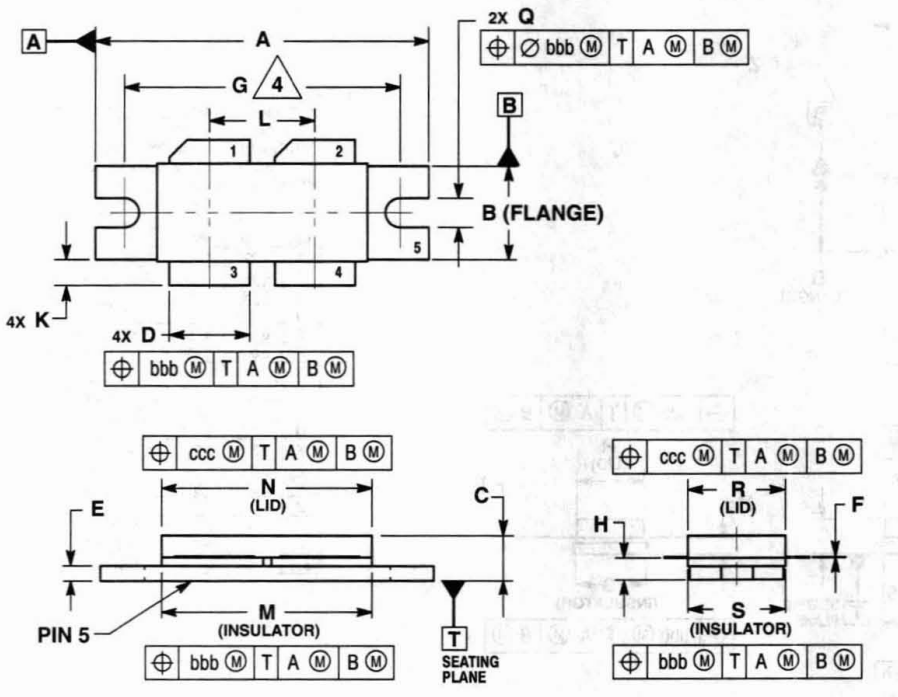


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.45
B	.225	.235	5.72	5.97
C	.125	.176	3.18	4.47
D	.034	.044	0.89	1.12
E	.055	.065	1.40	1.65
F	.004	.006	0.10	0.15
G	.562 BSC		14.28 BSC	
H	.077	.087	1.96	2.21
K	.085	.115	2.16	2.92
M	.355	.365	9.02	9.27
N	.355	.365	9.96	10.16
Q	.125	.135	3.18	3.43
R	.225	.235	5.72	5.97
S	.225	.235	5.72	5.97
aaa	.005		0.13	
bbb	.010		0.25	
ccc	.015		0.38	

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

CASE 360D–02
ISSUE B
(NI–360HF)

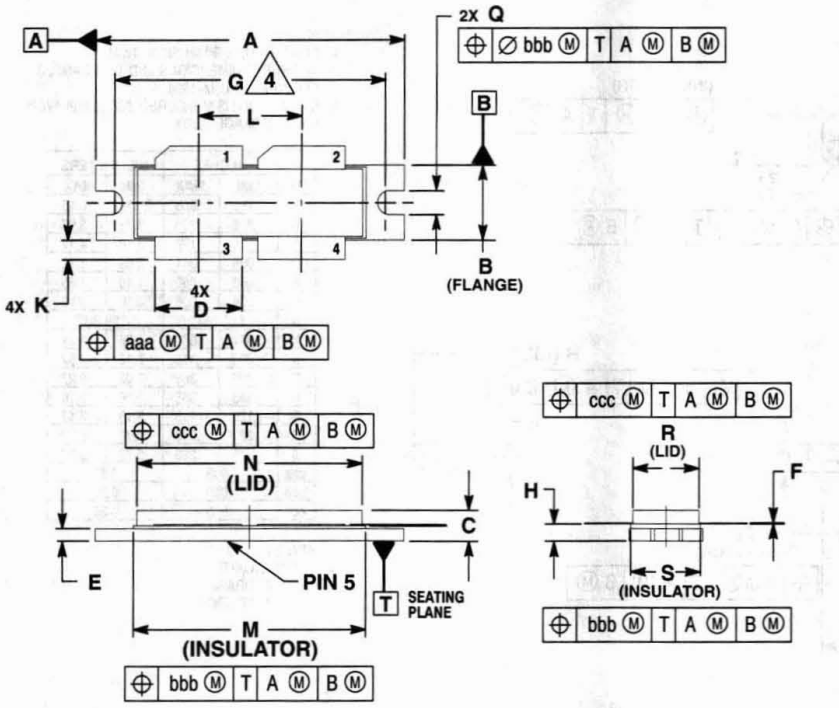


NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.140 (28.96) BASED ON M3 SCREW.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.180	0.224	4.57	5.69
D	0.325	0.335	8.26	8.51
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	1.100 BSC		27.94 BSC	
H	0.097	0.107	2.46	2.72
K	0.085	0.115	2.16	2.92
L	0.425 BSC		10.80 BSC	
M	0.852	0.868	21.64	22.05
N	0.851	0.869	21.62	22.07
Q	0.118	0.138	3.00	3.51
R	0.395	0.405	10.03	10.29
S	0.394	0.406	10.01	10.31
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375B–04
ISSUE E
(NI–860)

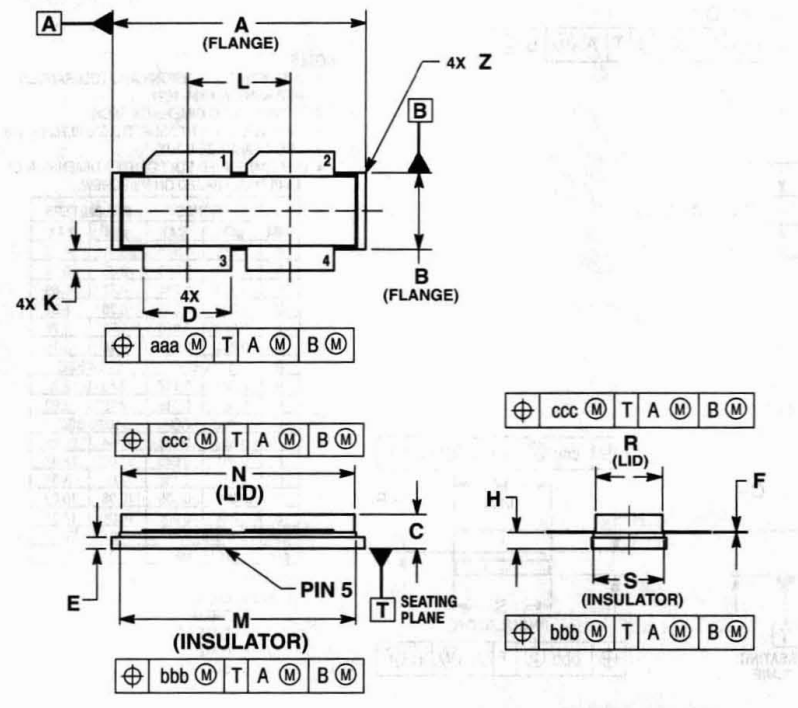


NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.28
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
G	1.400 BSC		35.56 BSC	
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
Q	0.120	0.130	3.05	3.30
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
aaa	0.013 REF		0.33 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.020 REF		0.51 REF	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375D–04
ISSUE C
(NI–1230)



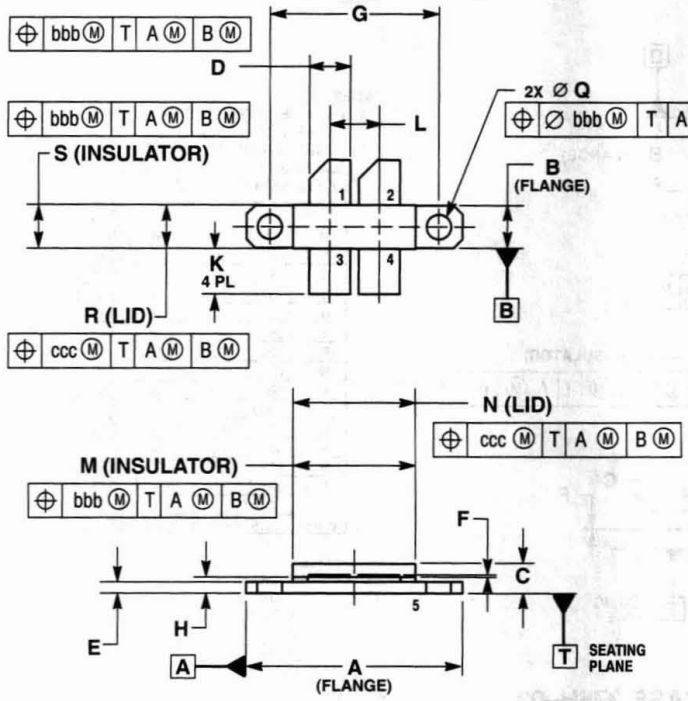
NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.325	1.335	33.66	33.91
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
Z	0	0.040	0	1.02
aaa	0.013 REF		0.33 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.020 REF		0.51 REF	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375E–03
ISSUE C
(NI–1230S)

CASE DIMENSIONS (continued)

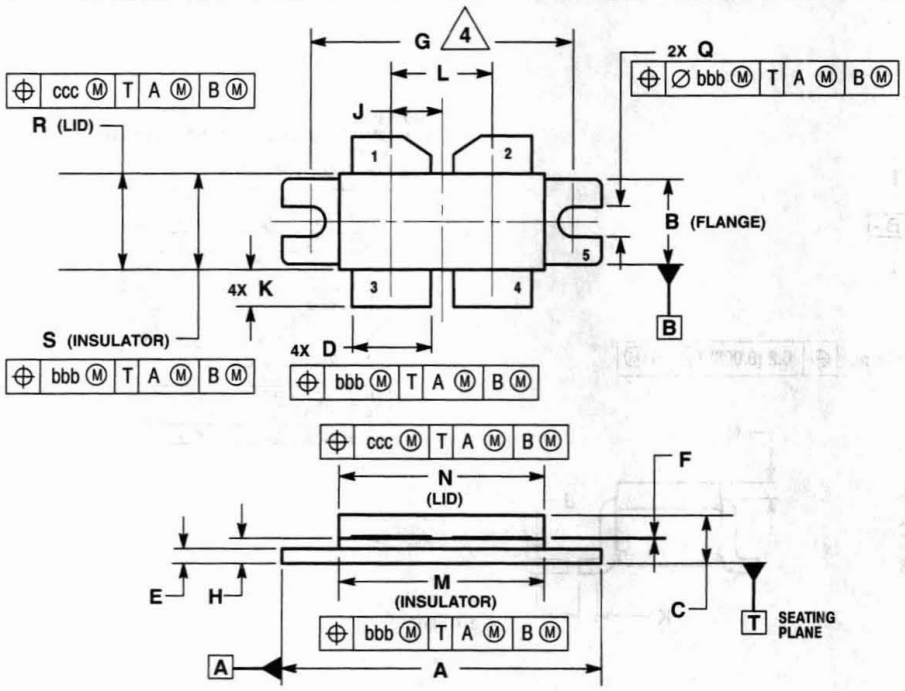


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.135	1.145	28.80	29.10
B	0.225	0.235	5.72	5.97
C	0.135	0.178	3.43	4.52
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.11	0.15
G	0.900 BSC		22.86 BSC	
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
L	0.260 BSC		6.60 BSC	
M	0.643	0.657	16.33	16.69
N	0.638	0.650	16.20	16.50
Q	Ø .125	Ø .135	Ø3.175	Ø 3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.715	5.97
bbb	0.010 BSC		0.254 BSC	
ccc	0.015 BSC		0.381 BSC	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375F–04
ISSUE D
(NI–650)



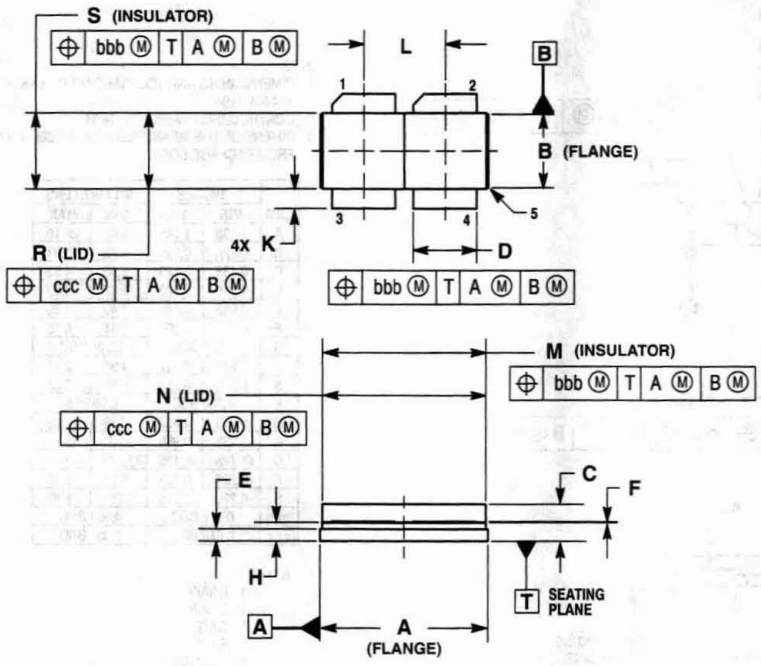
NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION H TO BE MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.140 (28.96) BASED ON 3M SCREW.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.180	0.224	4.57	5.69
D	0.325	0.335	8.26	8.51
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	1.100 BSC		27.94 BSC	
H	0.097	0.107	2.46	2.72
J	0.2125 BSC		5.397 BSC	
K	0.135	0.165	3.43	4.19
L	0.425 BSC		10.8 BSC	
M	0.852	0.868	21.64	22.05
N	0.851	0.869	21.62	22.07
Q	0.118	0.138	3.00	3.30
R	0.395	0.405	10.03	10.29
S	0.394	0.406	10.01	10.31
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375G–04
ISSUE E
(NI–860C3)

CASE DIMENSIONS (continued)

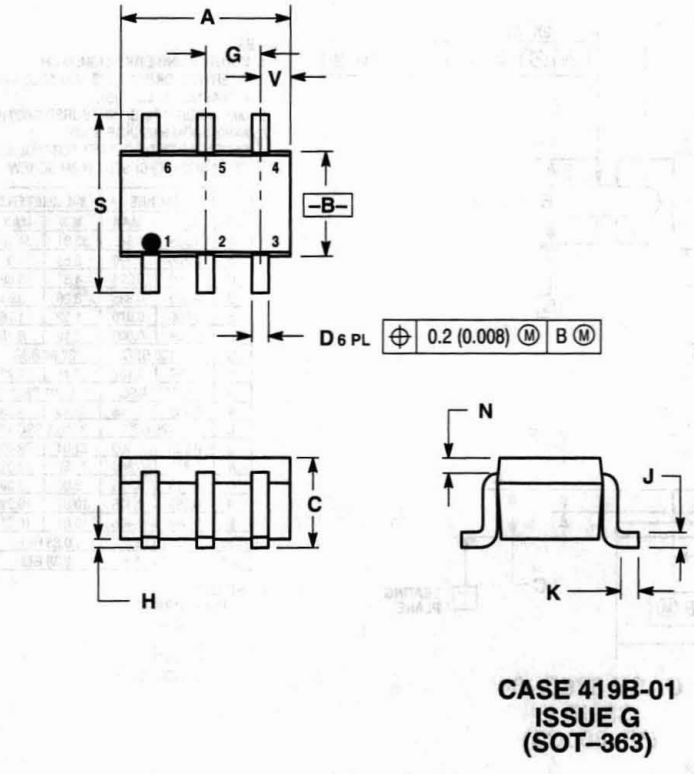


NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "H" TO BE MEASURED 0.030 (0.762) INCHES FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.885	.895	22.48	22.73
B	.380	.390	9.65	9.91
C	.180	.224	4.57	5.69
D	.325	.335	8.26	8.51
E	.060	.070	1.52	1.78
F	.004	.006	0.10	0.15
H	.097	.107	2.46	2.72
K	.085	.115	2.16	2.92
L	.425 BSC		10.8 BSC	
M	.852	.868	21.64	22.05
N	.851	.869	21.62	22.07
R	.395	.405	10.03	10.29
S	.394	.406	10.01	10.31
bbb	.010 REF		0.25 REF	
ccc	.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375H–03
ISSUE B
(NI–860S)

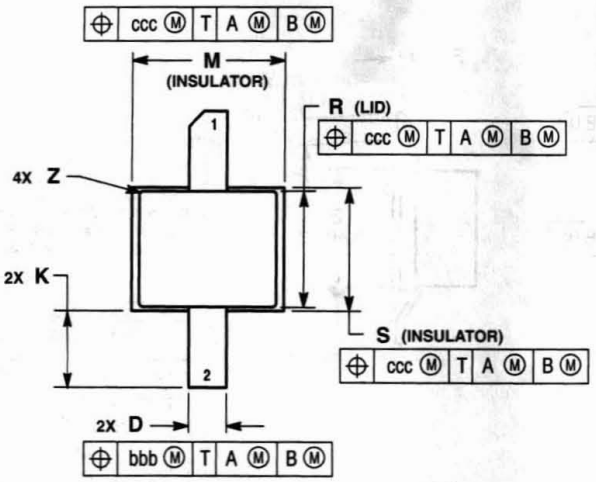


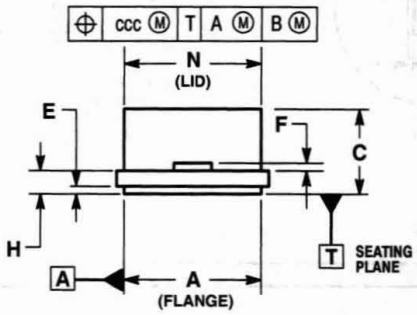
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

CASE 419B-01
ISSUE G
(SOT–363)

CASE DIMENSIONS (continued)





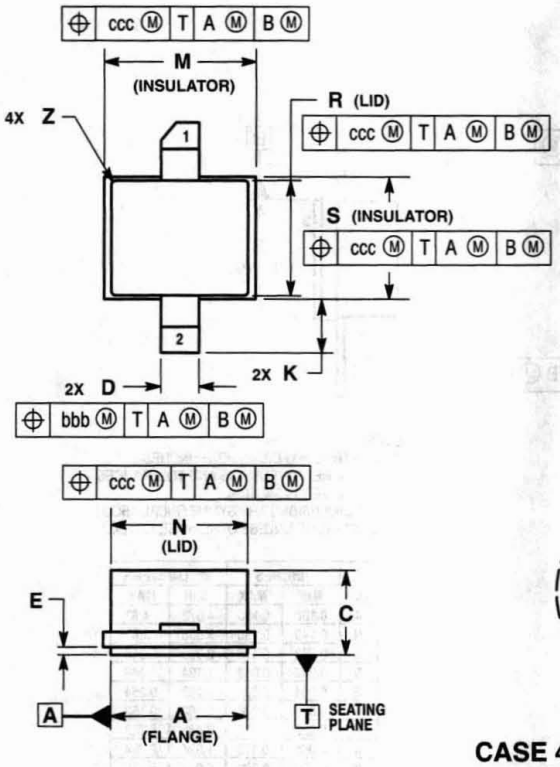
NOTES:
1. CONTROLLING DIMENSIONS: INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. ALL DIMENSIONS ARE SYMMETRICAL ABOUT CENTERLINE UNLESS OTHERWISE NOTED.

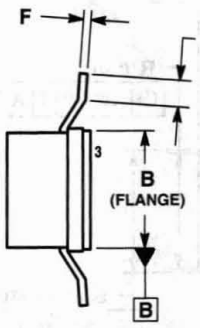
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.180	0.190	4.572	4.83
B	0.140	0.150	3.556	3.81
C	0.082	0.116	2.083	2.946
D	0.047	0.053	1.194	1.346
E	0.004	0.010	0.102	0.254
F	0.004	0.006	0.102	0.152
H	0.025	0.031	0.635	0.787
K	0.060	0.110	1.524	2.794
M	0.197	0.203	5.004	5.156
N	0.177	0.183	4.496	4.648
R	0.147	0.153	3.734	3.886
S	0.157	0.163	3.988	4.14
Z	---	0.020	---	0.508
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

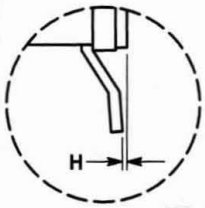
STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458B–03
ISSUE D
(NI–200S)

CASE DIMENSIONS (continued)





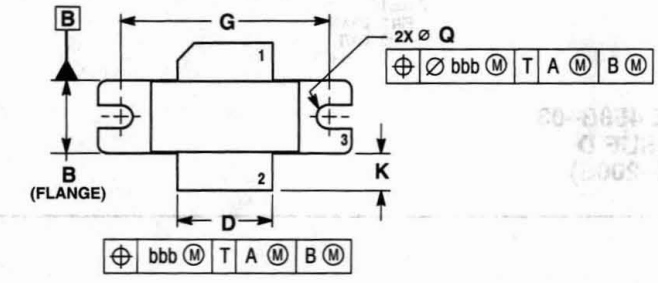


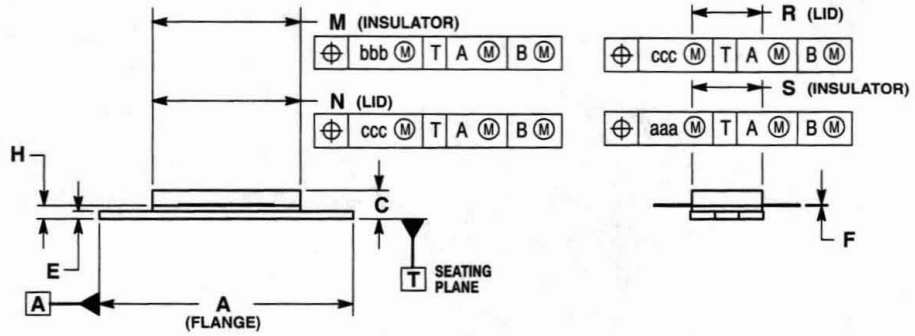
NOTES:
1. CONTROLLING DIMENSIONS: INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H (PACKAGE COPLANARITY): THE BOTTOM OF LEADS AND REFERENCE PLANE T MUST BE COPLANAR WITHIN DIMENSION H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.180	0.190	4.572	4.830
B	0.140	0.150	3.556	3.810
C	0.082	0.116	2.083	2.946
D	0.047	0.053	1.194	1.346
E	0.004	0.010	0.102	0.254
F	0.004	0.006	0.102	0.152
H	0.000	0.004	0.000	0.102
K	0.050	0.090	1.270	2.286
M	0.197	0.203	5.004	5.156
N	0.177	0.183	4.496	4.648
R	0.147	0.153	3.734	3.886
S	0.157	0.163	3.988	4.140
Y	0.020	0.040	0.508	1.016
Z	---	R .020	---	R .508
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458C–03
ISSUE D
(NI–200Z)





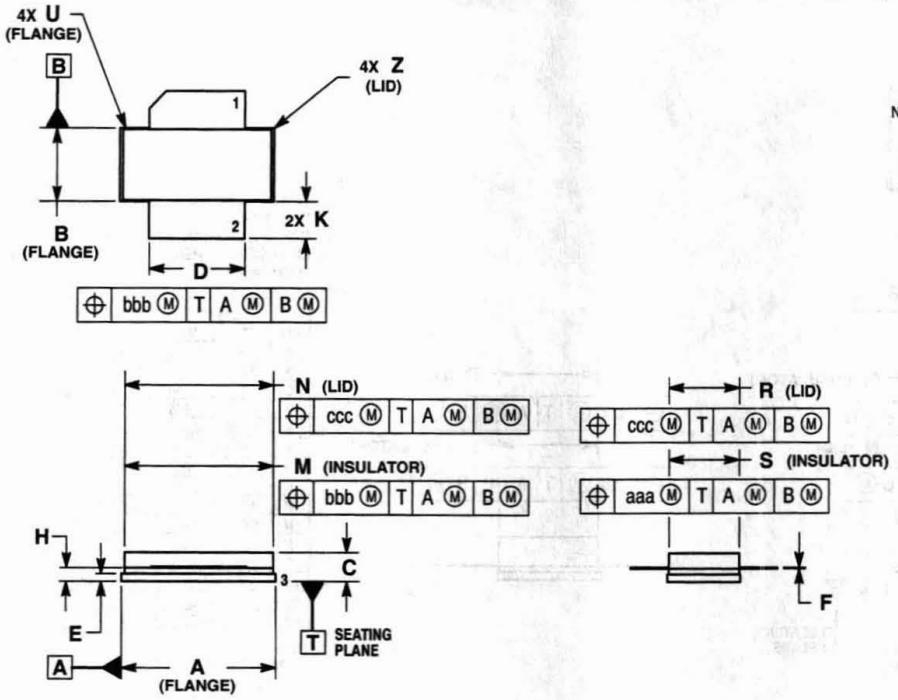
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	Ø.118	Ø.138	Ø3.00	Ø3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465–06
ISSUE F
(NI–780)

CASE DIMENSIONS (continued)

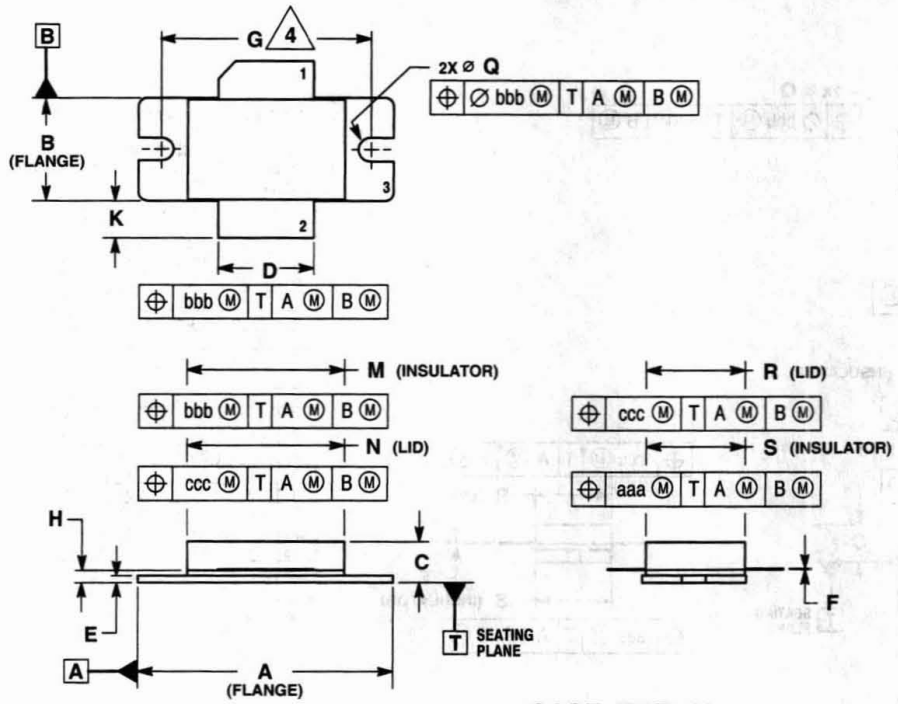


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

CASE 465A–06
ISSUE F
(NI–780S)

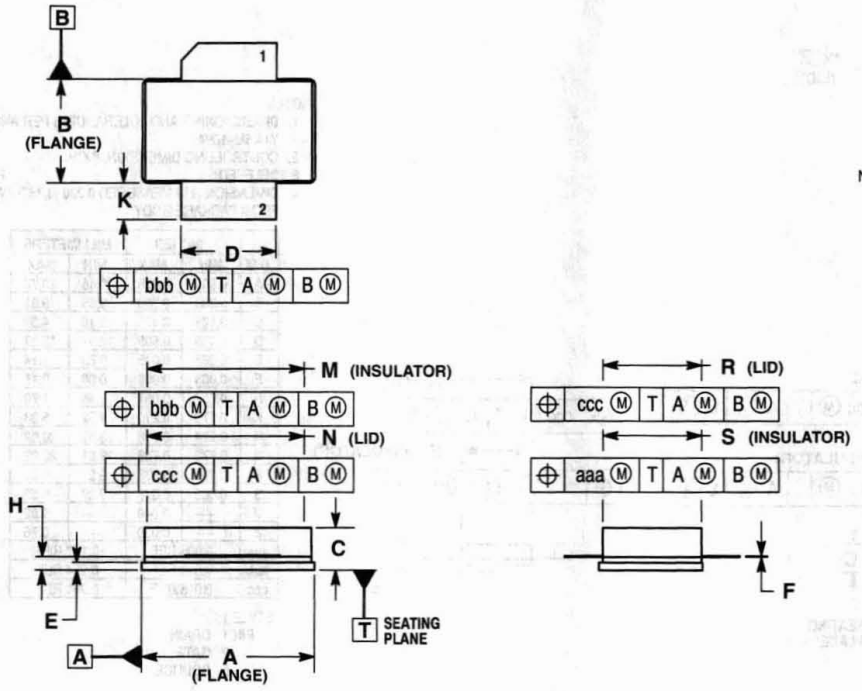


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.175	0.205	4.44	5.21
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	⌀.118	⌀.138	⌀3.00	⌀3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465B–03
ISSUE C
(NI–880)

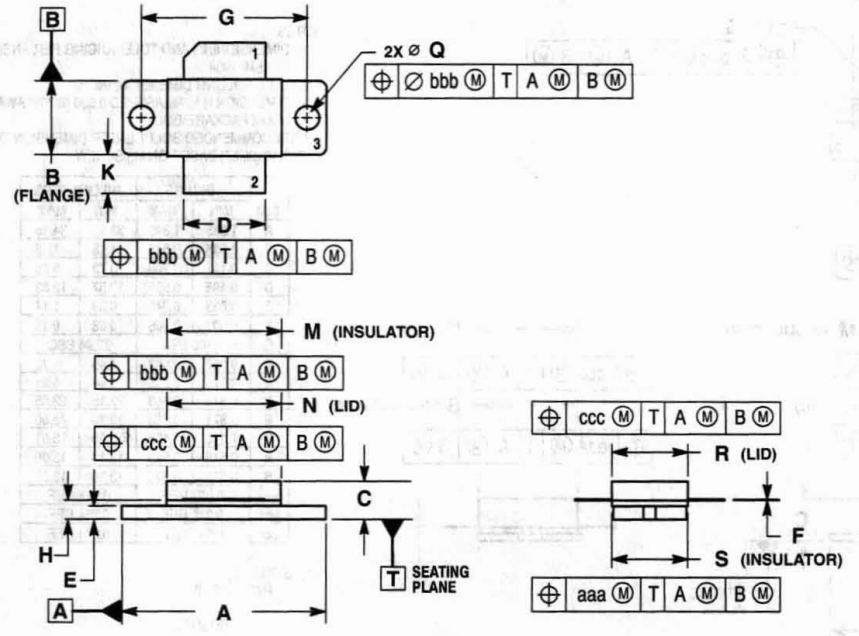


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465C–02
ISSUE A
(NI–880S)



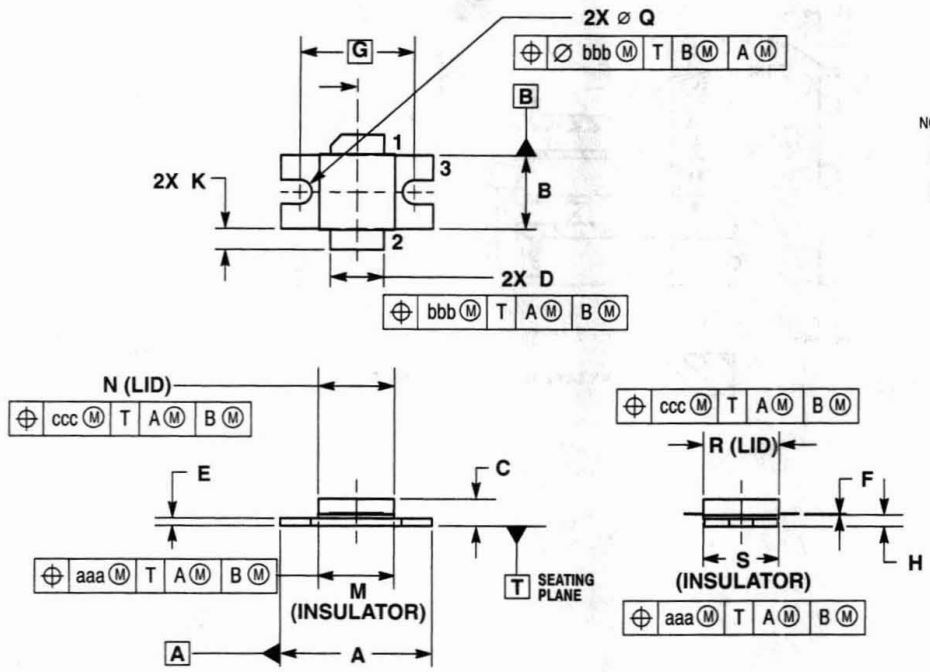
NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.065	1.075	27.05	27.30
B	0.380	0.390	9.65	9.91
C	0.160	0.205	4.06	5.21
D	0.425	0.435	10.80	11.05
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	0.870 BSC		22.10 BSC	
H	0.096	0.106	2.44	2.69
K	0.190	0.223	4.83	5.66
M	0.594	0.606	15.09	15.39
N	0.591	0.601	15.01	15.27
Q	0.124	0.130	3.15	3.30
R	0.394	0.404	10.01	10.26
S	0.395	0.405	10.03	10.29
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465D–05
ISSUE D
(NI–600)

CASE DIMENSIONS (continued)

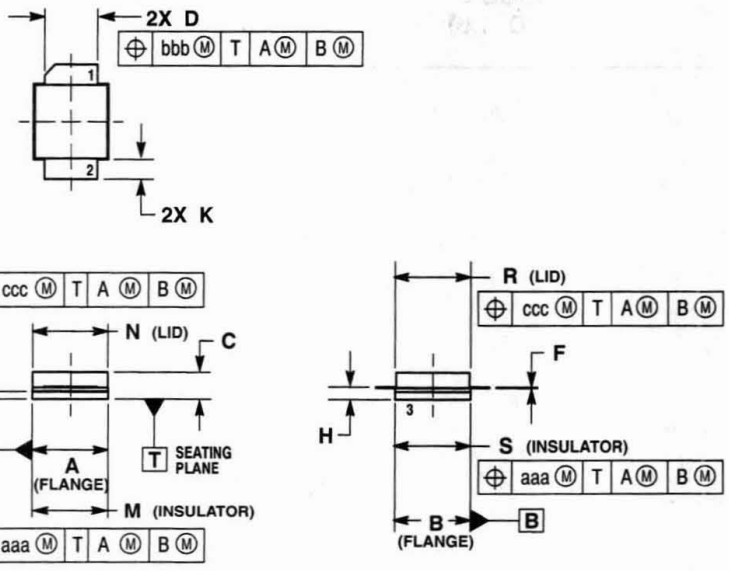


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.07	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	⌀ .110	⌀ .130	⌀ 2.79	⌀ 3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E–03
ISSUE D
(NI–400)



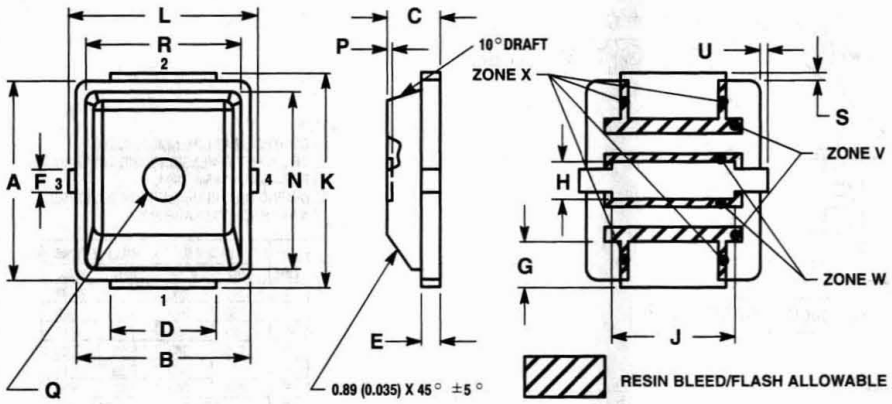
NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

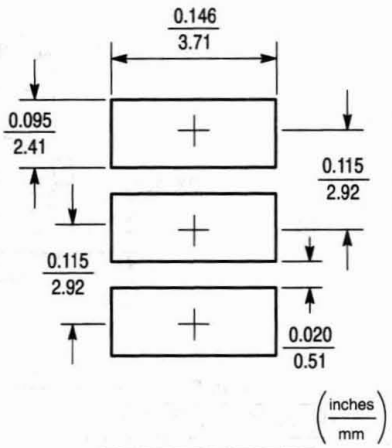
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.08	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005 REF		0.127 REF	
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465F–03
ISSUE B
(NI–400S)

CASE DIMENSIONS (continued)





SOLDER FOOTPRINT

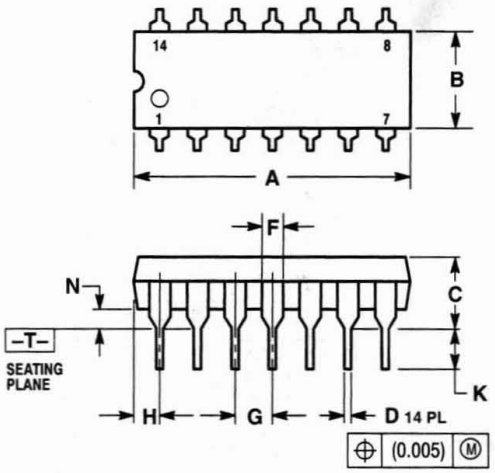
STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. SOURCE

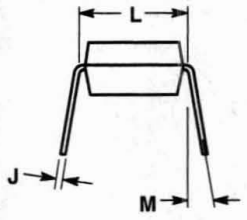
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. RESIN BLEED/FLASH ALLOWABLE IN ZONE V, W, AND X.

CASE 466–02
ISSUE B
(PLD–1.5)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.255	0.265	6.48	6.73
B	0.225	0.235	5.72	5.97
C	0.065	0.072	1.65	1.83
D	0.130	0.150	3.30	3.81
E	0.021	0.026	0.53	0.66
F	0.026	0.044	0.66	1.12
G	0.050	0.070	1.27	1.78
H	0.045	0.063	1.14	1.60
J	0.160	0.180	4.06	4.57
K	0.273	0.285	6.93	7.24
L	0.245	0.255	6.22	6.48
N	0.230	0.240	5.84	6.10
P	0.000	0.008	0.00	0.20
Q	0.055	0.063	1.40	1.60
R	0.200	0.210	5.08	5.33
S	0.006	0.012	0.15	0.31
U	0.006	0.012	0.15	0.31
ZONE V	0.000	0.021	0.00	0.53
ZONE W	0.000	0.010	0.00	0.25
ZONE X	0.000	0.010	0.00	0.25

CASE DIMENSIONS (continued)

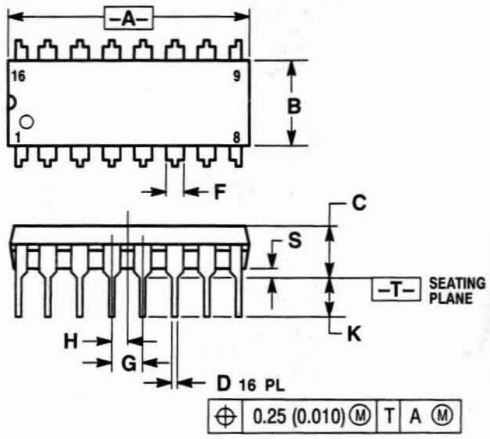


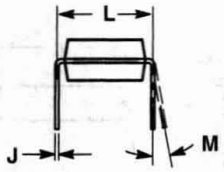


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 646-05 OBSOLETE, NEW STANDARD 646-06.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

CASE 646–06
ISSUE N
(DIP–14)

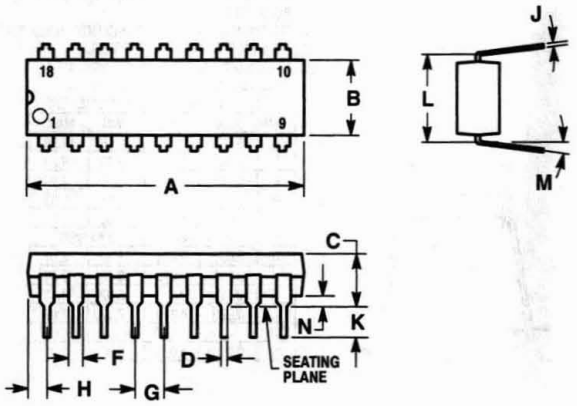




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

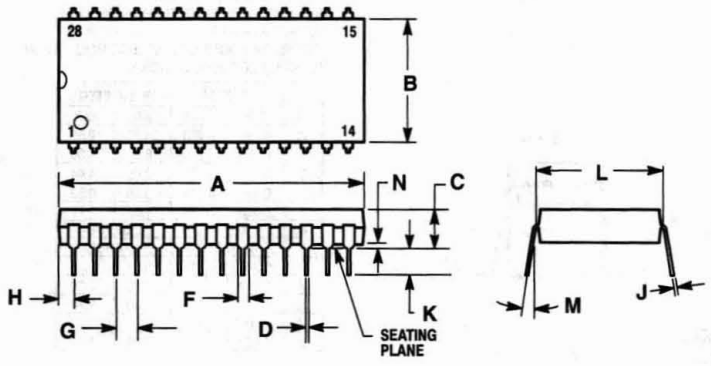
CASE 648–08
ISSUE R
(DIP–16)



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

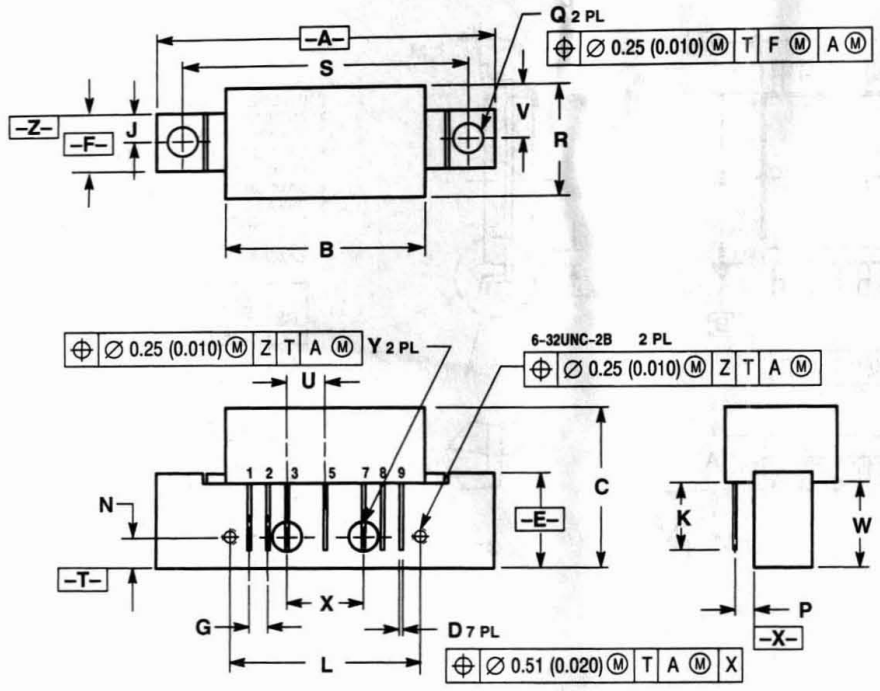
CASE 707–02
ISSUE C
(DIP–18)



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.085	1.65	2.16
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

CASE 710–02
ISSUE B
(DIP–28)



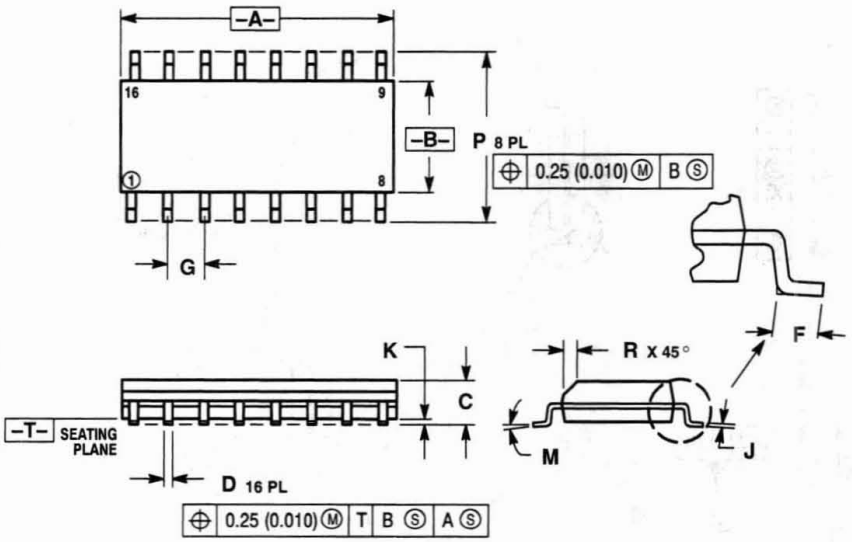
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-----	1.775	-----	45.08
B	-----	1.085	-----	27.56
C	-----	0.840	-----	21.34
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.315	0.355	8.00	8.50
L	1.00 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	-----	0.600	-----	15.24
S	1.500 BSC		38.10 BSC	
U	0.200 BSC		5.08 BSC	
V	----	0.250	----	6.35
W	0.435	0.450	11.05	11.43
X	0.400 BSC		10.16 BSC	
Y	0.152	0.163	3.85	4.15

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

STYLE 2:
PIN 1. RF OUTPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF INPUT

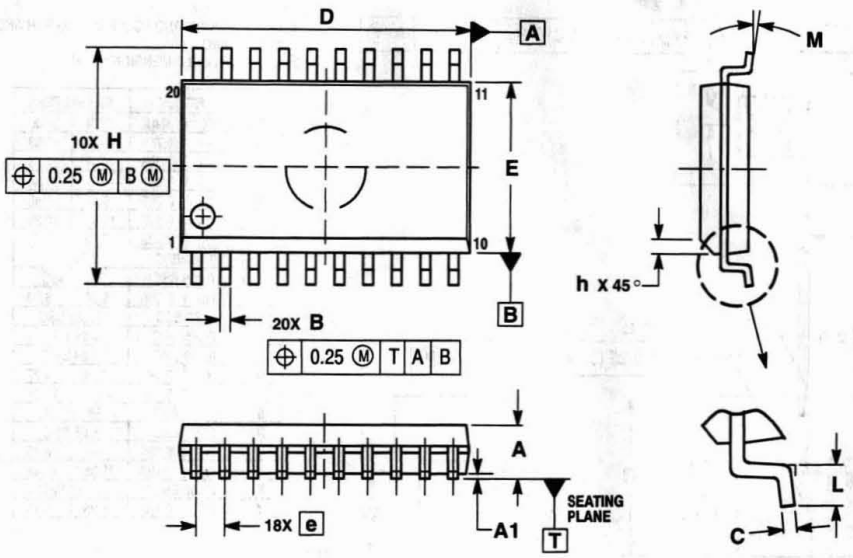
CASE 714Y–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

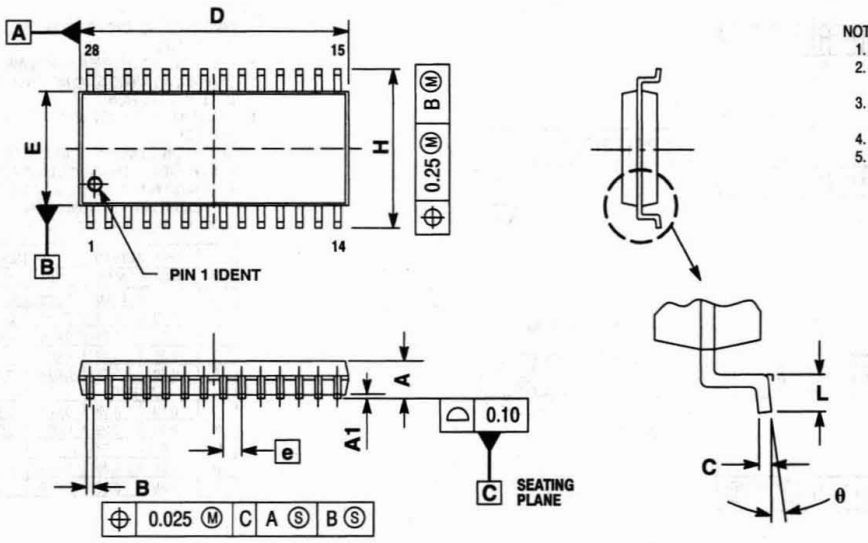
CASE 751B–05
ISSUE J
(SO–16)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.40	1.00
θ	0°	7°

CASE 751D–06
ISSUE G
(SO–20L)

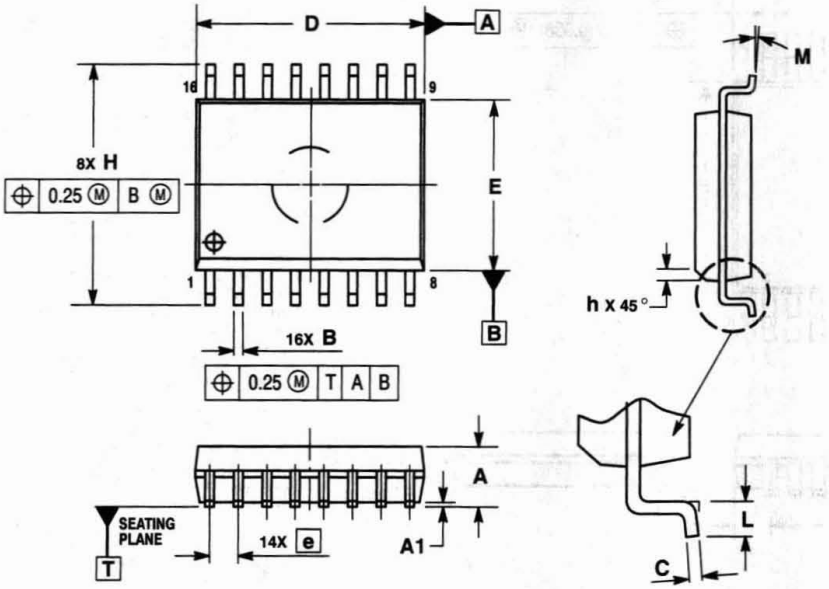


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

CASE 751F–05
ISSUE F
(SO–28L)

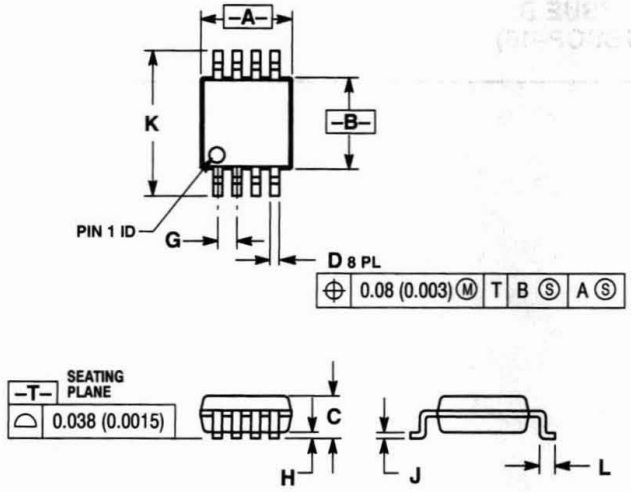
CASE DIMENSIONS (continued)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.40	1.00
M	0°	7°

CASE 751G–04
ISSUE C
(SO–16W)

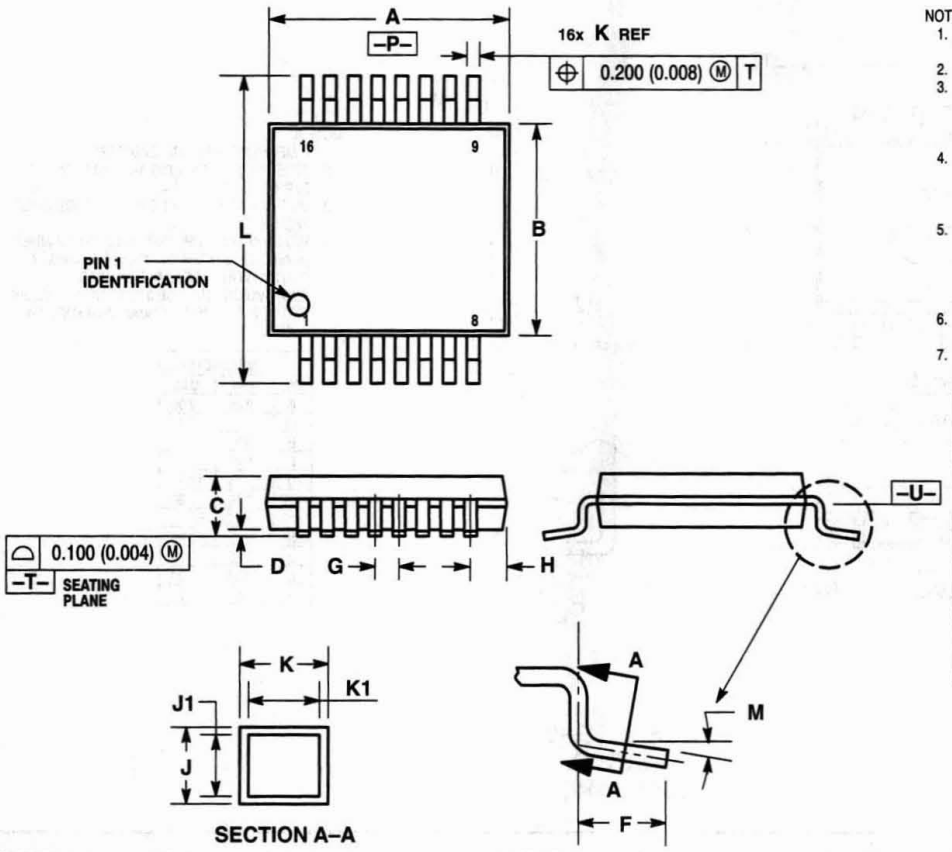


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

CASE 846A–02
ISSUE D
(Micro–8)

CASE DIMENSIONS (continued)

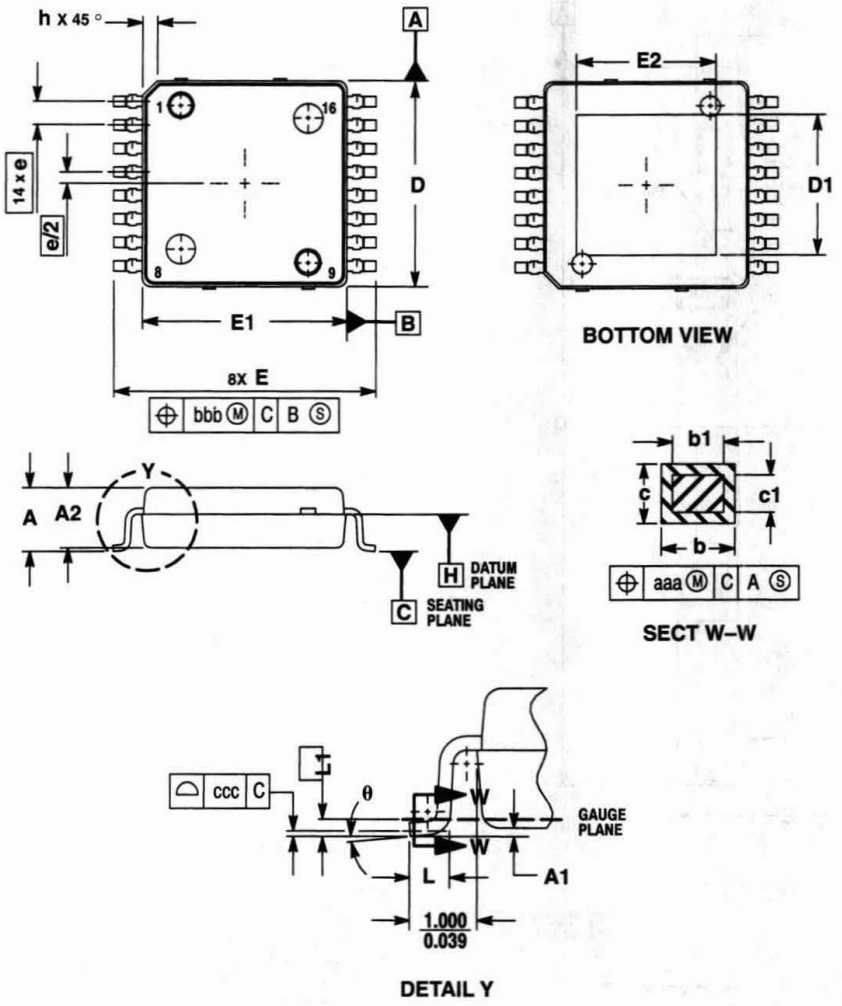


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	5.10	---	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

CASE 948C–03
ISSUE B
(TSSOP–16)

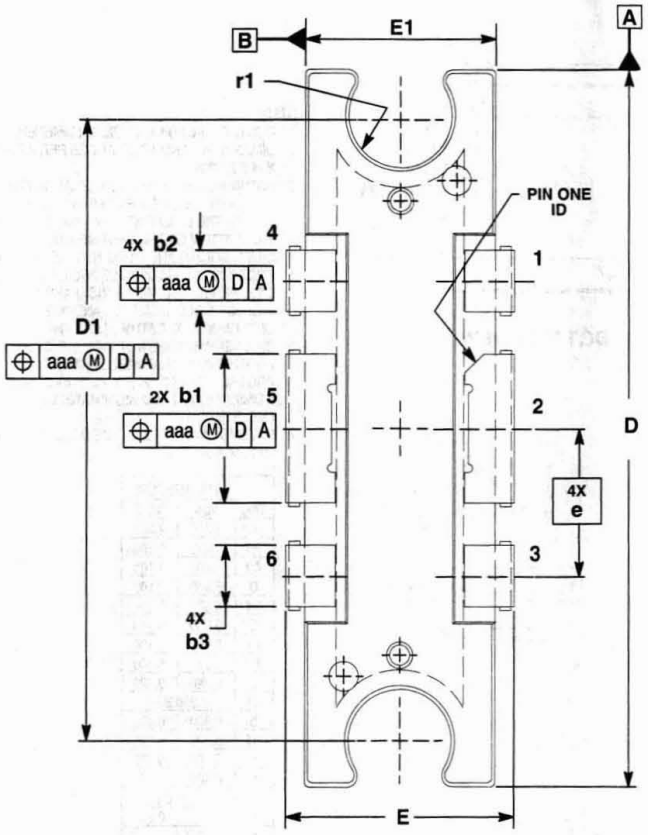
CASE DIMENSIONS (continued)

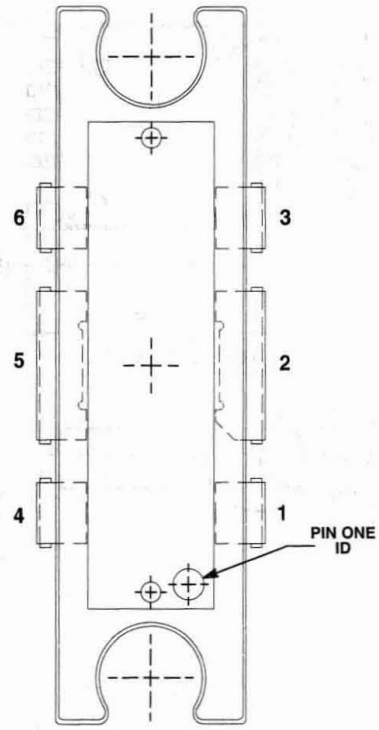


NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

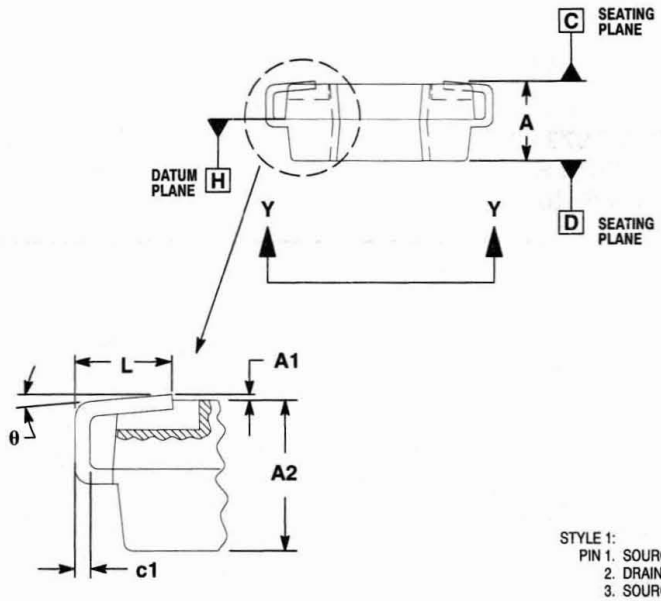
	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978–03
ISSUE B
(PFP–16)





VIEW Y–Y



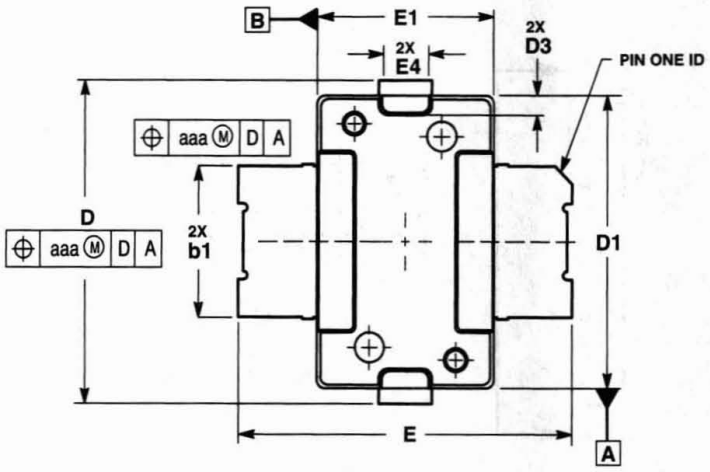
NOTES:
1. CONTROLLING DIMENSION: INCH .
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSION D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS b1 AND b3 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

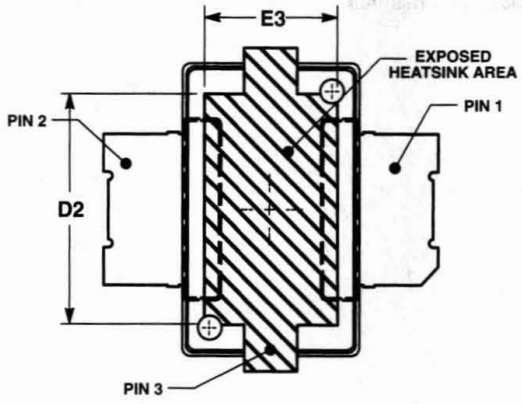
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.098	0.110	2.489	2.794
A1	0.000	0.004	0.000	0.102
A2	0.098	0.106	2.489	2.692
D	0.926	0.934	23.520	23.724
D1	0.806	0.814	20.472	20.676
E	0.296	0.304	7.518	7.722
E1	0.246	0.254	6.248	6.452
L	0.060	0.070	1.524	1.778
b1	0.193	0.199	4.902	5.055
b2	0.078	0.084	1.981	2.134
b3	0.088	0.094	2.235	2.388
c1	0.007	0.011	0.178	0.279
e	0.193 BSC		4.902 BSC	
r1	0.063	0.068	1.600	1.727
θ	0°	6°	0°	6°
aaa	0.004		0.102	

STYLE 1:
PIN 1. SOURCE (COMMON)
2. DRAIN
3. SOURCE (COMMON)
4. SOURCE (COMMON)
5. GATE
6. SOURCE (COMMON)

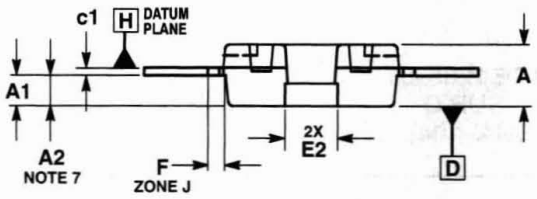
CASE 1264–07
ISSUE G
(TO–272)

CASE DIMENSIONS (continued)





BOTTOM VIEW



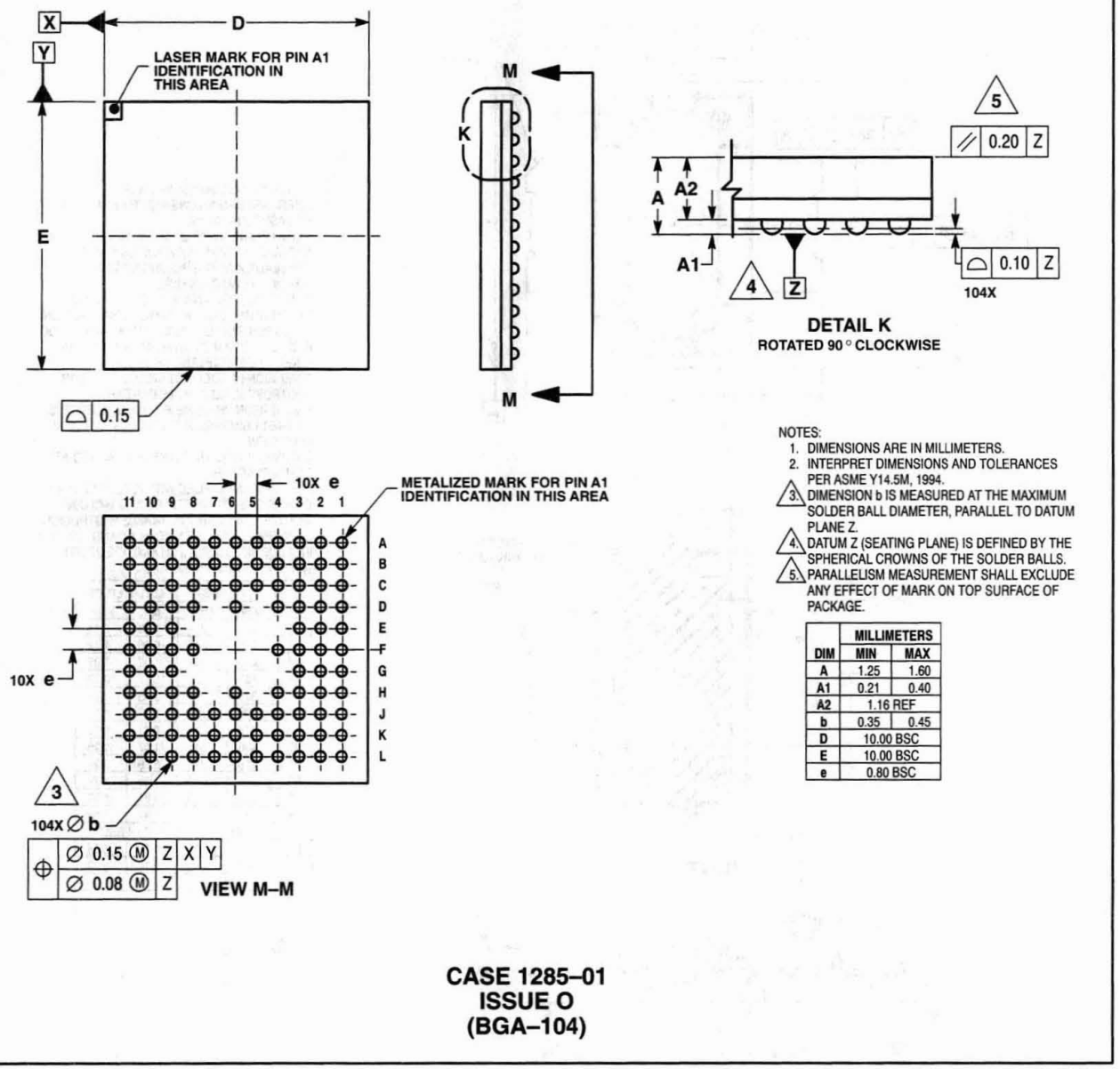
NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -D-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.076	.084	1.93	2.13
A1	.038	.044	0.96	1.12
A2	.040	.042	1.02	1.07
D	.416	.424	10.57	10.77
D1	.376	.384	9.55	9.75
D2	.290	.320	7.37	8.13
D3	.016	.024	0.41	0.61
E	.436	.444	11.07	11.28
E1	.236	.244	5.99	6.20
E2	.066	.074	1.68	1.88
E3	.150	.180	3.81	4.57
E4	.058	.066	1.47	1.68
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.06
c1	.007	.011	0.18	0.28
aaa	.004		0.10	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 1265-07
ISSUE F
(TO-270)

CASE DIMENSIONS (continued)

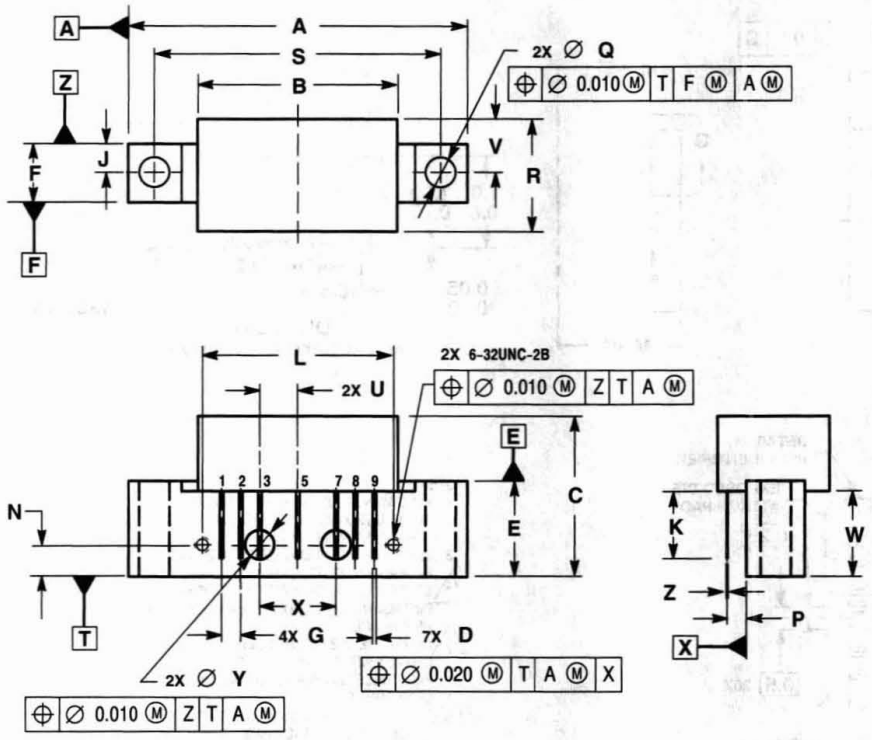


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.60
A1	0.21	0.40
A2	1.16 REF	
b	0.35	0.45
D	10.00 BSC	
E	10.00 BSC	
e	0.80 BSC	

CASE 1285–01
ISSUE O
(BGA–104)

CASE DIMENSIONS (continued)



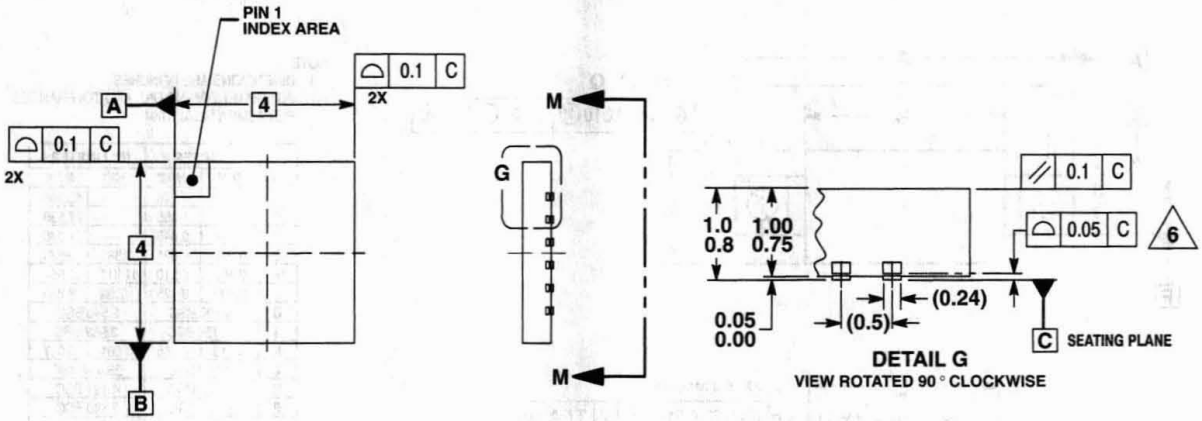
NOTES:
1. DIMENSIONS ARE IN INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	---	1.775	---	45.085
B	---	1.085	---	27.559
C	---	0.840	---	21.336
D	0.015	0.021	0.381	0.533
E	0.465	0.510	11.811	12.954
F	0.300	0.325	7.62	8.255
G	0.100 BSC		2.540 BSC	
J	0.156 BSC		3.962 BSC	
K	0.315	0.355	8.001	9.017
L	1.000 BSC		25.400 BSC	
N	0.165 BSC		4.191 BSC	
P	0.100 BSC		2.540 BSC	
Q	0.148	0.168	3.759	4.267
R	---	0.600	---	15.24
S	1.500 BSC		38.100 BSC	
U	0.200 BSC		5.080 BSC	
V	---	0.250	---	6.350
W	0.435	---	11.049	---
X	0.400 BSC		10.160 BSC	
Y	0.152	0.163	3.861	4.140
Z	0.009	0.011	0.229	0.279

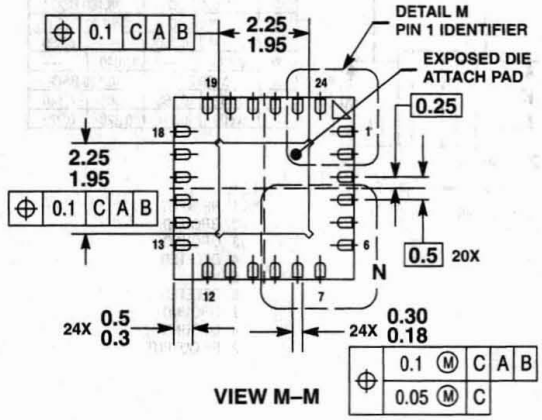
STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 1302–01
ISSUE B

CASE DIMENSIONS (continued)

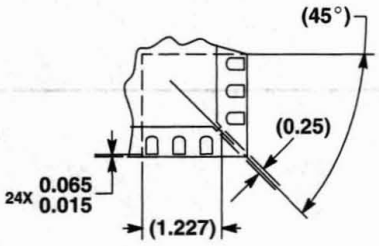


DETAIL G
VIEW ROTATED 90 ° CLOCKWISE

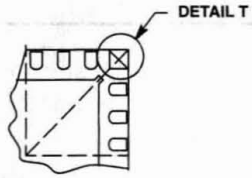


VIEW M–M

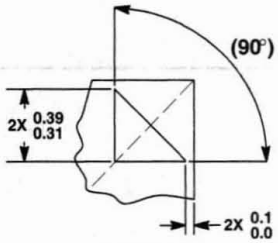
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
5. CORNER LEADS CAN BE USED FOR THERMAL OR GROUND AND ARE TIED TO THE DIE ATTACH PAD. THESE LEADS ARE NOT INCLUDED IN THE LEAD COUNT.
6. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
7. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12°.



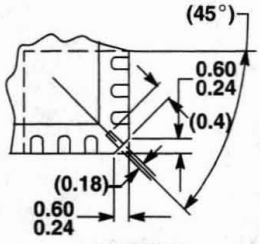
DETAIL N
PREFERRED CORNER CONFIGURATION
4



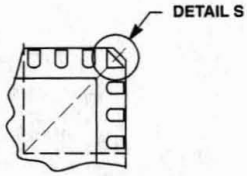
DETAIL M
PREFERRED PIN 1 BACKSIDE IDENTIFIER



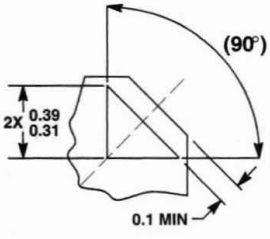
DETAIL T
PREFERRED PIN 1 BACKSIDE IDENTIFIER



DETAIL N
CORNER CONFIGURATION OPTION
4 5



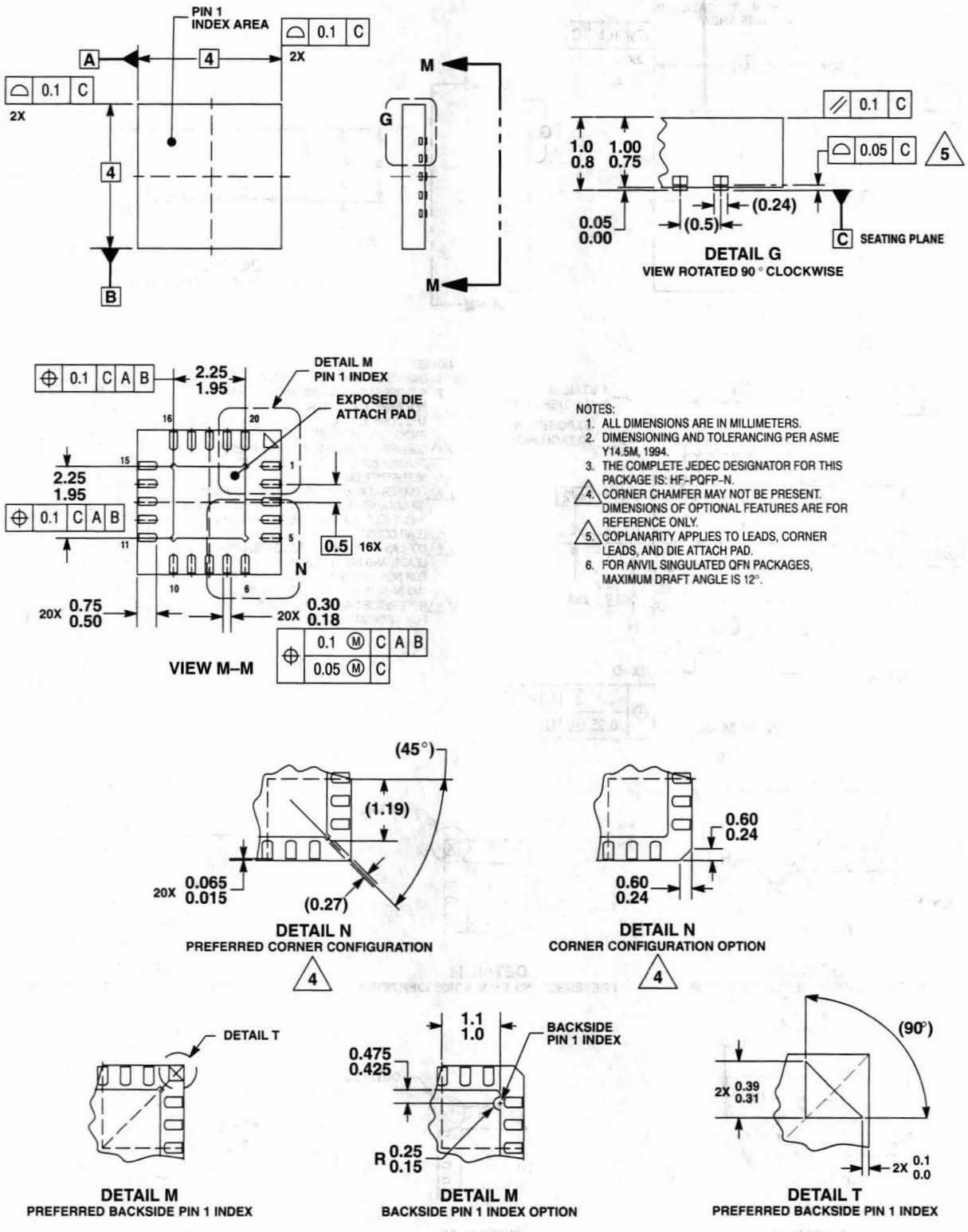
DETAIL M
PIN 1 BACKSIDE IDENTIFIER OPTION



DETAIL S
PIN 1 BACKSIDE IDENTIFIER OPTION

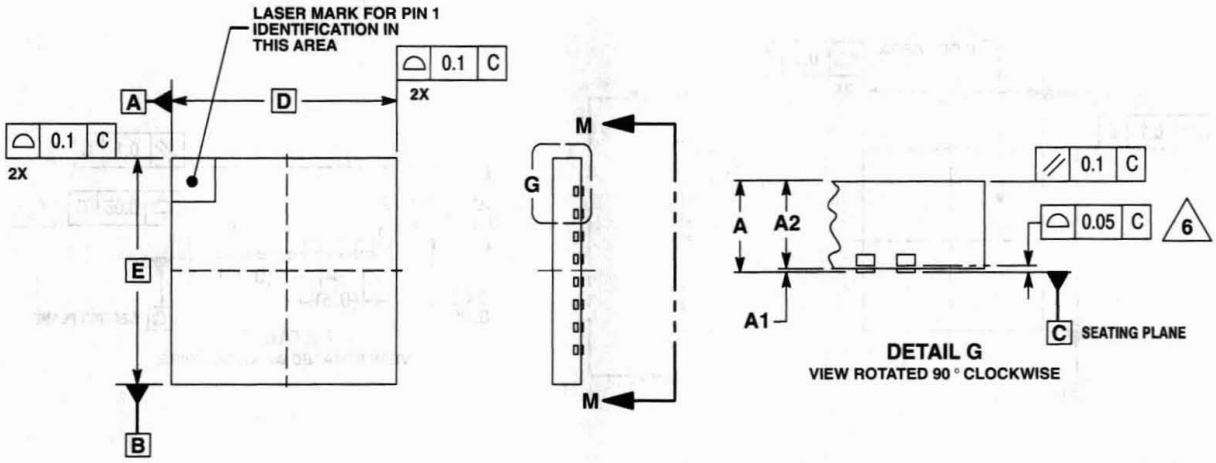
CASE 1307–01
ISSUE B
(QFN–24)

CASE DIMENSIONS (continued)

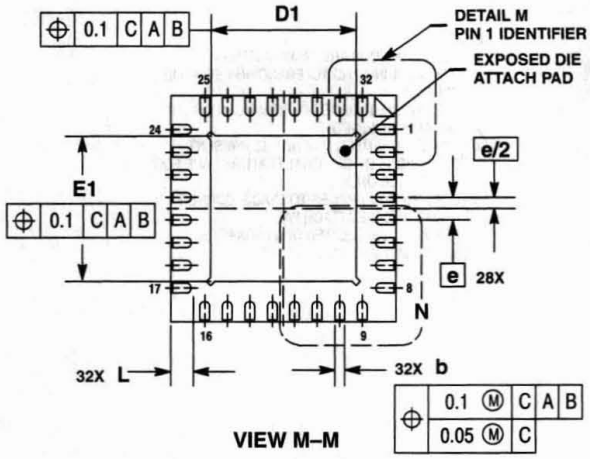


CASE 1308–02
ISSUE C
(QFN–20)

CASE DIMENSIONS (continued)



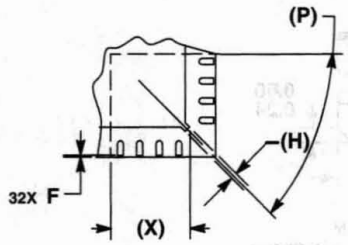
DETAIL G
VIEW ROTATED 90 ° CLOCKWISE



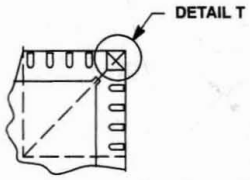
VIEW M–M

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
5. CORNER LEADS CAN BE USED FOR THERMAL OR GROUND AND ARE TIED TO THE DIE ATTACH PAD. THESE LEADS ARE NOT INCLUDED IN THE LEAD COUNT.
6. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
7. FOR NON-MAP STYLE QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12/M+2A258.
8. REFERENCE DIMENSIONS: H, P, R, X, AND Y ARE FOR INFORMATION ONLY.

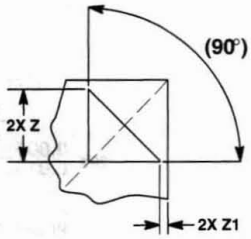
	MILLIMETERS	
DIM	MIN	MAX
A	0.8	1
A1	0	0.05
A2	0.75	1
b	0.18	0.3
D	5 BSC	
D1	2.95	3.25
E	5 BSC	
E1	2.95	3.25
e	0.5 BSC	
F	0.015	0.065
H	0.25	
L	0.3	0.5
P	(45°)	
R	0.18	
W	0.24	0.6
X	1.73	
Y	0.4	
Z	0.31	0.39
Z1	0	0.1
Z2	0.1	---
θ	SEE NOTE 7	



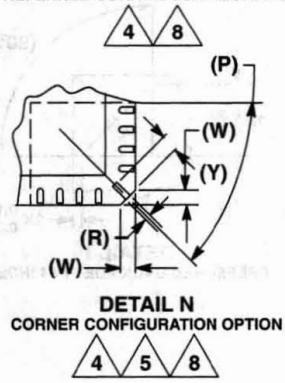
DETAIL N
PREFERRED CORNER CONFIGURATION



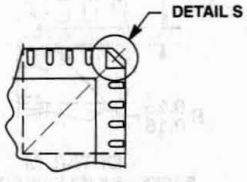
DETAIL M
PREFERRED PIN 1 BACKSIDE IDENTIFIER



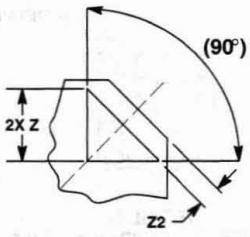
DETAIL T
PREFERRED PIN 1 BACKSIDE IDENTIFIER



DETAIL N
CORNER CONFIGURATION OPTION
4 5 8



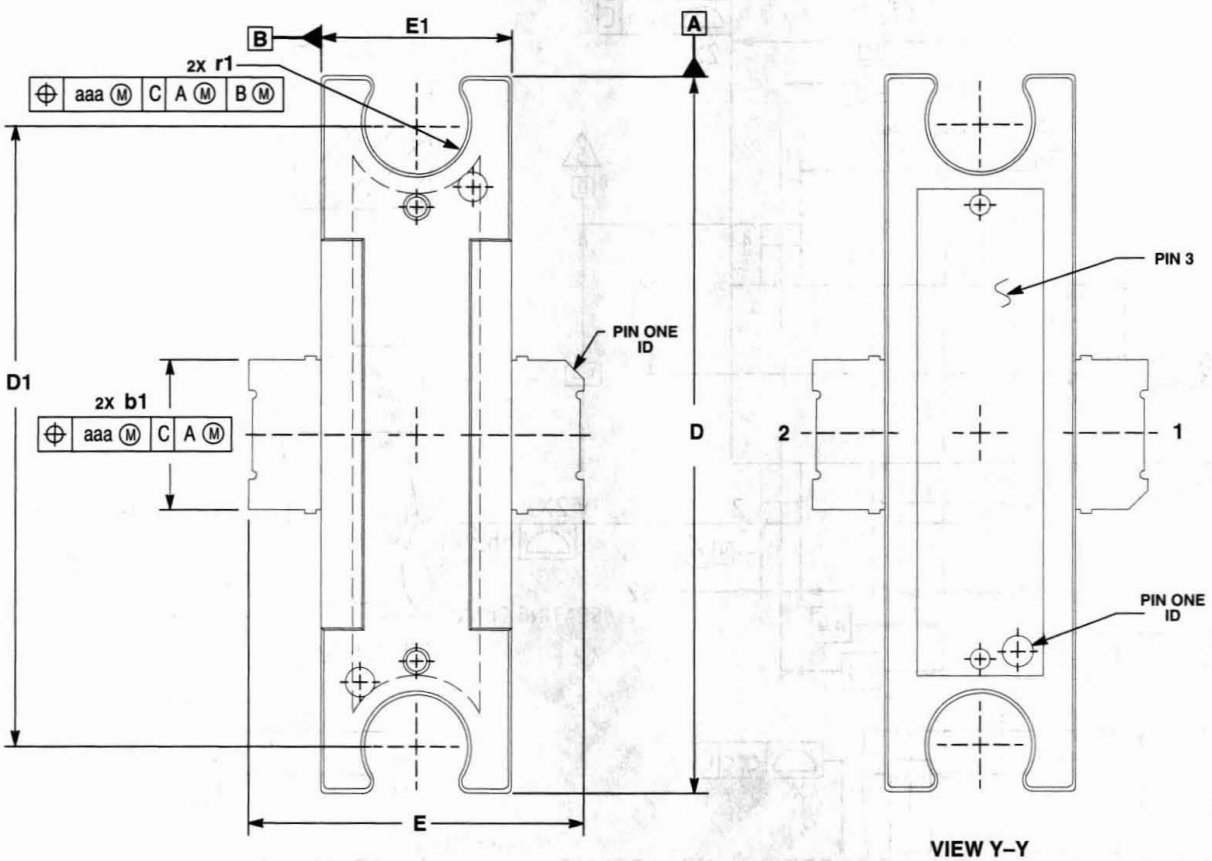
DETAIL M
PIN 1 BACKSIDE IDENTIFIER OPTION



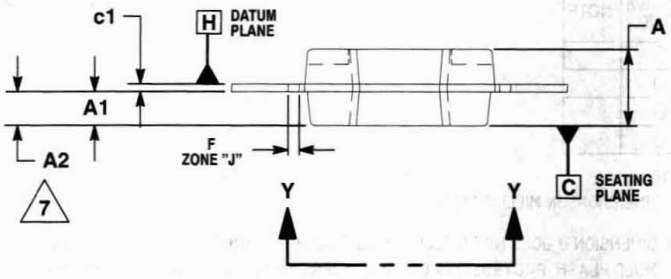
DETAIL S
PIN 1 BACKSIDE IDENTIFIER OPTION

CASE 1311–02
ISSUE B
(QFN–32, 5x5 mm)

CASE DIMENSIONS (continued)



VIEW Y–Y

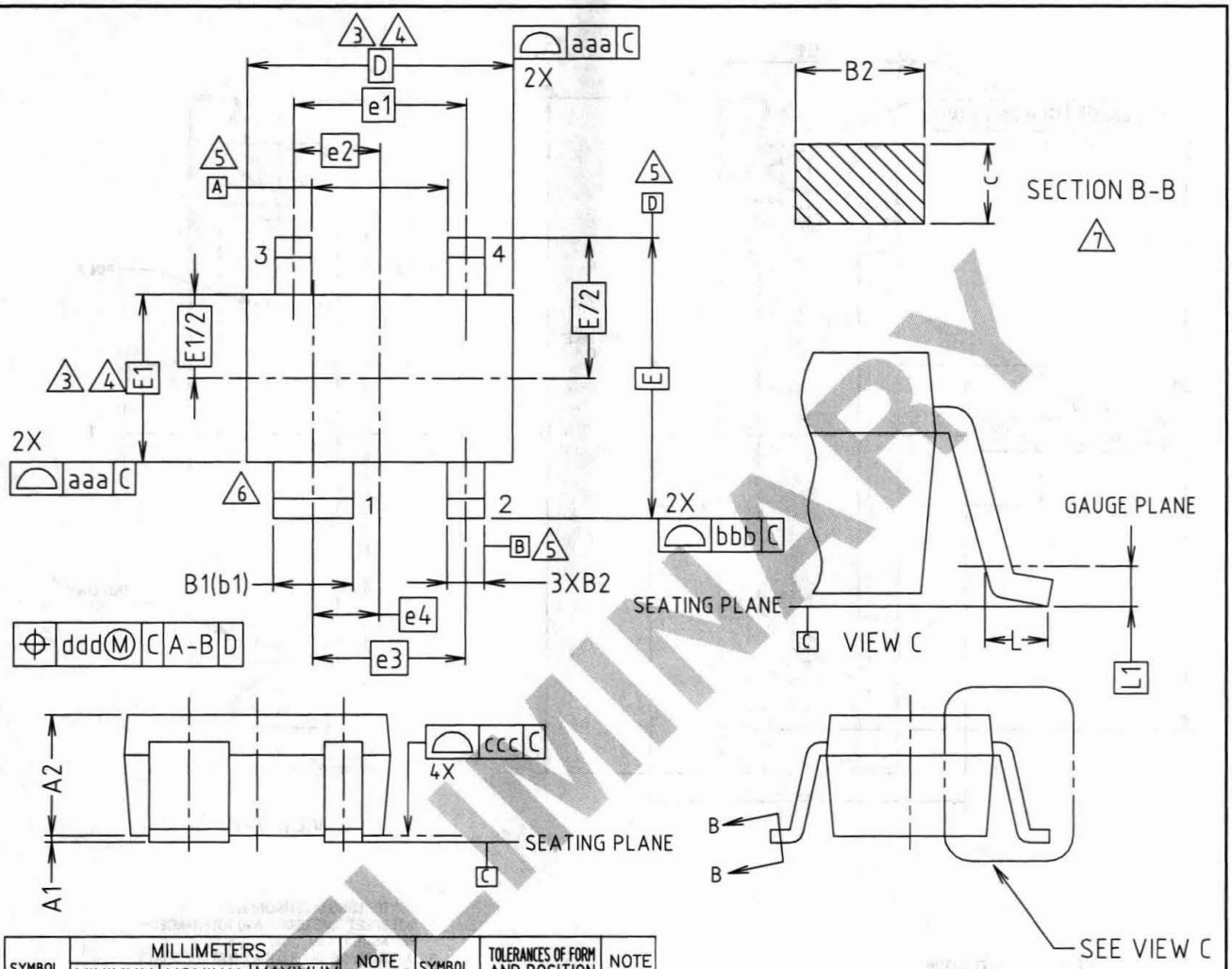


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.098	.110	2.49	2.79
A1	.038	.044	0.96	1.12
A2	.040	.042	1.02	1.07
D	.926	.934	23.52	23.72
D1	.810 BSC		20.57 BSC	
E	.438	.442	11.12	11.23
E1	.246	.254	6.25	6.45
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.05
c1	.007	.011	.18	.28
r1	.063	.068	1.60	1.73
aaa	.004		.10	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 1337–01
ISSUE O
(TO–272 Dual Lead)



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A1	0.00	–	0.10	
A2	0.80	0.90	1.00	
B1	0.55	–	0.70	
B2	0.25	–	0.40	
c	0.10	–	0.25	
D	2.00 BSC			3,4
E	2.10 BSC			
E1	1.25 BSC			3,4
e1	1.30 BSC			
e2	0.65 BSC			
e3	1.15 BSC			
e4	0.50 BSC			
L	0.25	–	–	
L1	0.15 BSC			

SYMBOL	TOLERANCES OF FORM AND POSITION	NOTE
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.10	

NOTE:

1. DIMENSIONS IN MILLIMETERS.

3 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm PER SIDE.

4 DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

5 DATUMS A, B AND D TO BE DETERMINED 0.10mm FROM THE LEAD TIP.

6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08mm AND 0.15mm FROM THE LEAD TIP.

Plastic Package
SOT–343R
(Preliminary)

PRELIMINARY

Chapter Ten
Applications and Product Literature

Motorola's Applications Literature provides guidance to the effective use of its semiconductor families across a broad range of practical applications. Many different topics are discussed in a way that is not possible in a device data sheet, from detailed circuit designs complete with PCB layouts, through matters to consider when embarking on a design, to complete overviews of product families and their design philosophies.

Information is presented in the form of Application Notes, Article Reprints and Engineering Bulletins.

Table of Contents

	Page
Applications Literature	10.1–2
Product Literature	10.1–2

Literature

Application Notes, Engineering Bulletins and Article Reprints of special interest to designers of RF and RF/IF equipment are listed below. This technical documentation is available on the Motorola Semiconductor Product Sector Web site or is available through the Motorola Literature Distribution Center. Phone and fax numbers for ordering literature are listed on the back cover of this book and in our Accessing Data On–line section.

Application Notes

AN211A Field Effect Transistors in Theory and Practice
AN419 UHF Amplifier Design Using Data Sheet Design Curves
AN423 Field Effect Transistor RF Amplifier Design Techniques
AN535 Phase–Locked–Loop Design Fundamentals
AN548A Microstrip Design Techniques for UHF Amplifiers
AN721 Impedance Matching Networks Applied to RF Power Transistors
AN923 800 MHz Test Fixture Design
AN955 A Cost Effective VHF Amplifier for Land Mobile Radios
AN1022 Mechanical and Thermal Considerations in Using RF Linear Hybrid Amplifiers
AN1024 RF Linear Hybrid Amplifiers
AN1025 Reliability Considerations in Design and Use of RF Integrated Circuits
AN1026 Extending the Range of an Intermodulation Distortion Test
AN1027 Reliability/Performance Aspects of CATV Amplifier Design
AN1032 How Load VSWR Affects Non–Linear Circuits
AN1033 Match Impedances in Microwave Amplifiers
AN1034 Three Balun Designs for Push–Pull Amplifiers
AN1040 Mounting Considerations for Power Semiconductors
AN1207 The MC145170 in Basic HF and VHF Oscillators
AN1253 An Improved PLL Design Method Without ϖn and ζ
AN1277 Offset Reference PLLs for Fine Resolution or Fast Hopping
AN1526 RF Power Device Impedances: Practical Considerations
AN1530 Motorola Advanced Amplifier Concept Package
AN1539 An IF Communication Circuit Tutorial
AN1580 Mounting and Soldering Recommendations for the Motorola Power Flat Pack Package
AN1602 3.6 V and 4.8 V GSM/DCS1800 Dual Band PA Application with DECT Capability Using Standard Motorola RFIC's
AN1617 Mounting Recommendations for Copper Tungsten Flanged Transistors
AN1639 Phase Noise Measurement Using the Phase Lock Technique
AN1643 RF LDMOS Power Modules for GSM Base Station Application: Optimum Biasing Circuit
AN1670 60 Watts, GSM 900 MHz, LDMOS Two–Stage Amplifier
AN1671 MC145170 PSpice Modeling Kit
AN1673 Solder Reflow Mounting Method for the MRF286 and Similar Packages
AN1674 Mounting Method with Mechanical Fasteners for the MRF286 and Similar Packages
AN1696 Broadband Intermodulation Performance Development Using the Rohde & Schwarz Vector Network Analyzer ZVR
AN1697 GSM900/DCS/1800 Dual–Band 3.6 V Power Amplifier Solution with Open Loop Control Scheme
AN1907 Surface Mount Solder Attach Method for the MRF9045MR1 in the TO–270 Plastic RF Package
AN1908 Solder Mounting Method for the MRF19090S and Similar Packages
AN1923 Mounting Method with Mechanical Fasteners for the MRF19090 and Similar Packages
AN4005 Thermal Management and Mounting Method for the PLD 1.5 RF Power Surface Mount Package

Article Reprints

AR164 Good RF Construction Practices and Techniques
AR254 Phase–Locked Loop Design Articles
AR510 VSWR Protection of Solid State RF Power Amplifiers
AR511 Biasing Solid State Amplifiers to Linear Operation
AR579 CAD of a Broadband, Class–C 65 Watt UHF Power Amplifier
AR581 Procedure Performs Thermal Measurements on Pulsed Devices
AR612 Plastic Packages Hold Power RF MOSFETs
AR624 Aluminum–Based Metallization Enhances Device Reliability
AR628 Impedance Measurements for High Power RF Transistors Using the TRL Method
AR629 Digital Predistortion Techniques for RF Power Amplifiers with CDMA Applications

Engineering Bulletins

EB38 Measuring the Intermodulation Distortion of Linear Amplifiers
EB105 A 30 Watt, 800 MHz Amplifier Design
EB209 Mounting Method for RF Power Leadless Surface Mount Transistors
EB211 Thermal Management and Solder Mounting Method for the MRF286, 60 Watt Power Device in a CuW (Copper Tungsten) Base Package

Product Literature

DL110/D Wireless RF Product Device Data Book
SG46/D Wireless RF Product Selector Guide
CD301PC/D Wireless RF Product Data Library for PC CD–ROM

Chapter Eleven

Motorola Distributor & Worldwide Sales Offices

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